# Studies on Current Hysteresis Controllers And Low Order Harmonic Suppression Techniques for IM Drives with Dodecagonal Voltage Space Vectors

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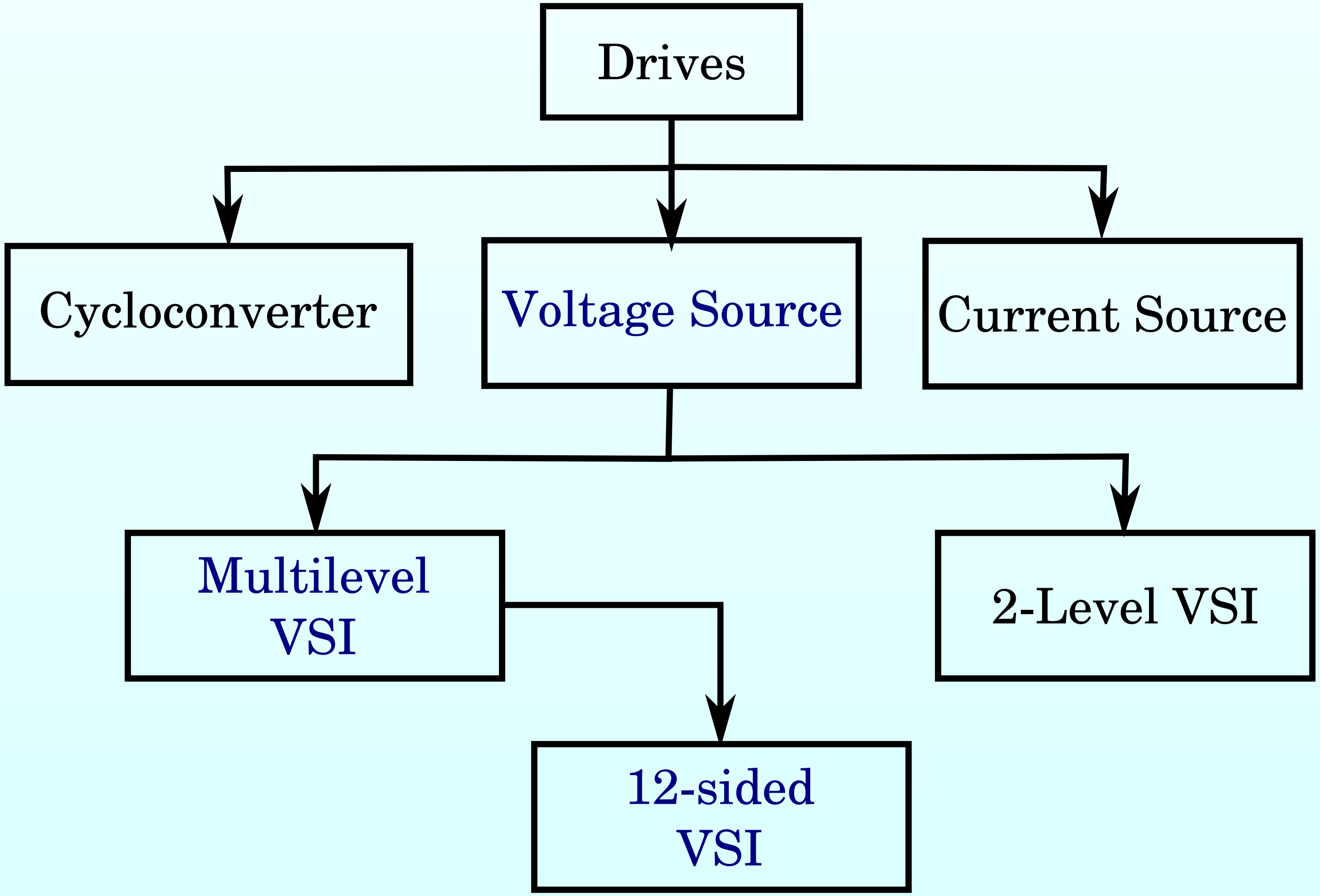
# Organization

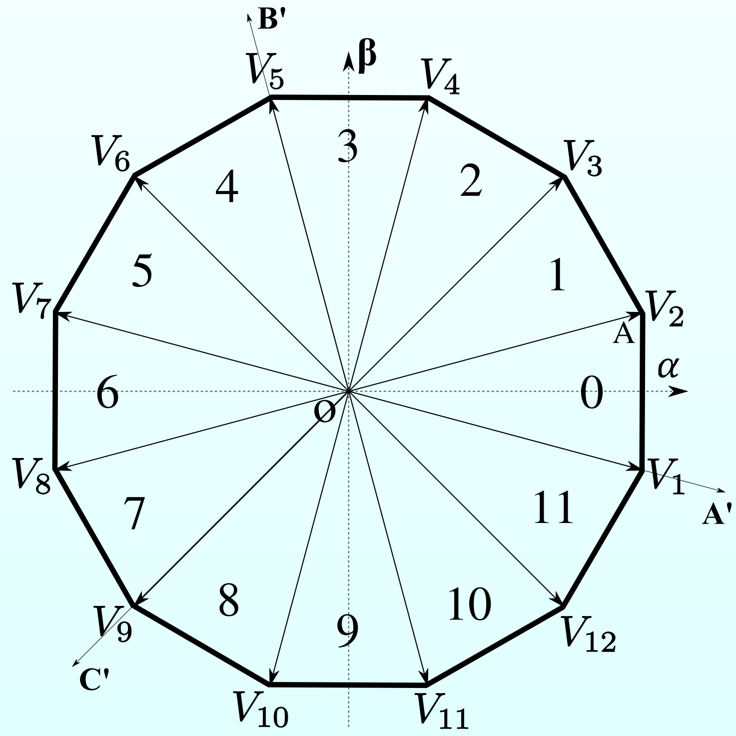
- Introduction
- A nearly constant switching frequency CESV based hysteresis controller for an IM drive with single dodecagonal voltage space vectors
- A nearly constant switching frequency CESV based hysteresis controller for an IM drive with multilevel dodecagonal voltage space vectors
- A 5th and 7th order harmonic suppression scheme for open-end winding split-phase IM drive using capacitor-fed inverters
- Conclusion and future scope

# Induction Motor Drives



# 12-sided polygonal space vector diagram

- Advantages of Dodecagon
  - Elimination of 6n ± 1,(n=odd) harmonics
  - Increased modulation range



# Controllers for VSI

- PWM Voltage source Inverters
  - Voltage controlled PWM VSI
  - Current controlled PWM VSI
- Features of current controlled PWM VSI
  - Simple logic, easily implemented
  - Excellent dynamic response
  - Inherent short-circuit protection
  - Disadvantages - large current ripple in steady-state, switching frequency variation

# Current Controlled PWM VSI

- Ramp comparison controller
- Predictive Current controller
- Hysteresis Current Controller (HCC)
- Neural network controller
- Fuzzy logic controller

# Hysteresis Current Controlled VSI

- Fixed tolerance band HCC
  - Switching frequency variation in a fundamental cycle & change in motor speed
  - Non-optimum current ripple
  - Harmonic content in load current - overheating of machine
- Variable tolerance band HCC
  - Variable hysteresis band for constant switching frequency
    - Adaptive hysteresis band
    - Sinusoidal hysteresis band
  - Disadvantages - complex logic, stability problems,
    limitations in transient performnce

# Space Phasor Variable band HCC VSI

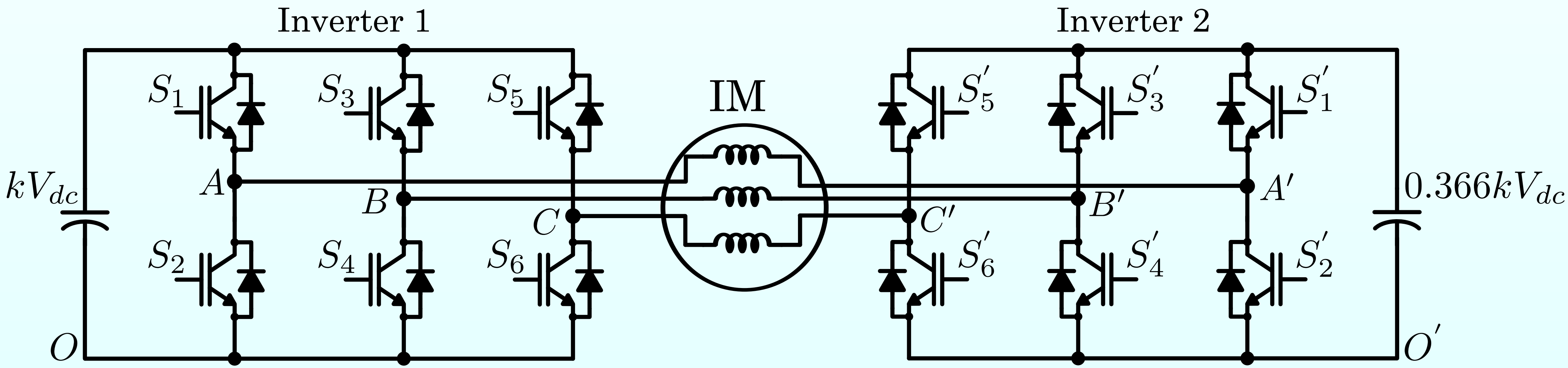
- Continuously varying parabolic boundary for Curret Error Space Phasor
  - Selection of proper shape & size of parabolic boundary for CESV
  - Proper orientation of parabolic boundary along orthogonal X-Y axes
    - Identify current sector
  - Vector selection to minimize switching

# A nearly constant switching frequency CESV based hysteresis controller for an IM drive with single dodecagonal voltage space vectors

# Organization

- Power circuit and space-vector diagram
- Analysis of CESV in VC-SVPWM
- Parabolic CESV boundaries for nearly constant switching frequency
- Vector selection logic for proposed controller
- Sector detection logic for proposed controller
- Block diagram of the proposed controller
- Simulation and experimental results
- Conclusion

# Power circuit of the proposed inverter



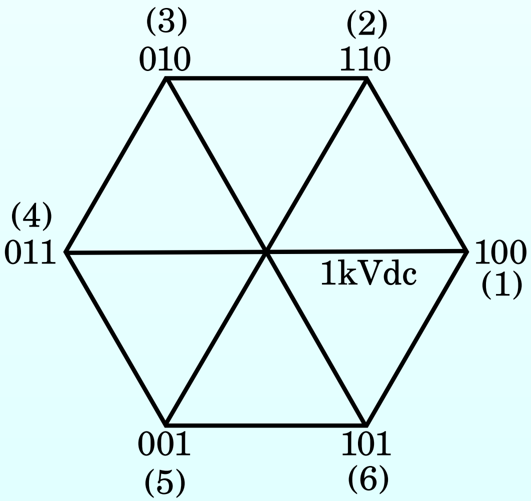

- Open-end winding Induction Motor fed from 2-level inverters from both sides
- Asymmetrical DC link Voltages
- Pole Voltages of Inverter-1 → V(A,O), V(B,O), V(C,O)
- Pole Voltages of Inverter-2 → V(A',O'), V(B',O'), V(C',O')
- Phase Voltages are differences of respective pole voltages of two inverters

# Dodecagonal space vector diagram

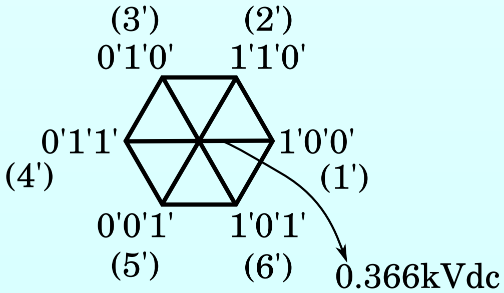
- Individual hexagons

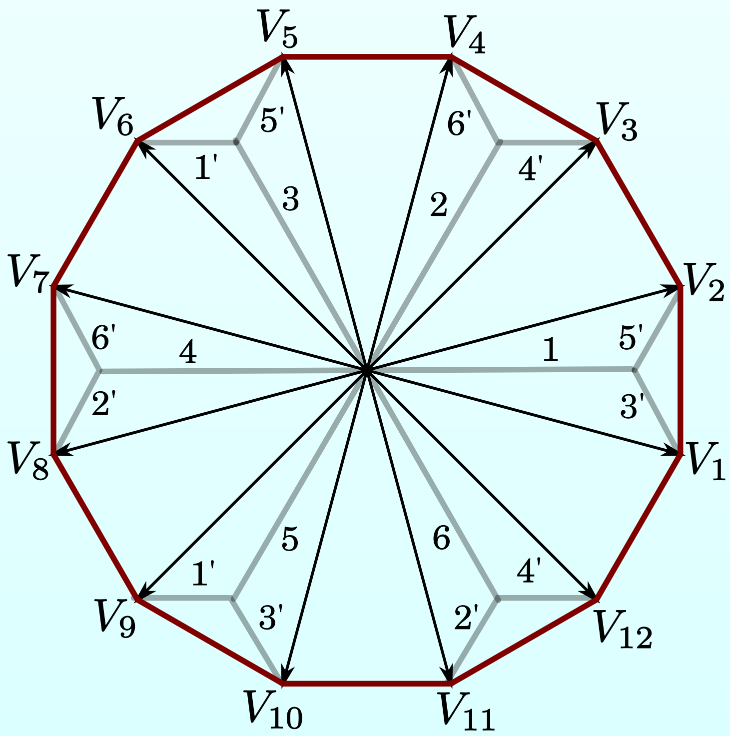
Resultant dodecagon

Inverter 1




Inverter 2

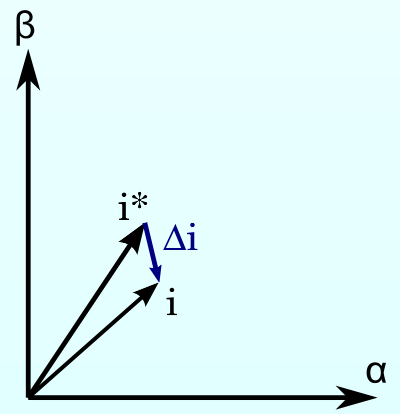


# Proposed HCC

- Analyse boundary of constant switching frequency VC-SVPWM
- Use boundary of VC-SVPWM to get constant switching frequency in steady state
- Identify sector and switch appropriate vectors

# Current Error Space Vector (CESV)



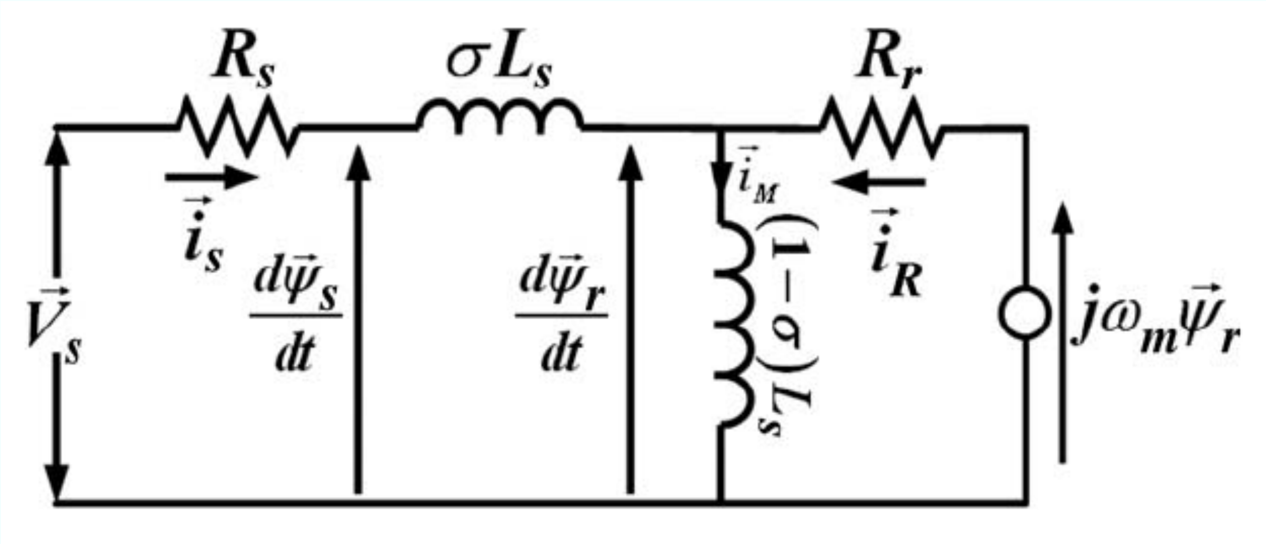

Current-Error in space phasor Diagram

- Current Error Space Vector: Δi = i - i*

$$\Delta i = \Delta i_A + \Delta i_B \ e^{j(2\pi/3)} + \Delta i_C \ e^{j(4\pi/3)}$$

$$\Delta i = \Delta i_\alpha + j\Delta i_\beta$$

# Dynamic Equation of Current Error




Space phasor based equivalent circuit of IM in the stationary reference frame with rotor flux as reference vector

$$\vec{V}_k = R_s\vec{i}_s + \sigma L_s\frac{d\vec{i}_s}{dt} + \frac{d\vec{\Psi}_r}{dt};$$

$$\vec{i}_s = \vec{i}_s^* + \Delta\vec{i}_s$$

$$\vec{V}_k = R_s\left(\vec{i}_s^* + \Delta\vec{i}_s\right) + \sigma L_s\frac{d\left(\vec{i}_s^* + \Delta\vec{i}_s\right)}{dt} + \frac{d\vec{\Psi}_r}{dt}$$

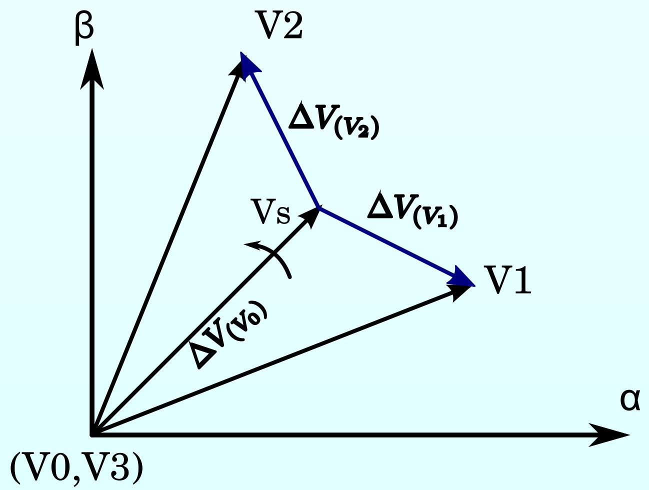
$$taking \quad \vec{V}_s = R_s\vec{i}_s^* + \sigma L_s\frac{d\vec{i}_s^*}{dt} + \frac{d\vec{\Psi}_r}{dt}$$

$$then \quad \vec{V}_k = \vec{V}_s + R_s\Delta\vec{i}_s + \sigma L_s\frac{d\Delta\vec{i}_s}{dt}$$

$$\vec{V}_k \approx \vec{V}_s + \sigma L_s\frac{d\Delta\vec{i}_s}{dt} \quad \Rightarrow \quad \frac{d\Delta\vec{i}_s}{dt} = \frac{\vec{V}_k - \vec{V}_s}{\sigma L_s} = \frac{\Delta V_{(V_k)}}{\sigma L_s}$$

$$integrating \;\; both \;\; sides \;\; \Delta i_{(V_k)} = \frac{\Delta V_{(V_k)}}{\sigma L_s}t$$

# CESV For VC-SVPWM Inverter




Voltage-error vectors for diffrent Vectors

- From dynamic equation of current error:

$$\Delta i_{(V_k)} = \frac{\Delta V_{(V_k)}}{\sigma L_s} t$$

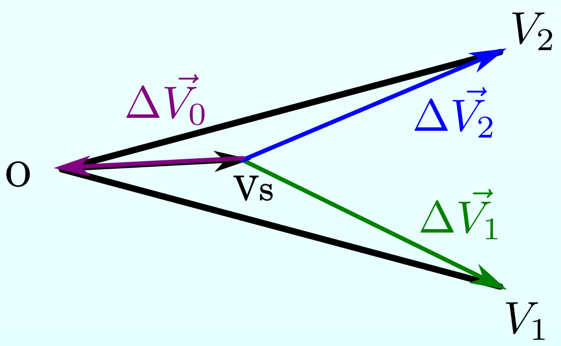
- In a switching cycle Ts - V1, V2 & V0 vectors are applied for T1,T2 & T0 duration respectively
- The current errors at end of each vector are:

$$\Delta i_{(V_1)} = \frac{\Delta V_{(V_1)}}{\sigma L_s} T_1$$

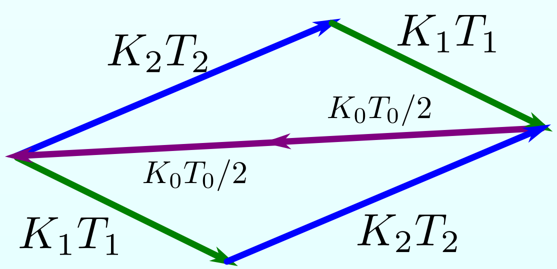
$$\Delta i_{(V_2)} = \frac{\Delta V_{(V_2)}}{\sigma L_s} T_2$$

$$\Delta i_{(V_0)} = \frac{\Delta V_{(V_0)}}{\sigma L_s} T_0$$

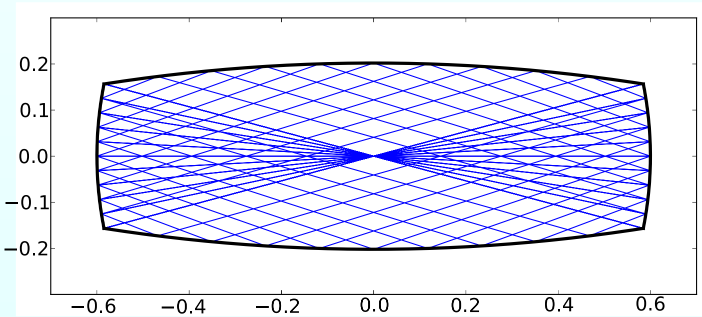
# CESV Trajectory of VC-SVPWM inverter




sector 0

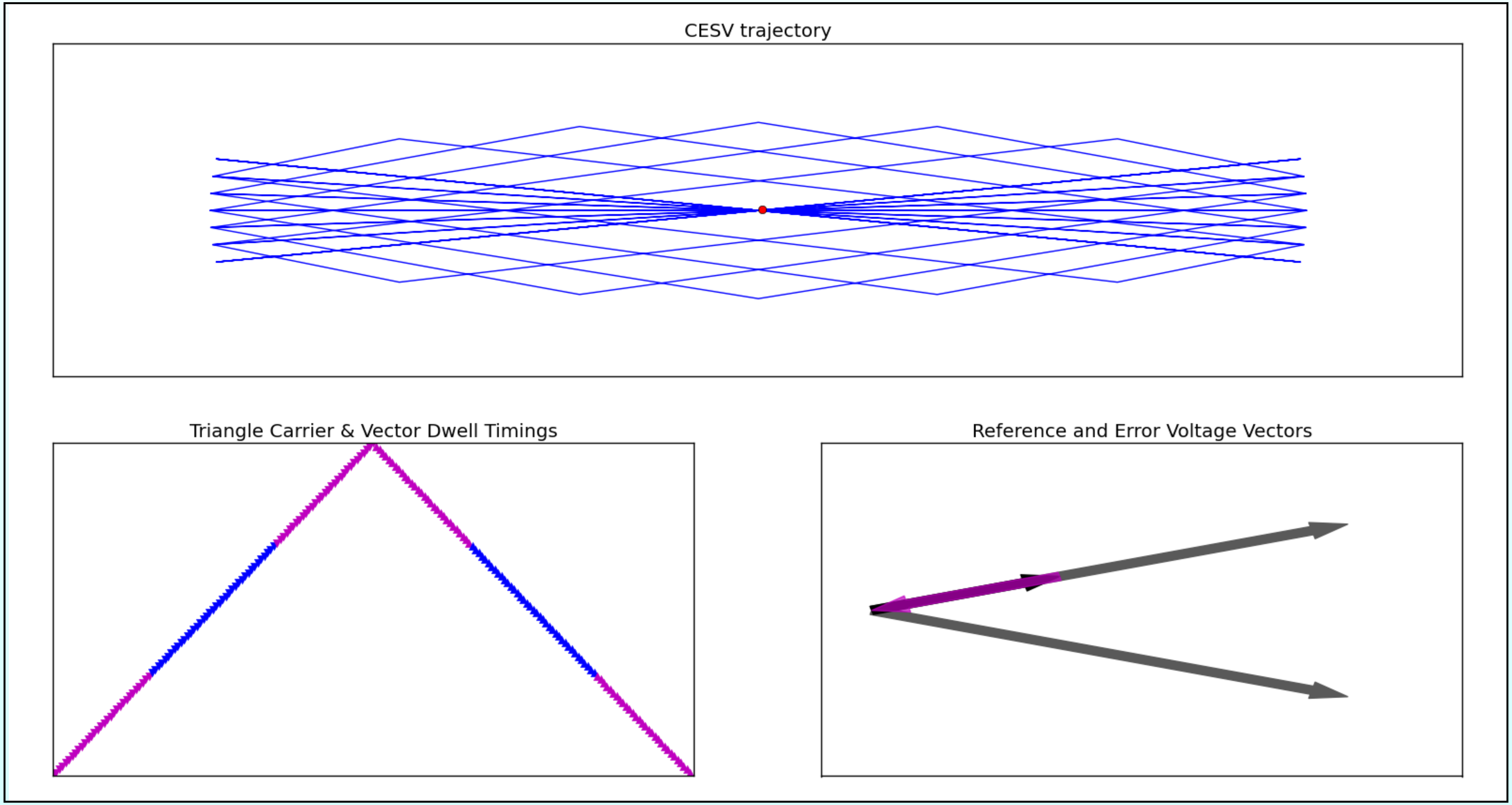



$$K_i = \frac{\Delta\vec{V_i}}{\sigma L_s}$$

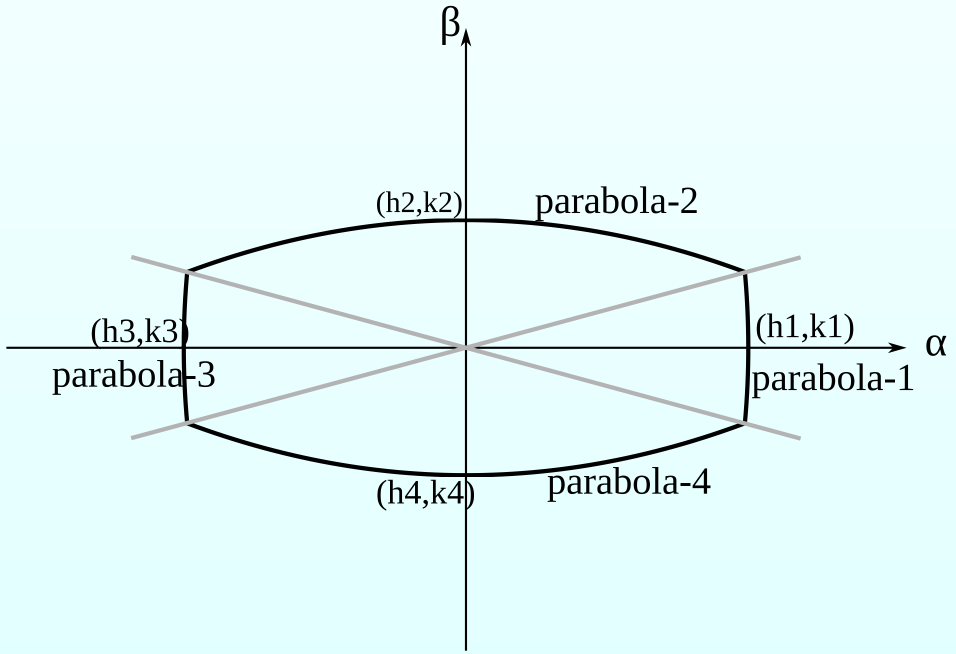


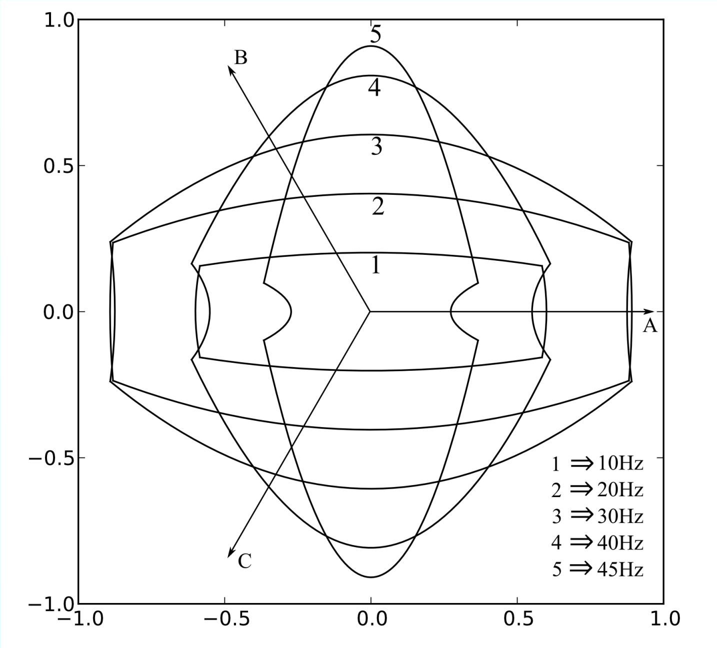

- For each sampled point of Vs in a VC-SVPWM based inverter, CESV trajectory is traced out for vectors V1, V2 & V0
- The corner points of all trajectories in a sector gives the boundary for that sector

# CESV Trajectory of VC-SVPWM inverter



# CESV Boundaries for 12-sided Inverter Fed Drive



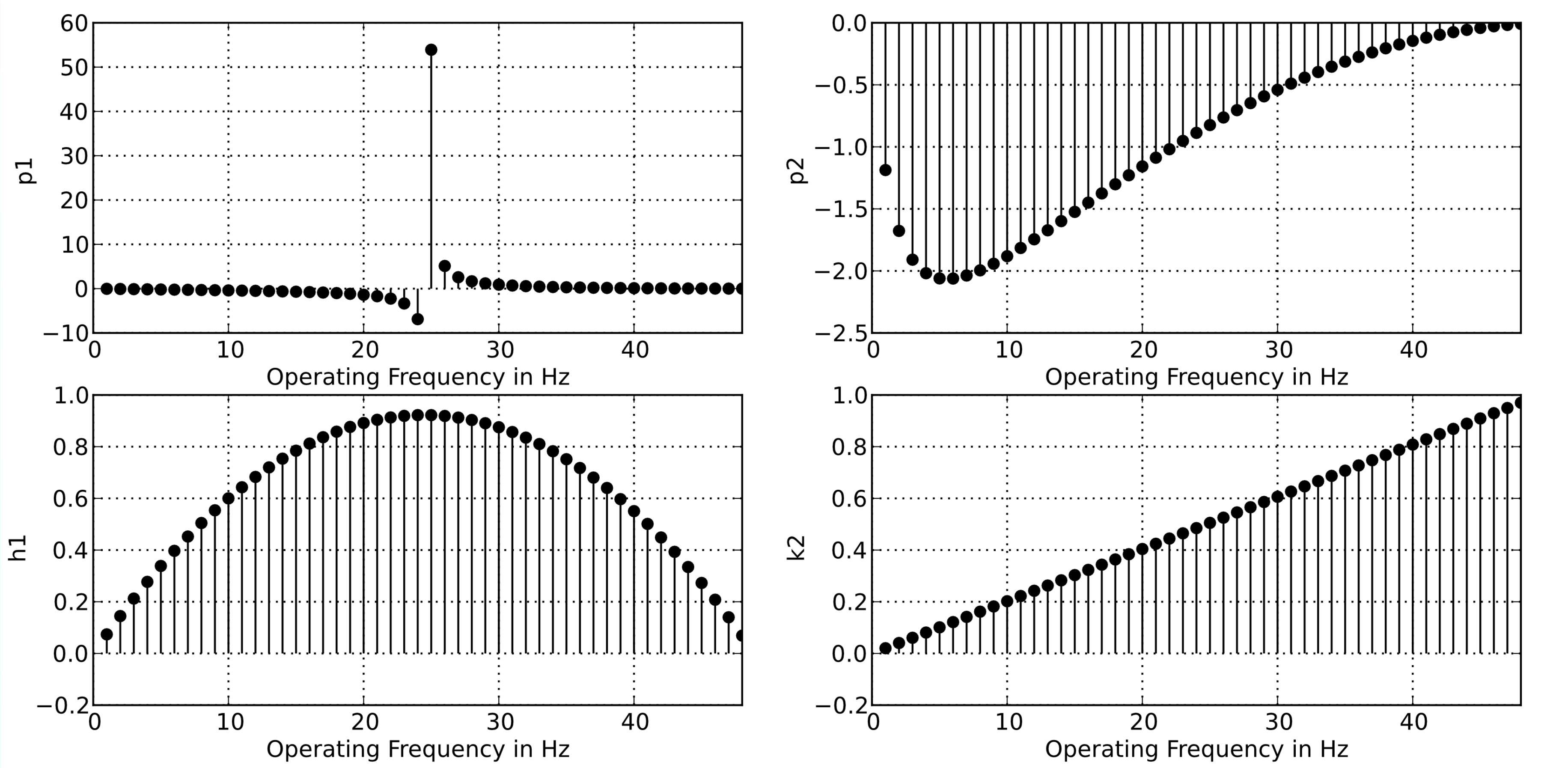




- Current error boundary formed by four unique parabolas
- Parabolic boundaries varies with magnitude of Vs vector
- Characterized by equations:

$$(x-h)^2 = 4p\,(y-k) \;\; and\,(y-k)^2 = 4p\,(x-h)$$

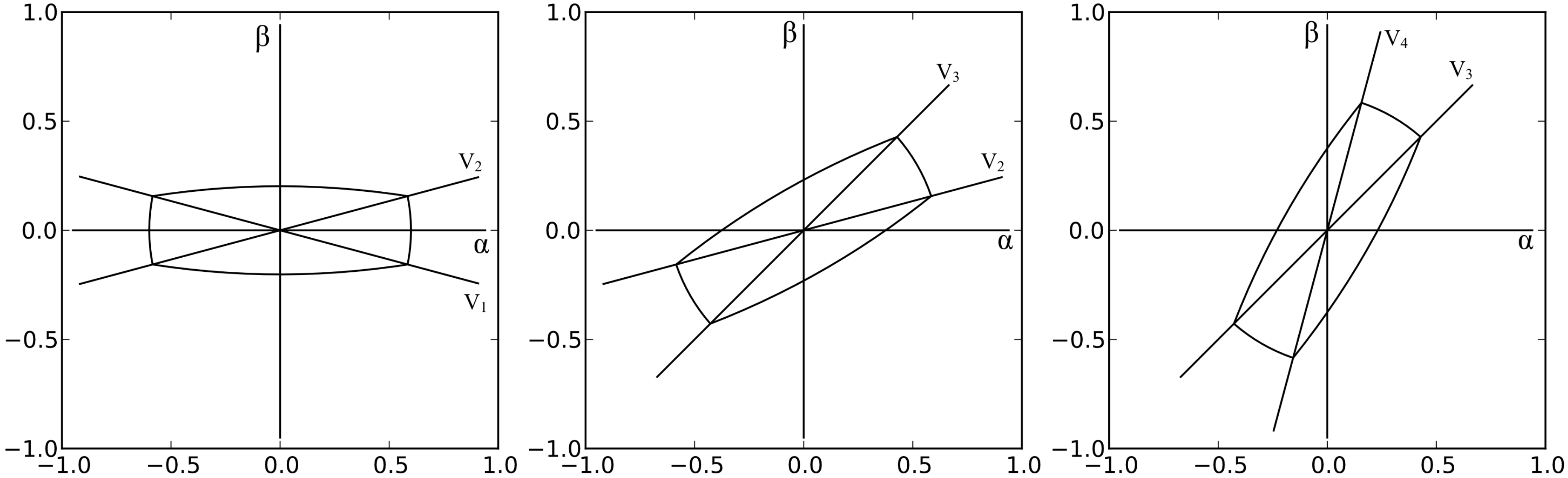
- Four parameters p1,p2,h1,k2 are sufficient to define the parabolic boundary

# Variation of Parabola parameters




- Variation of parabola parameters p1, p2, h1, k2 for variation in frequency from 0 to 48Hz
- Four look-up tables are used for selecting these four boundary parameters

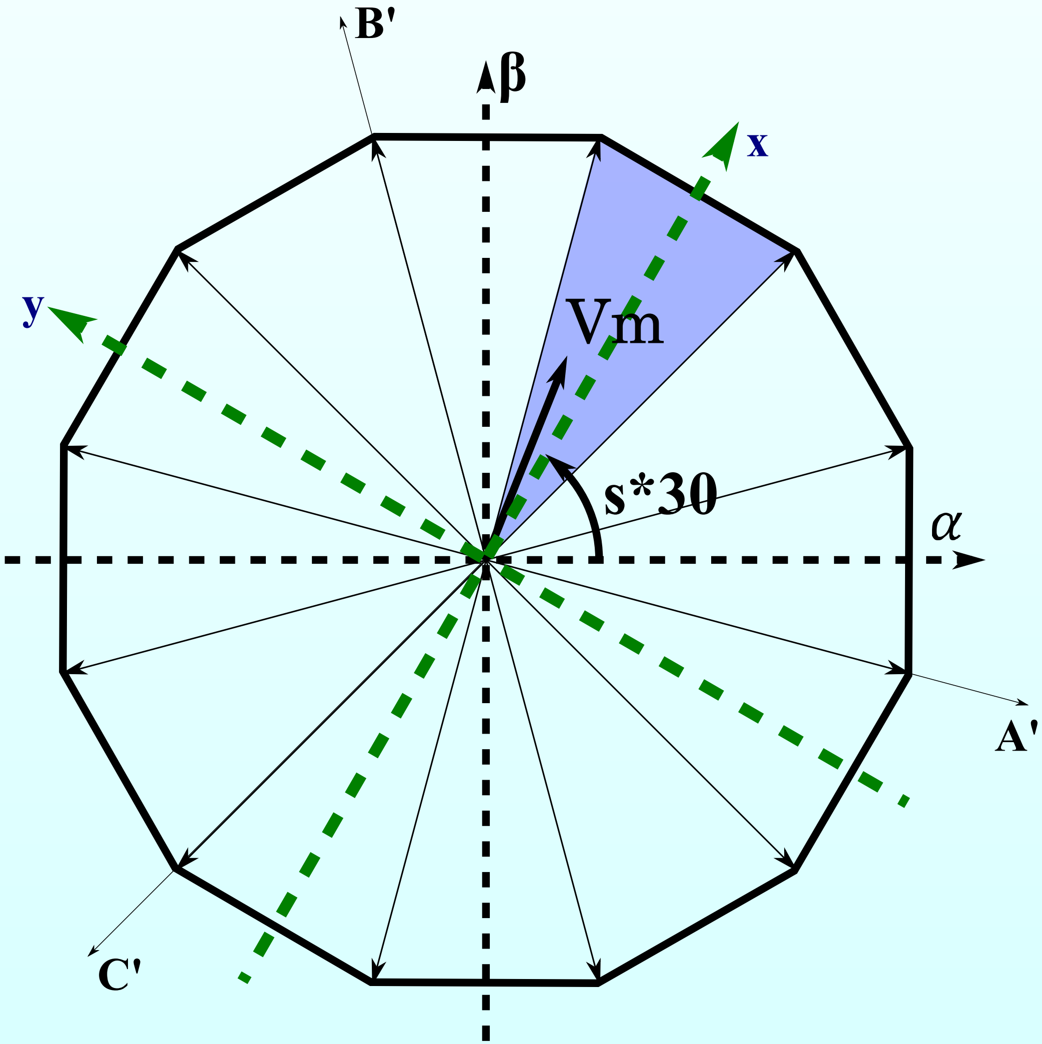
# CESV Boundaries For Different Sectors




CESV boundaries for sectors 0,1,2 at 10Hz

- Identical CESV boundaries for different sectors
- Single set of parabolic equations is sufficient
  - transform CESV to an x-y axis passing through center of current sector

# Transformation to General Reference Frame

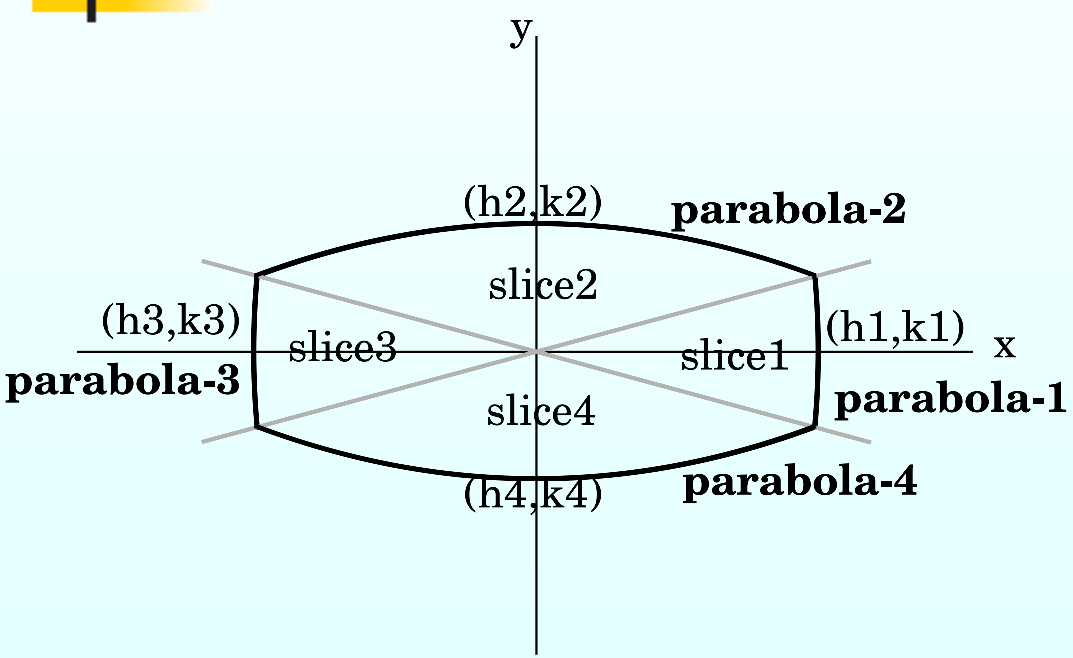



- Transform CESV from α – β axis to x-y axis passing through center of current sector - (s)

$$\Delta i_x = \Delta i_\alpha cos(s \times 30^o) + \Delta i_\beta sin(s \times 30^o)$$
$$\Delta i_y = -\Delta i_\alpha sin(s \times 30^o) + \Delta i_\beta cos(s \times 30^o)$$

- Reduces computation complexity

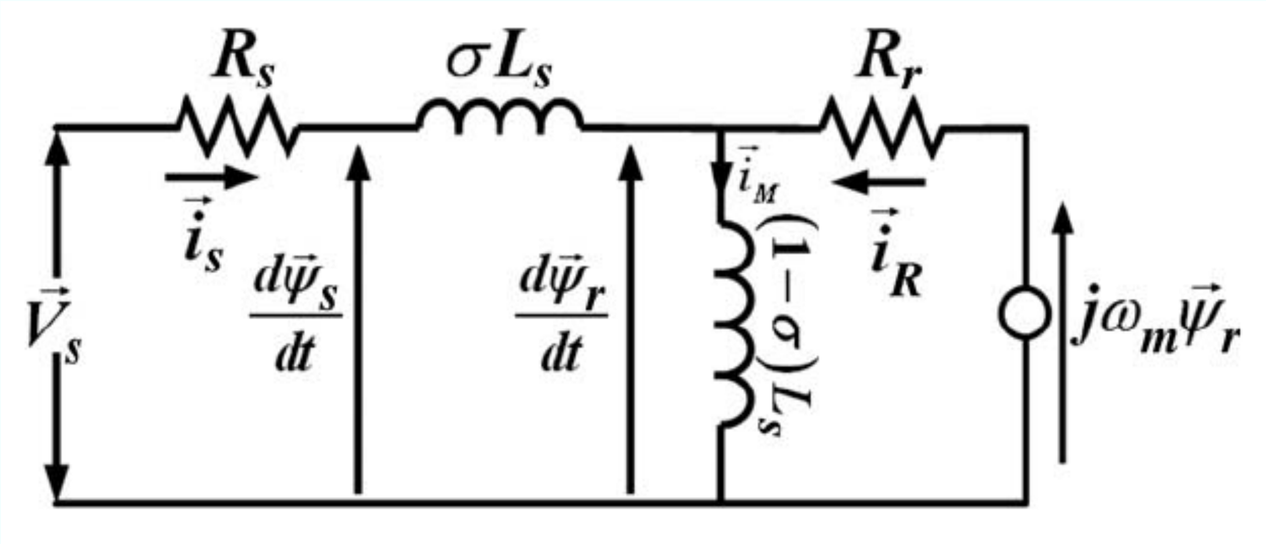
# Vector Selection Logic




- Generalized vector selection logic
  - for all sectors
  - for both directions
- V1 - first vector in current sector
- V2 - second vector in current sector
- V0,V3 - zero vectors

| Present Vector | $\lvert y\rvert - \lvert x\rvert \tan 15 < 0$ | | $\lvert y\rvert - \lvert x\rvert \tan 15 \geq 0$ | |
|---|---|---|---|---|
| | x < 0 & $sign(p1)(y^2 + 4p_1(x + h_1)) < 0$ | x > 0 & $sign(p1)(y^2 - 4p_1(x - h_1)) < 0$ | y<0 & $(x^2 + 4p_2(y + k_2)) \geq 0$ | y>0 & $(x^2 - 4p_2(y - k_2)) \geq 0$ |
| V0 | V1 | | V2 | V1 |
| V1 | | V0 | V2 | |
| V2 | | V3 | | V1 |
| V3 | V2 | | V2 | V1 |

# Estimating of Fundamental Stator Voltage




Space phasor based equivalent circuit of IM in the stationary reference frame with rotor flux as reference vector

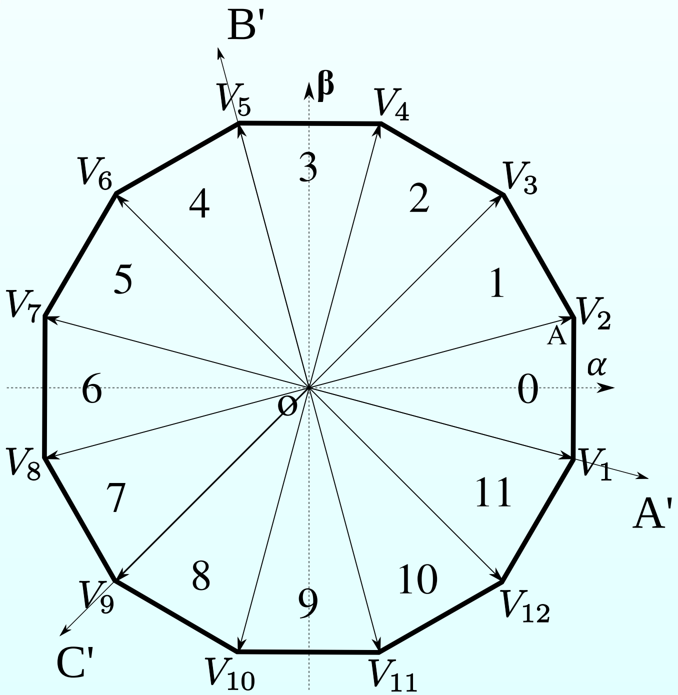
$$\overrightarrow{V_k} = \overrightarrow{V_s} + R_s\Delta\overrightarrow{i_s} + \sigma L_s\frac{d\Delta\overrightarrow{i_s}}{dt}$$

$$\Rightarrow \overrightarrow{V_s} = \overrightarrow{V_k} - R_s\Delta\overrightarrow{i_s} - \sigma L_s\frac{d\Delta\overrightarrow{i_s}}{dt}$$

$$\Rightarrow V_{s\alpha} = V_{k\alpha} - \Delta i_{s\alpha}R_s - \sigma L_s\frac{d\Delta i_{s\alpha}}{dt}$$

$$\& \; V_{s\beta} = V_{k\beta} - \Delta i_{s\beta}R_s - \sigma L_s\frac{d\Delta i_{s\beta}}{dt}$$

# Sector Detection Logic




| Condition | | Sector |
|---|---|---|
| $V_a' > V_b' > V_c'$ | $V_b' < 0$ | $sect0$ |
| | $V_b' \geq 0$ | $sect1$ |
| $V_b' > V_a' > V_c'$ | $V_a' \geq 0$ | $sect2$ |
| | $V_a' < 0$ | $sect3$ |
| $V_b' > V_c' > V_a'$ | $V_c' < 0$ | $sect4$ |
| | $V_c' \geq 0$ | $sect5$ |
| $V_c' > V_b' > V_a'$ | $V_b' \geq 0$ | $sect6$ |
| | $V_b' < 0$ | $sect7$ |
| $V_c' > V_a' > V_b'$ | $V_a' < 0$ | $sect8$ |
| | $V_a' \geq 0$ | $sect9$ |
| $V_a' > V_c' > V_b'$ | $V_c' \geq 0$ | $sect10$ |
| | $V_c' < 0$ | $sect11$ |

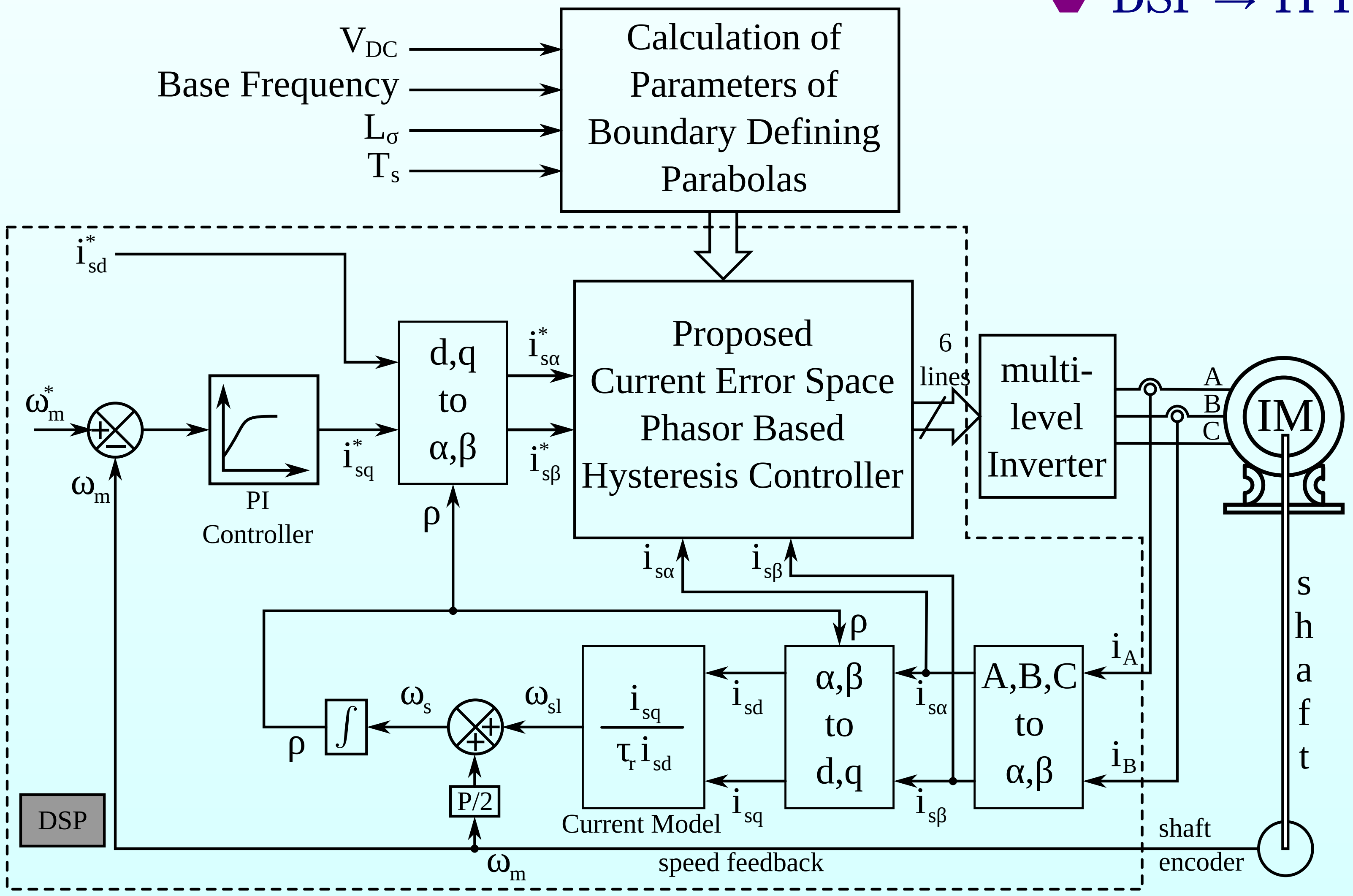
- $Transform\ V_{s\alpha}, V_{s\beta}\ to\ V_a', V_b', V_c'$

$$
\begin{aligned}
V_a' &= \quad 0.6440 \times V_{s\alpha} - 0.1725 \times V_{s\beta} \\
V_b' &= -0.1725 \times V_{s\alpha} + 0.6440 \times V_{s\beta} \\
V_c' &= -0.4714 \times V_{s\alpha} - 0.4714 \times V_{s\beta}
\end{aligned}
$$

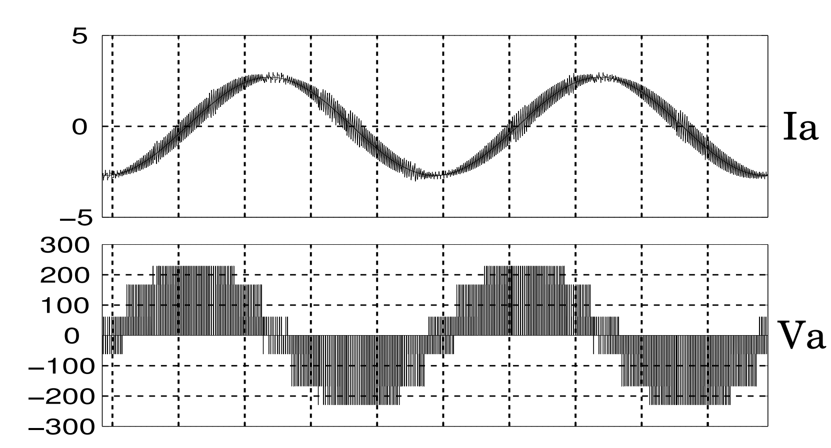
- Use Table to decide sector

# Block Diagram of the Proposed Controller

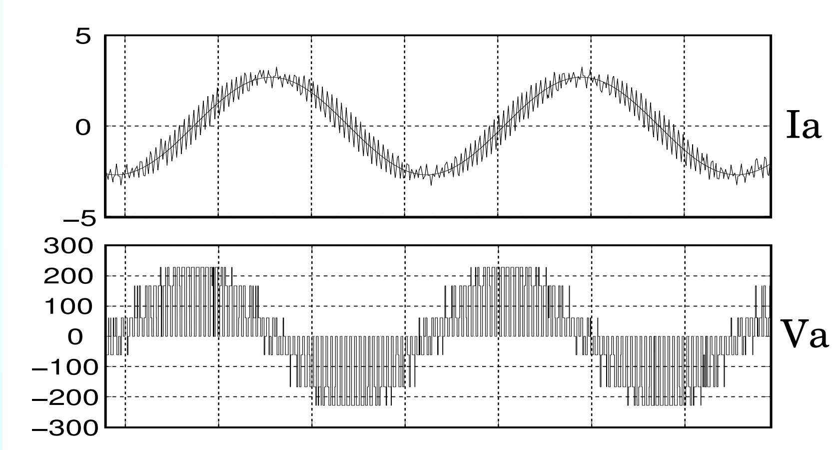
- DSP → TI TMS320LF2812A



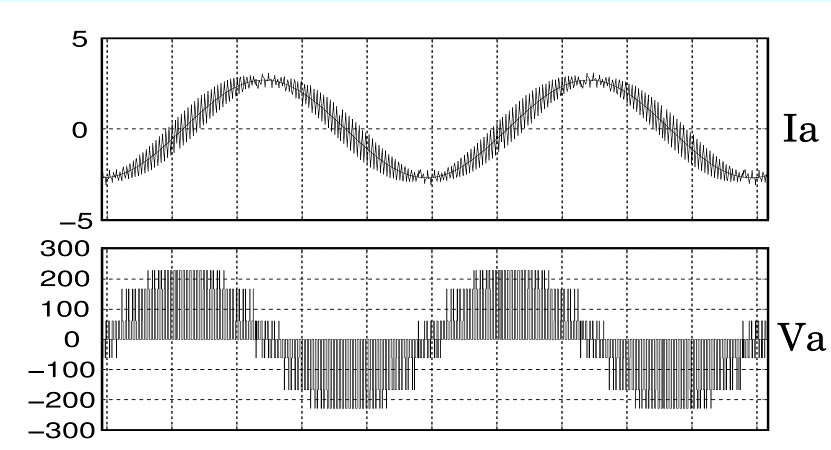
# Simulation Results - Phase Voltage & Current



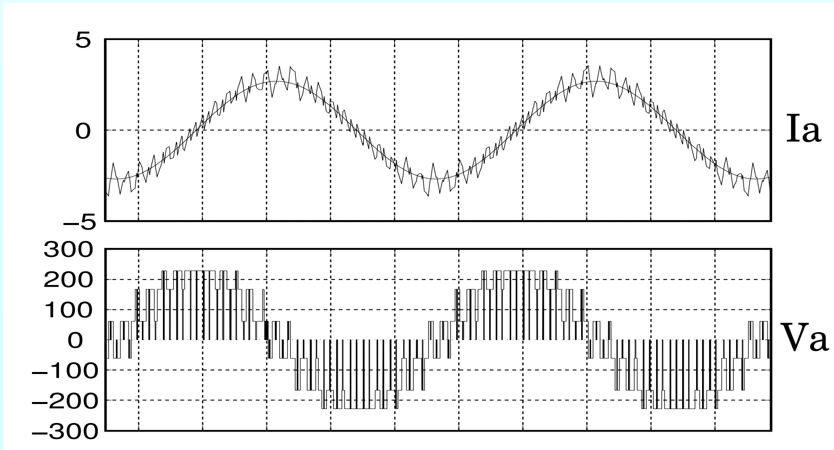

10Hz steady state, x-axis 20ms/div




30Hz steady state, x-axis 10ms/div



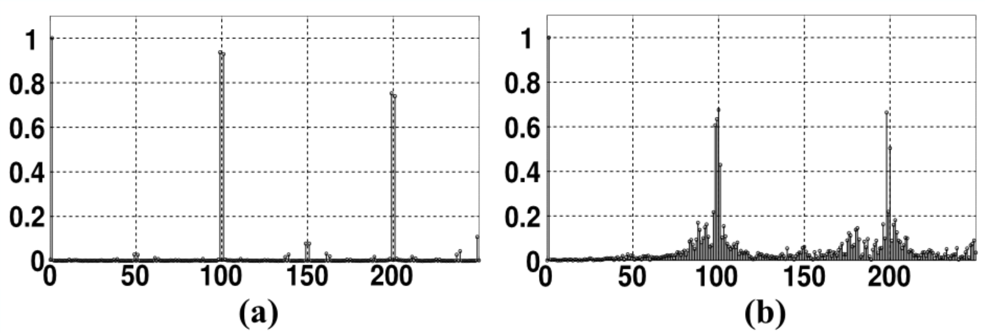

20Hz steady state, x-axis 10ms/div



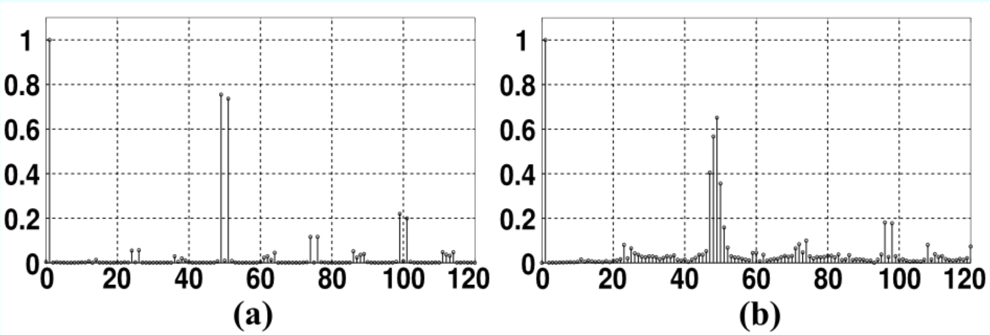

40Hz steady state, x-axis 5ms/div

# Simulation Results - FFTs

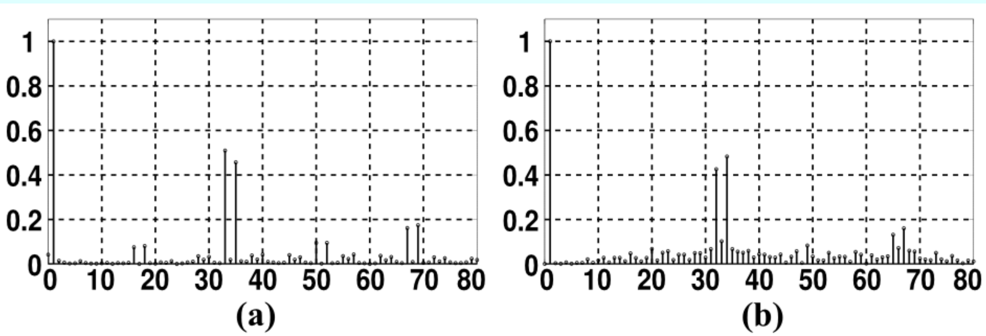
Normalized Harmonic Spectrum (FFT) of phase Voltage




@10Hz




@20Hz

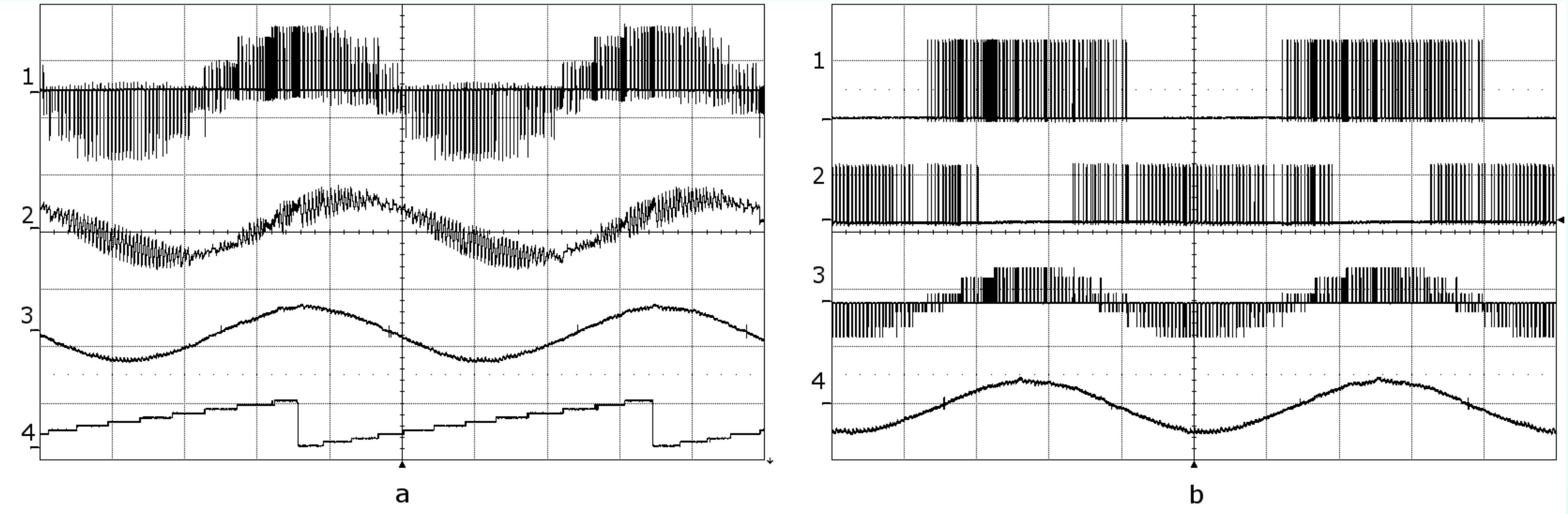



@30Hz

VC-SVPWM Proposed Controller

# Experimental Results

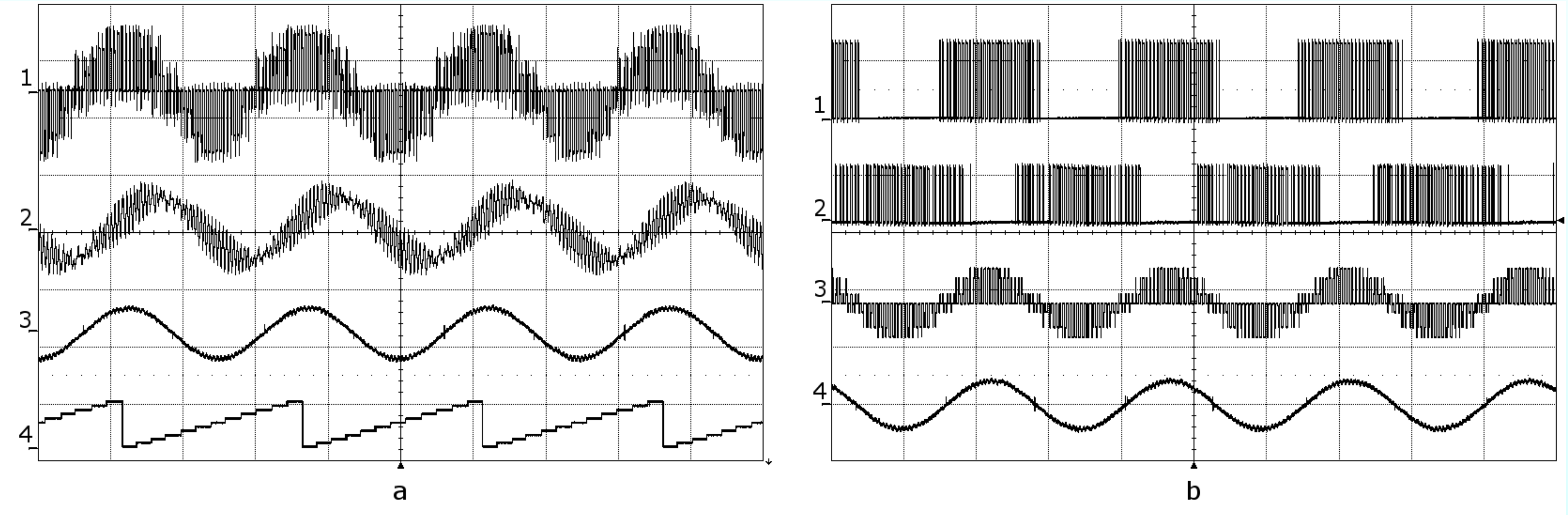
Steady State waveforms @10Hz




a1:Phase Voltage(200V/div), a2:Phase Current(1A/div),
a3:Estimated Stator Voltage(100V/Div) and a4:Sector;
b1:Inverter1 Pole Voltage A (200V/div), b2: Inverter2 Pole Voltage A' (100V/div),
b3:Phase Voltage A-A'(400V/div) and b4:Estimated Stator Voltage(100V/Div)
(X-axis 20ms/div)

# Experimental Results

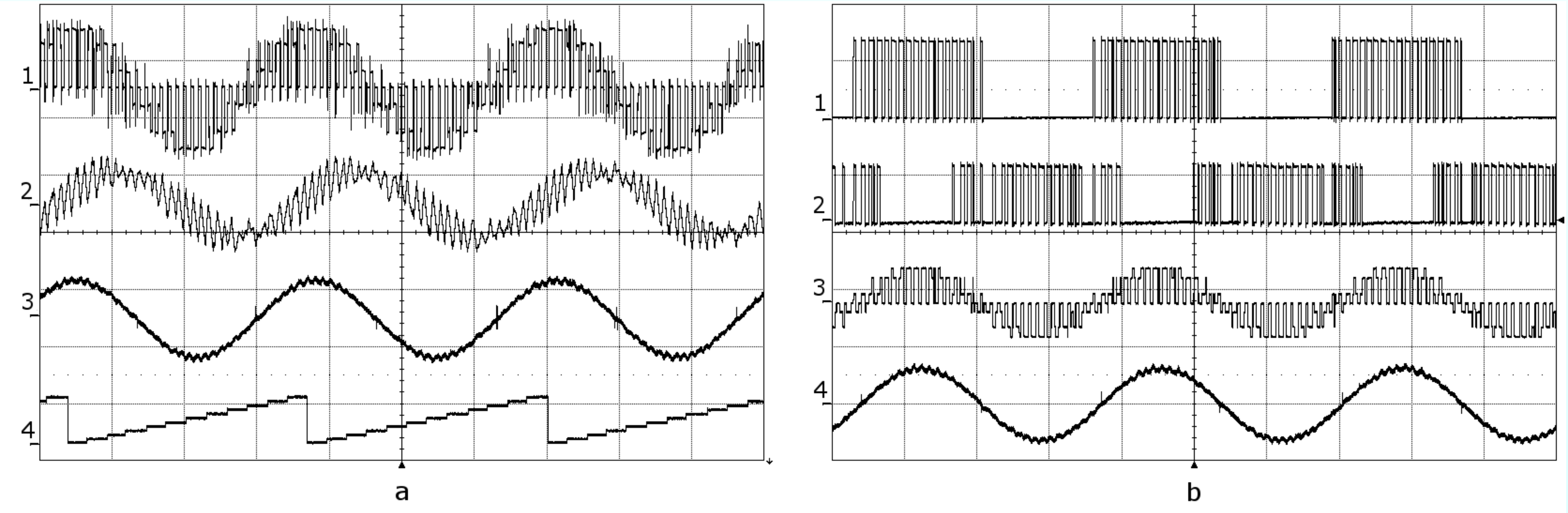
Steady State waveforms @20Hz




a1:Phase Voltage(200V/div), a2:Phase Current(1A/div),
a3:Estimated Stator Voltage(200V/Div) and a4:Sector;
b1:Inverter1 Pole Voltage A (200V/div), b2: Inverter2 Pole Voltage A' (100V/div),
b3:Phase Voltage A-A'(400V/div) and b4:Estimated Stator Voltage(200V/Div)
(X-axis 20ms/div)

# Experimental Results

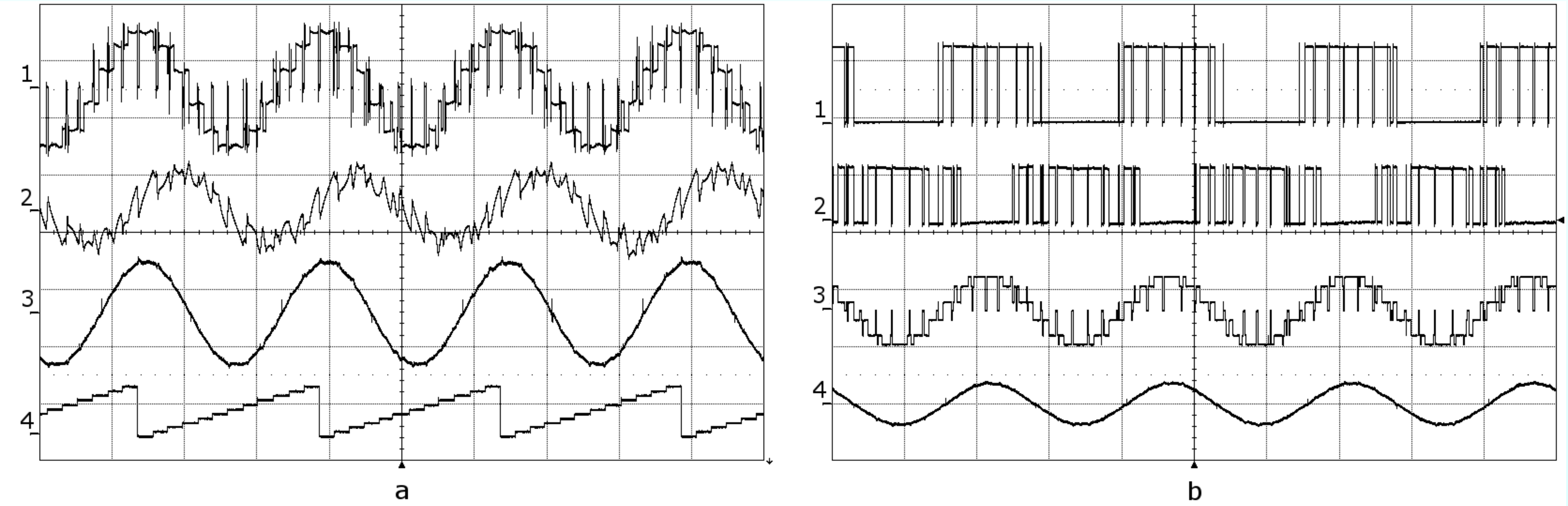
Steady State waveforms @30Hz




a1:Phase Voltage(200V/div), a2:Phase Current(1A/div),
a3:Estimated Stator Voltage(200V/Div) and a4:Sector;
b1:Inverter1 Pole Voltage A (200V/div), b2: Inverter2 Pole Voltage A' (100V/div),
b3:Phase Voltage A-A'(400V/div) and b4:Estimated Stator Voltage(200V/Div)
(X-axis 10ms/div)

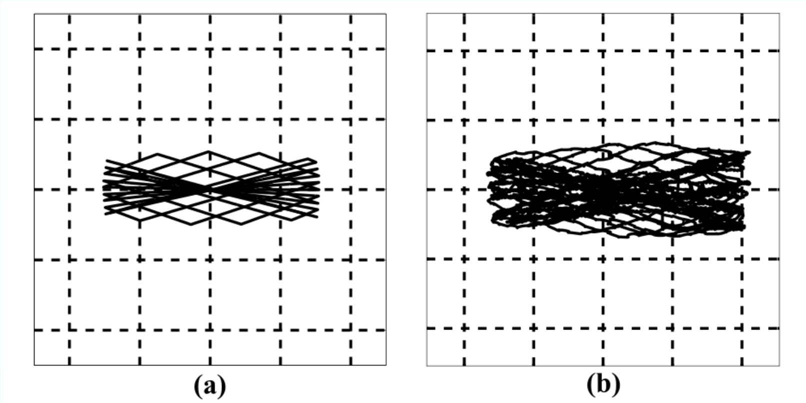
# Experimental Results

Steady State waveforms @40Hz

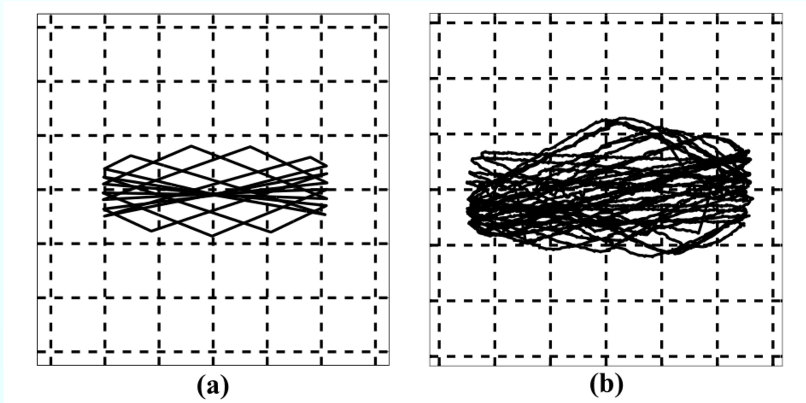



a1:Phase Voltage(200V/div), a2:Phase Current(1A/div),
a3:Estimated Stator Voltage(200V/Div) and a4:Sector;
b1:Inverter1 Pole Voltage A (200V/div), b2: Inverter2 Pole Voltage A' (100V/div),
b3:Phase Voltage A-A'(400V/div) and b4:Estimated Stator Voltage(500V/Div)
(X-axis 10ms/div)

# Current Error Space Phasor

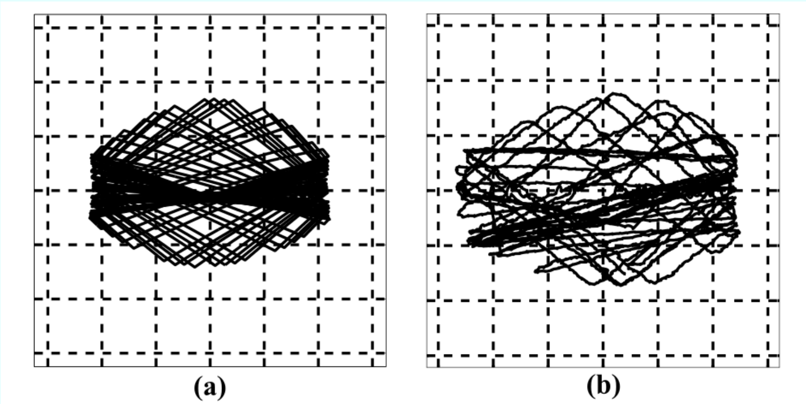



10Hz a)VC-SVPWM b)Proposed Controller

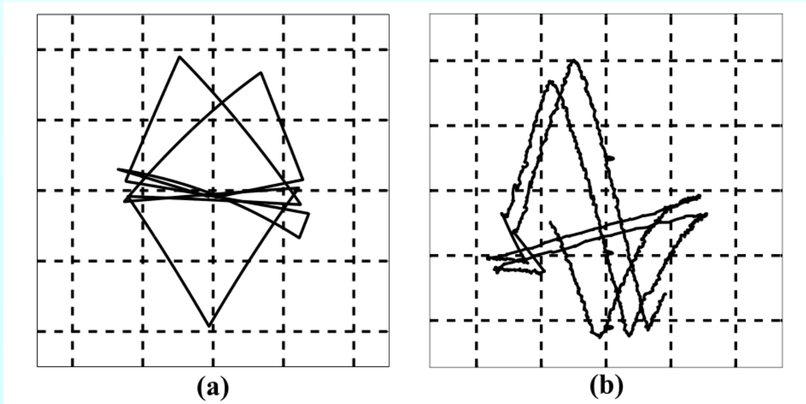



20Hz a)VC-SVPWM b)Proposed Controller

X & Y Axis 0.4A/div



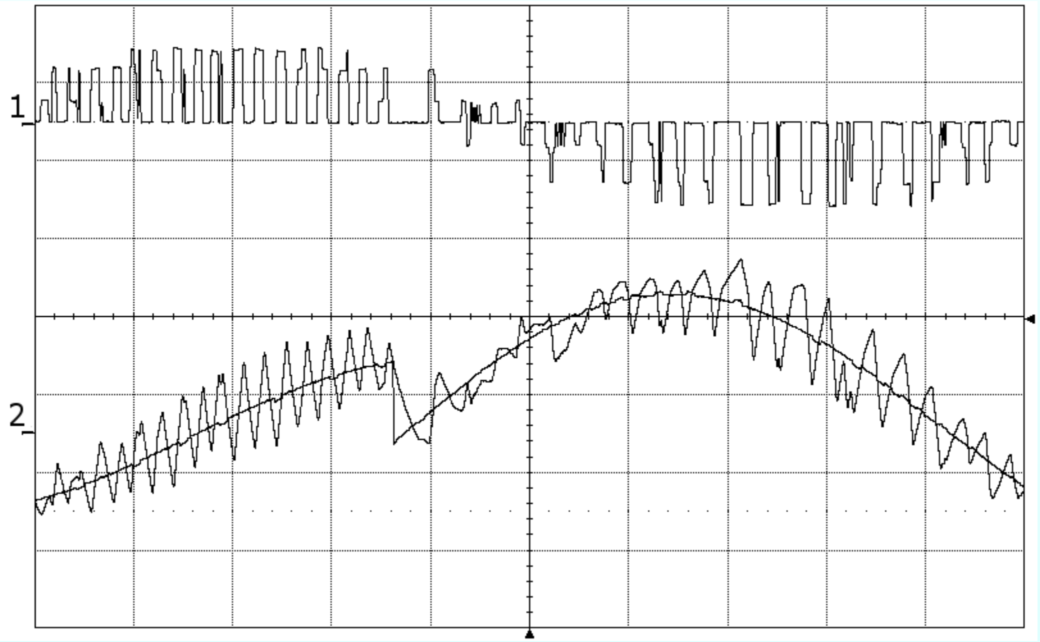

30Hz a)VC-SVPWM b)Proposed Controller



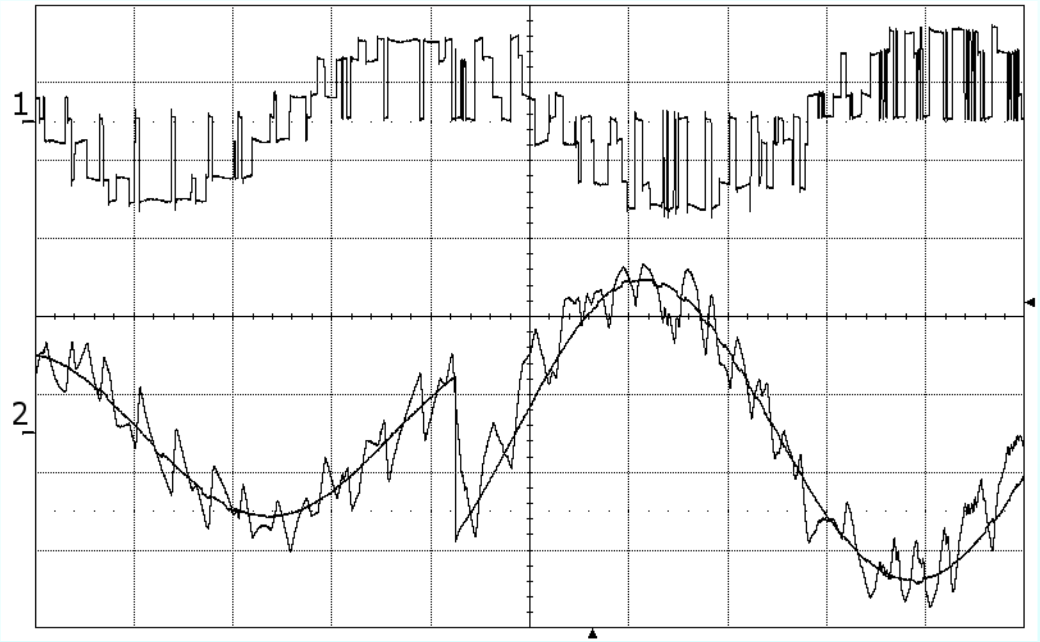

40Hz a)VC-SVPWM b)Proposed Controller

# Experimental Results

Proposed Hysteresis Controller characteristics when a sudden change in Isq* is applied



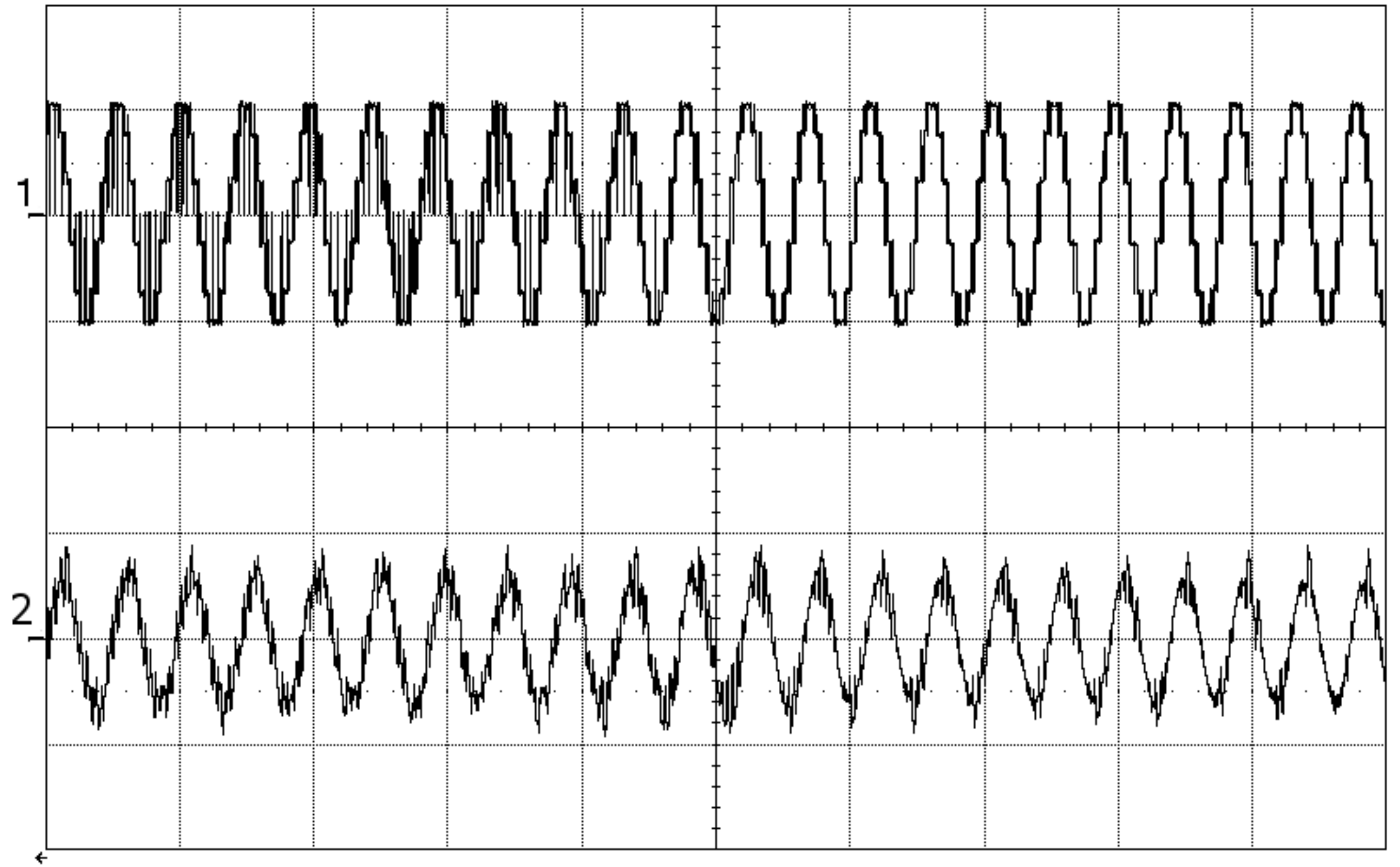

@20Hz




@40Hz

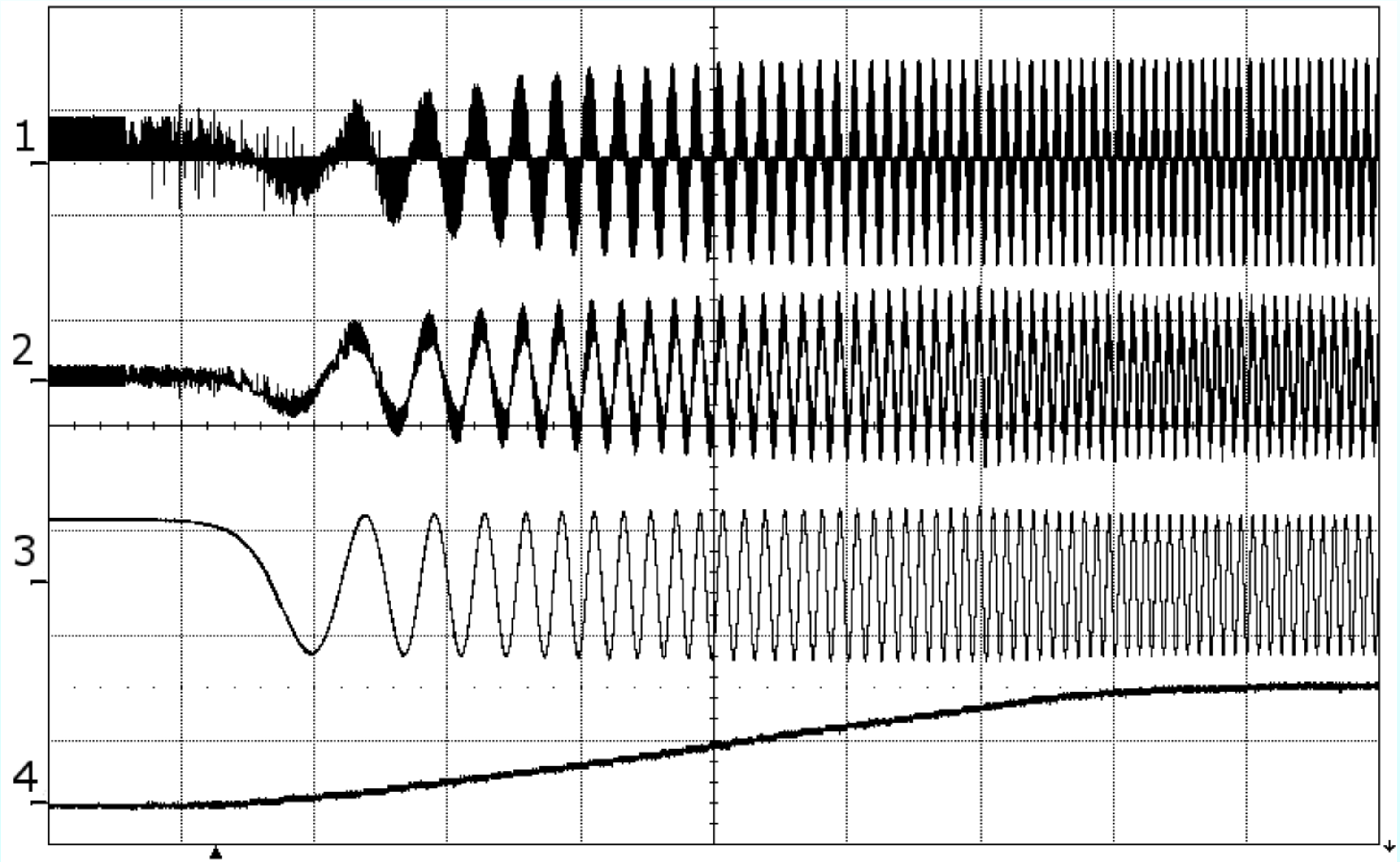
1:Phase voltage(200V/div) and
2:Phase current(0.5A/div)
(X-axis 5ms/div)

# Experimental Results



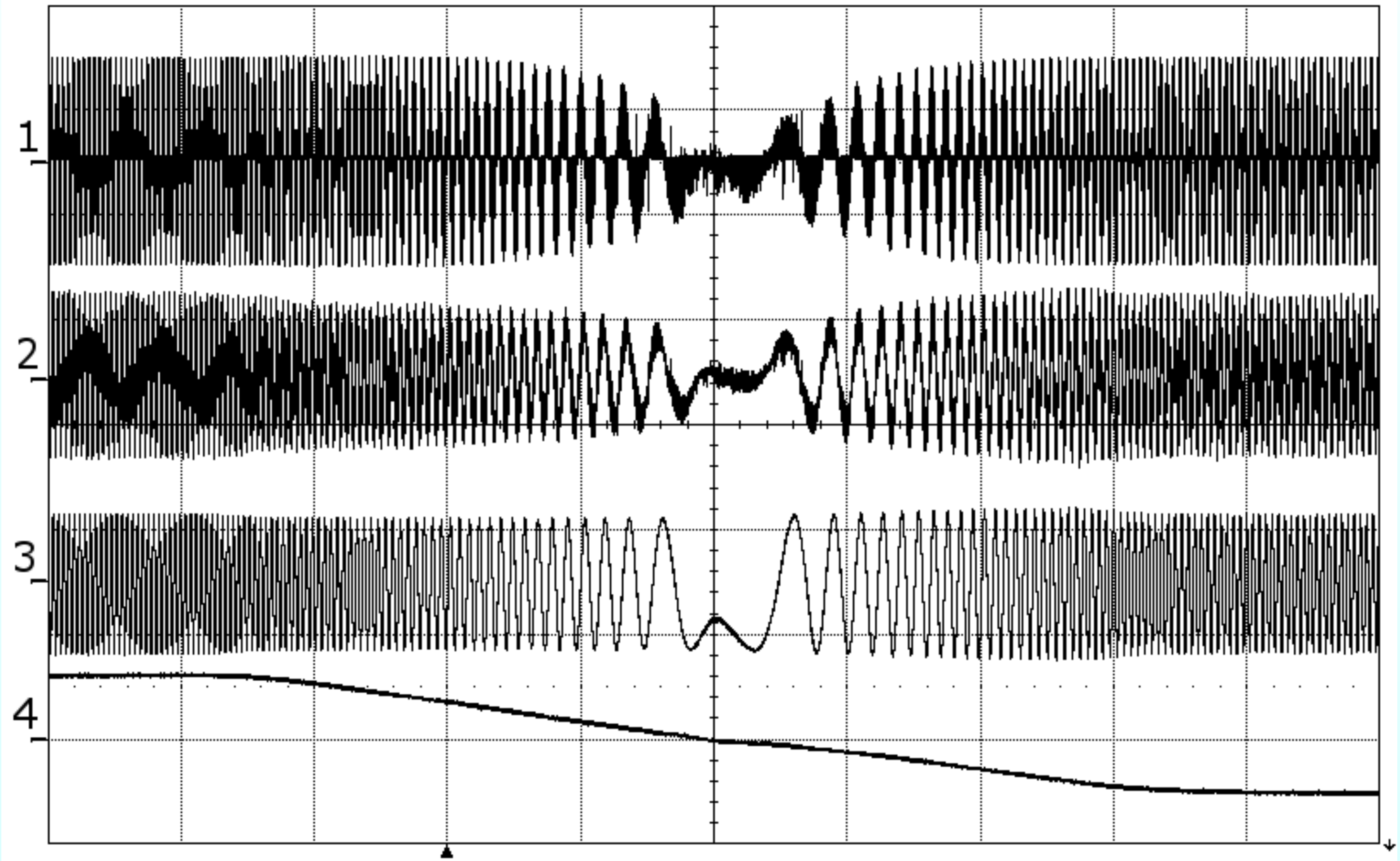

1:Phase Voltage(200V/div) and 2:Phase Current(1A/div) during transition from linear modulation to twelve-step mode (X-axis 50ms/div)

# Experimental Results




1:Phase Voltage(200V/div), 2:Phase Current(1A/div), 3:Reference Current(1A/Div) and 4:frequency(20Hz/Div) during acceleration from stand still to 20 Hz (X-axis 500ms/div)

# Experimental Results




1:Phase Voltage(200V/div), 2:Phase Current(1A/div),
3:Reference Current(1A/Div) and 4:frequency(40Hz/Div)
during speed reversal from 20Hz to -20Hz
(X-axis 1s/div)

# Conclusion

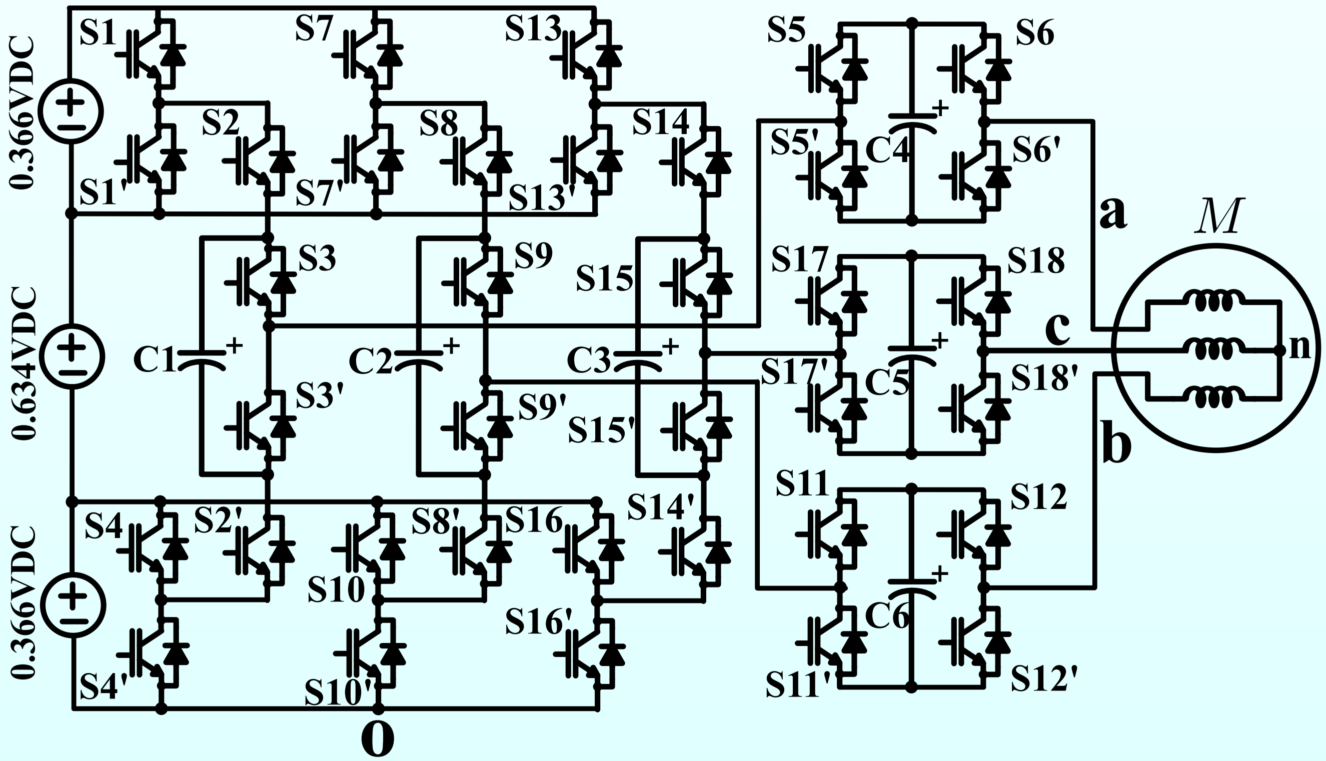
- Proposed controller has switching frequency pattern similar to that of VC-SVPWM dodecagonal inverter
- Generalized vector selection logic valid for all sectors and both direction
- All advantages of space phasor based HCC -
  - adjacent voltage vector switching,
  - excellent dynamic performance, simple control
- All advantages of dodecagonal voltage space -
  - elimination of $6(n\pm1)$, ($n$=odd) harmonics
  - extended linear modulation range

# A nearly constant switching frequency CESV based hysteresis controller for an IM drive with multilevel dodecagonal voltage space vectors

# Organization

- Power circuit and space-vector diagram
- Analysis of CESV in VC-SVPWM
- Online boundary computation
- Block diagram and flow chart of the proposed controller
- Simulation and experimental results
- Conclusion

# Power circuit for multilevel 12-sided polygons




- Six-level inverter cascaded with a floating capacitor H-bridge cell
- Capacitor C1, C2, C3 - 0.5 VDC
- Capacitor C4, C5, C6 - 0.183 VDC
- Asymmetrical nine-level inverter

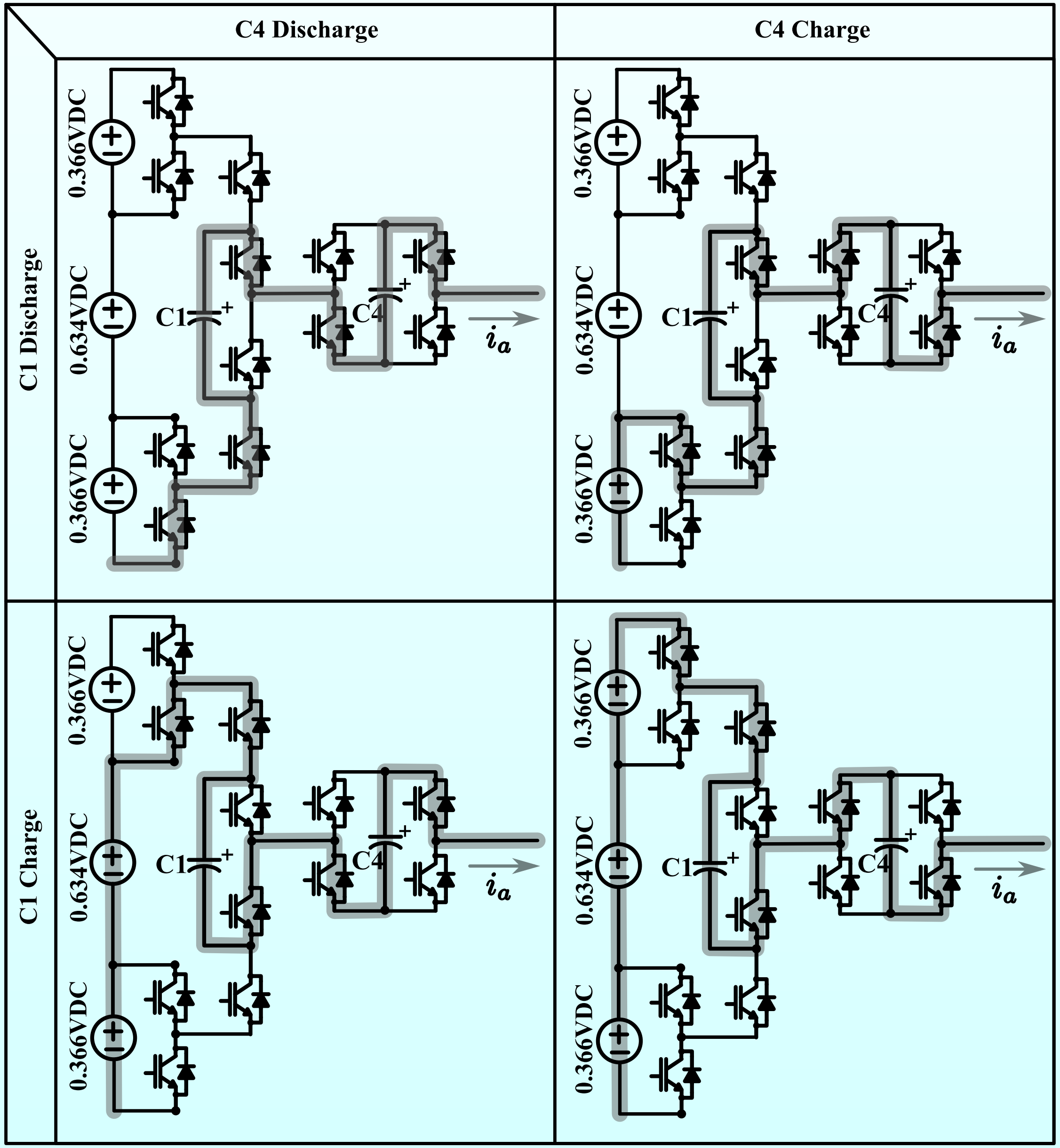
# Individual Leg Pole Voltages

- Redundant states to charge or discharge used capacitors

| Pole Voltage Levels | Method of generation | Effect on capacitors when current is positive (towards the motor terminal) | |
|---|---|---|---|
| | | C1 | C4 |
| 0.183VDC | Vc4 | No effect | Discharging |
| | 0.366VDC-Vc4 | No effect | Charging |
| 0.366VDC | 0.366VDC | No effect | No effect |
| 0.5VDC | Vc1 | Discharging | No effect |
| | VDC-Vc1 | Charging | No effect |
| 0.683VDC | Vc1+Vc4 | Discharging | Discharging |
| | 0.366VDC+Vc1-Vc4 | Discharging | Charging |
| | VDC-Vc1+Vc4 | Charging | Discharging |
| | 1.366VDC-Vc1-Vc4 | Charging | Charging |
| 0.866VDC | 0.366+Vc1 | Discharging | No effect |
| | 1.366VDC-Vc1 | Charging | No effect |
| 1VDC | VDC | No effect | No effect |
| 1.183VDC | VDC+Vc4 | No effect | Discharging |
| | 1.366VDC-Vc4 | No effect | Charging |
| 1.366VDC | 1.366VDC | No effect | No effect |
| 0 | 0 | No effect | No effect |

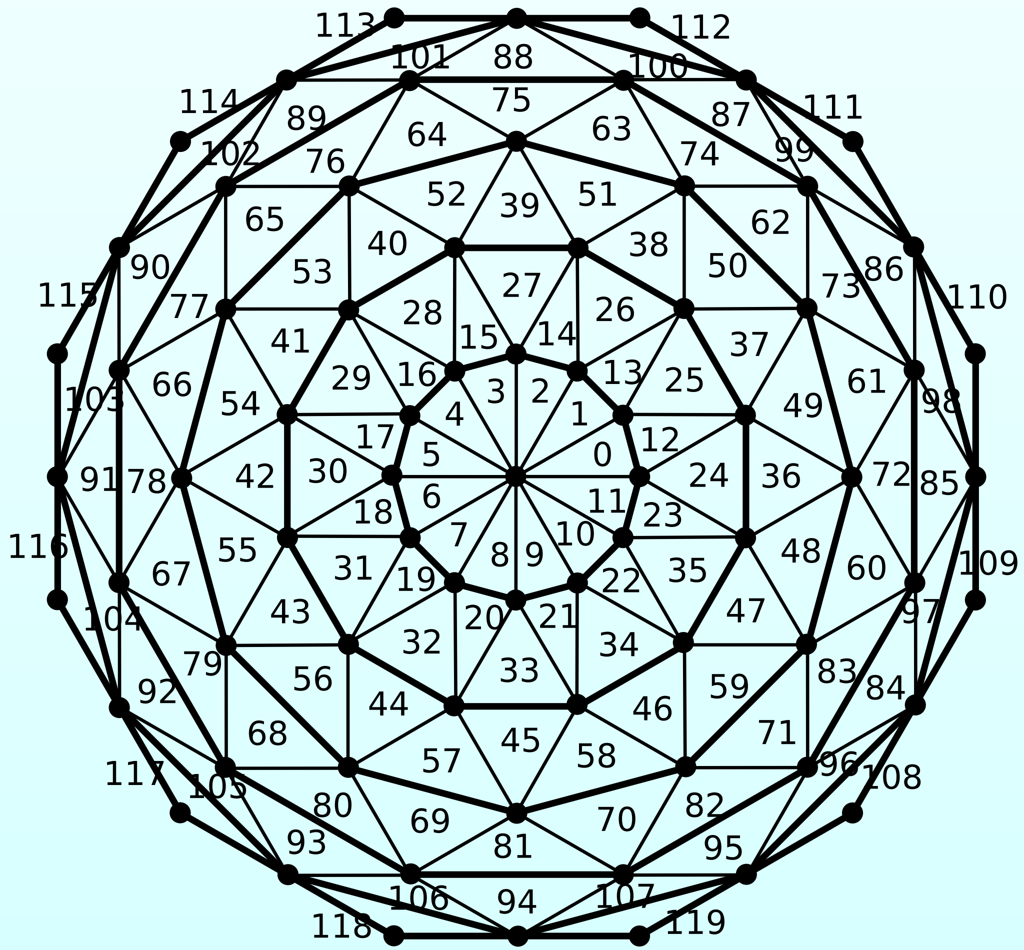
# Pole Voltages Example 0.683 VDC

- One out of four combinations chosen depending on capacitor voltages



# Multilevel dodecagonal Space Vector Diagram

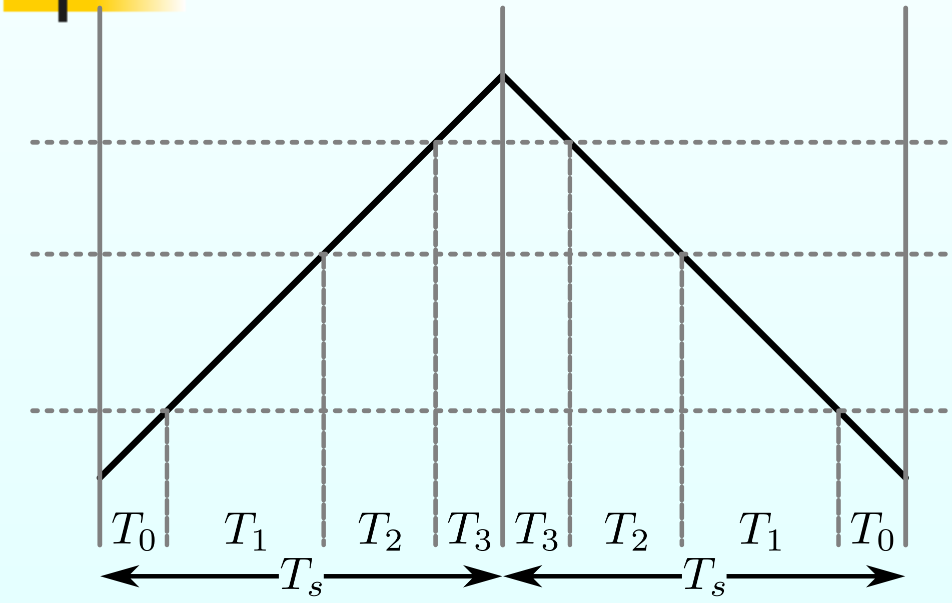
- Voltage vectors lying on dodecagon chosen
- Six 12-sided polygons
- Radius of outermost dodecagon - 1.225 VDC
- 72 voltage vectors, 120 triangles

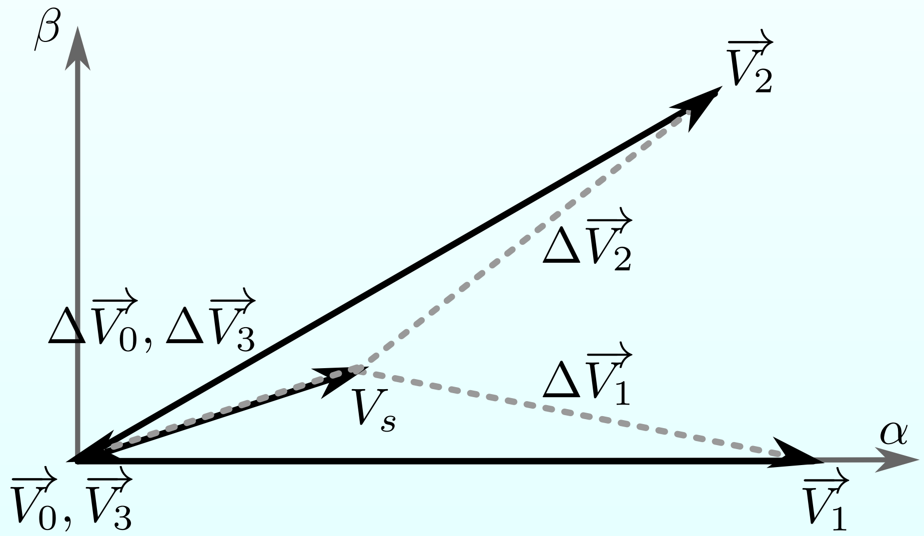


# Proposed HCC

- Analyse trajectory of constant switching frequency VC-SVPWM
- Use same trajectory as VC-SVPWM to get constant switching frequency, during steady state operation
- Identify triangle and vectors timings
- Check boundary crossing and switch appropriate vectors

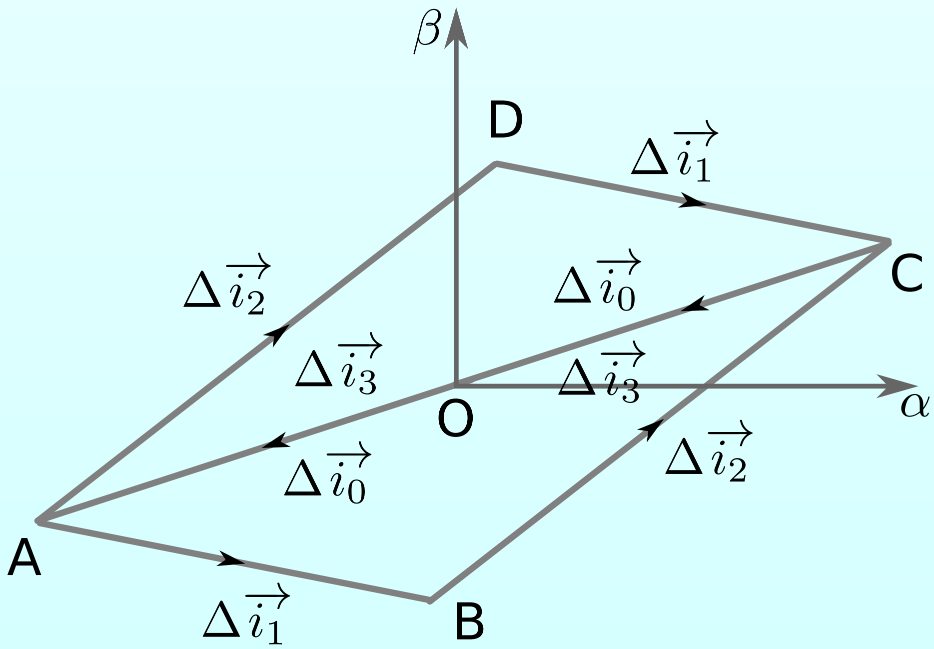
# SVPWM CESV Trajectory Analysis




- Ramp up trajectory - OABCO
- Ramp down trajectory - OADCO
- CESV trajectory of each vector:
  - Starts at end of previous vector's trajectory
  - Length given by:

$$\Delta\vec{i}_k^* = \frac{\Delta\vec{V}_k}{L_\sigma} T_k, \qquad k = 0, 1, 2, 3$$

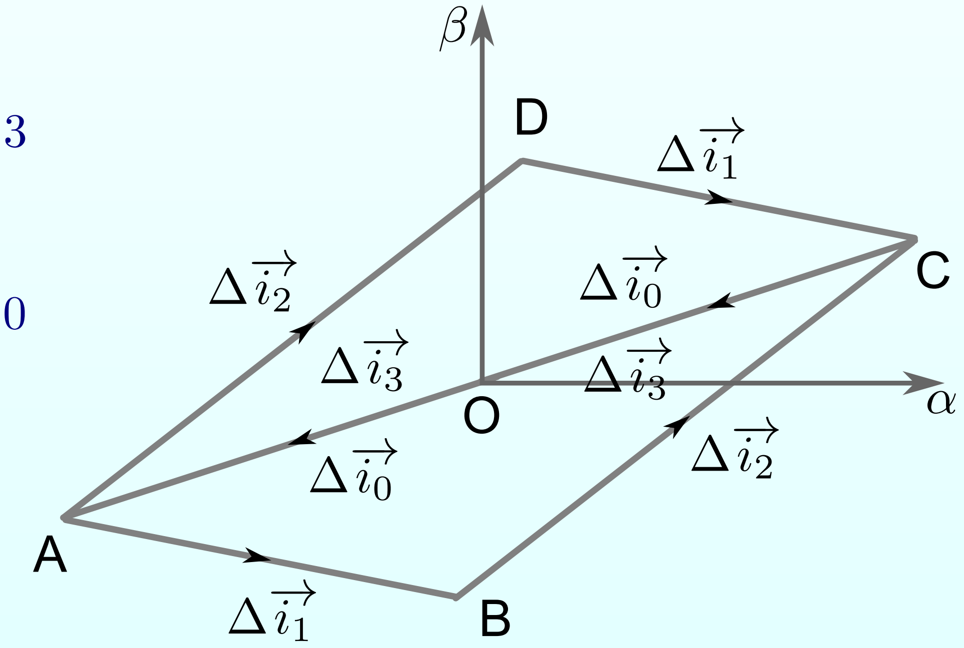


# Online Boundary Algorithm

- Determine start of trajectory

  Forward sequence: $\vec{s_k} = \sum_{j=0}^{k-1} \Delta \vec{i_j^*}, \quad k = 1, 2, 3$

  Reverse sequence: $\vec{s_k} = \sum_{j=3}^{k+1} \Delta \vec{i_j^*}, \quad k = 2, 1, 0$




- Calculate length of trajectory

$$\Delta \vec{i_k^*} = \frac{\Delta \vec{V_k}}{L_\sigma} T_k, \quad k = 0, 1, 2, 3$$

- Shift actual CESV to new origin $\Delta \vec{i_k} - \vec{s_k}$

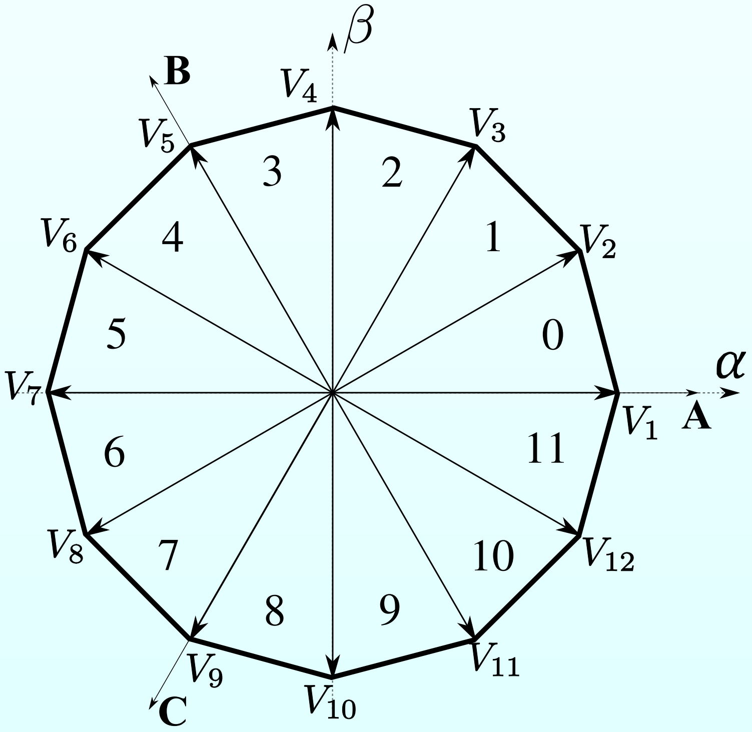
- Check projection along calculated trajectory $(\Delta \vec{i_k} - \vec{s_k}) \cdot \frac{\Delta \vec{i_k^*}}{|\Delta \vec{i_k^*}|} \geq |\Delta \vec{i_k^*}|$

  - Simplifying:

$$(\Delta \vec{i_k} - \vec{s_k}) \cdot \Delta \vec{i_k^*} \geq |\Delta \vec{i_k^*}|^2$$

$$i_x \geq i_x^*$$

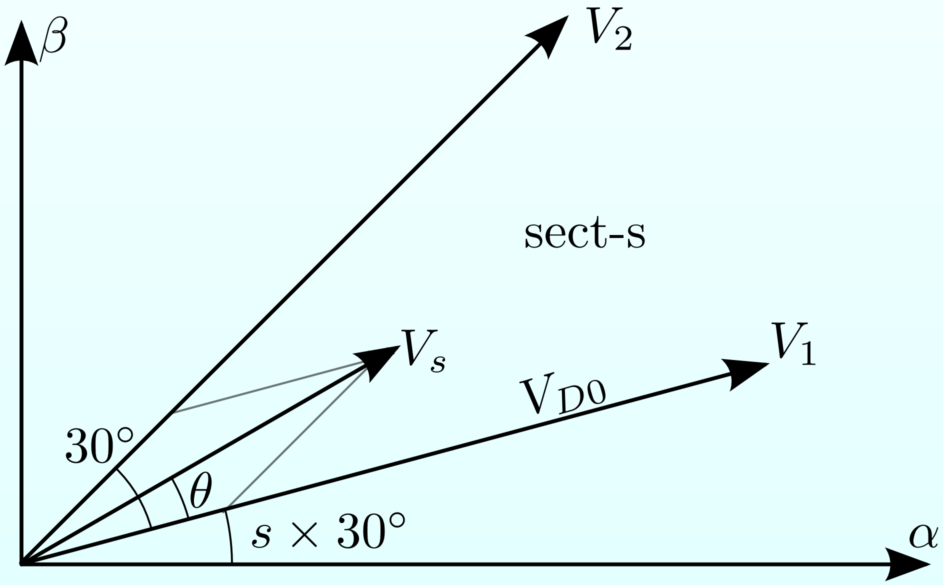
# Sector Detection Logic




| Condition | | Sector |
|---|---|---|
| $V_a > V_b > V_c$ | $V_b < 0$ | sect0 |
| | $V_b \geq 0$ | sect1 |
| $V_b > V_a > V_c$ | $V_a \geq 0$ | sect2 |
| | $V_a < 0$ | sect3 |
| $V_b > V_c > V_a$ | $V_c < 0$ | sect4 |
| | $V_c \geq 0$ | sect5 |
| $V_c > V_b > V_a$ | $V_b \geq 0$ | sect6 |
| | $V_b < 0$ | sect7 |
| $V_c > V_a > V_b$ | $V_a < 0$ | sect8 |
| | $V_a \geq 0$ | sect9 |
| $V_a > V_c > V_b$ | $V_c \geq 0$ | sect10 |
| | $V_c < 0$ | sect11 |

- Estimate $V_s$ from $V_k$, $\Delta i$, $R_s$ and $\sigma L_s$
- Transform $V_{s\alpha}$, $V_{s\beta}$ to $V_a$, $V_b$, $V_c$
- Use Table to decide sector

# Timing Caculation - 0° Dodecagonal Sector




- **Volts-sec balance of vectors in a sector 's'**

$$T_s\vec{V}_s = T_1 V_{D0}\angle(s30°) + T_2 V_{D0}\angle(s+1)30°$$

- **Solving for $T_1$ and $T_2$**

$$\begin{bmatrix} T_1 \\ T_2 \end{bmatrix} = \frac{2T_s}{V_{D0}} \begin{bmatrix} \sin\left((s+1)\,30°\right) & -\cos\left((s+1)\,30°\right) \\ -\sin\left(s30°\right) & \cos\left(s30°\right) \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix}$$

- **Simplifying in terms of sampled reference value**

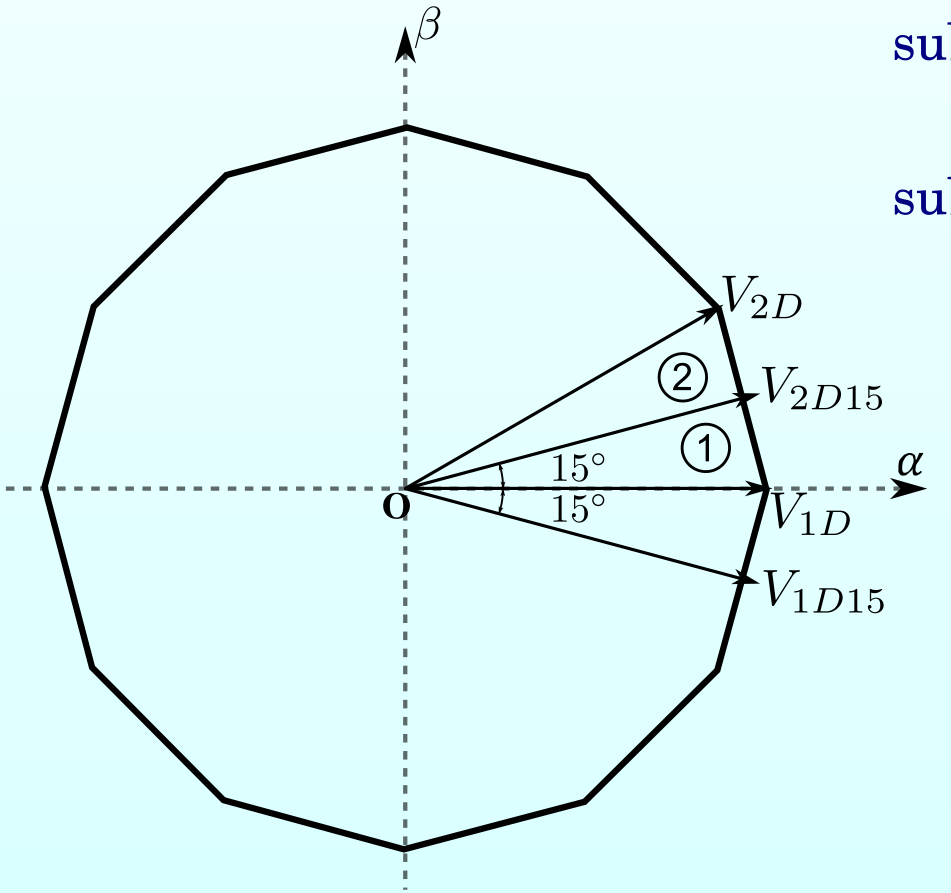
**even sectors:**

$$\begin{bmatrix} T_{1D0} \\ T_{2D0} \end{bmatrix} = \frac{T_s}{|V_{D0}|} \begin{bmatrix} 3V_{minAbs} \\ \sqrt{3}(V_{midAbs} - V_{minAbs}) \end{bmatrix}$$

**odd sectors:**

$$\begin{bmatrix} T_{1D0} \\ T_{2D0} \end{bmatrix} = \frac{T_s}{|V_{D0}|} \begin{bmatrix} \sqrt{3}(V_{midAbs} - V_{minAbs}) \\ 3V_{minAbs} \end{bmatrix}$$

# Timing Caculation - 15° Dodecagonal Sector




- Rotate both vectors by 15°

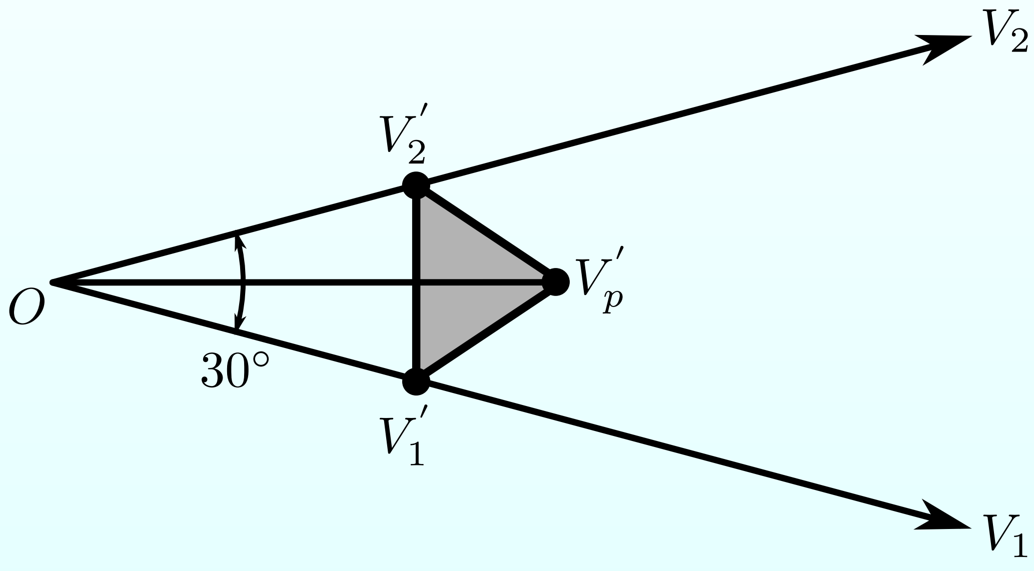
**sub-sector 1:**

$$\begin{bmatrix} T_{1D15} \\ T_{2D15} \end{bmatrix} = \begin{bmatrix} 0.5176 & -0.5176 \\ 0.5176 & \sqrt{2} \end{bmatrix} \begin{bmatrix} T_{1D0} \\ T_{2D0} \end{bmatrix}$$

**sub-sector 2:**

$$\begin{bmatrix} T_{1D15} \\ T_{2D15} \end{bmatrix} = \begin{bmatrix} \sqrt{2} & 0.5176 \\ -0.5176 & 0.5176 \end{bmatrix} \begin{bmatrix} T_{1D0} \\ T_{2D0} \end{bmatrix}$$

# Timing Caculation - General Triangle




- Solving volts-sec balance equation in terms of $V_1$ , $V_2$ , $V'_1$ , $V'_2$ , $V_p$ , $T_1$ , $T_2$

$$T_p^{'} = \frac{|V_1|(T_1 + T_2) - |V_2^{'}|T_s}{|V_p^{'}| - |V_2^{'}|\cos(15)}\cos(15)$$

$$T_1^{'} = \frac{2|V_1|T_1\cos(15) - |V_p^{'}|T_p^{'}}{2|V_1^{'}|\cos(15)}$$

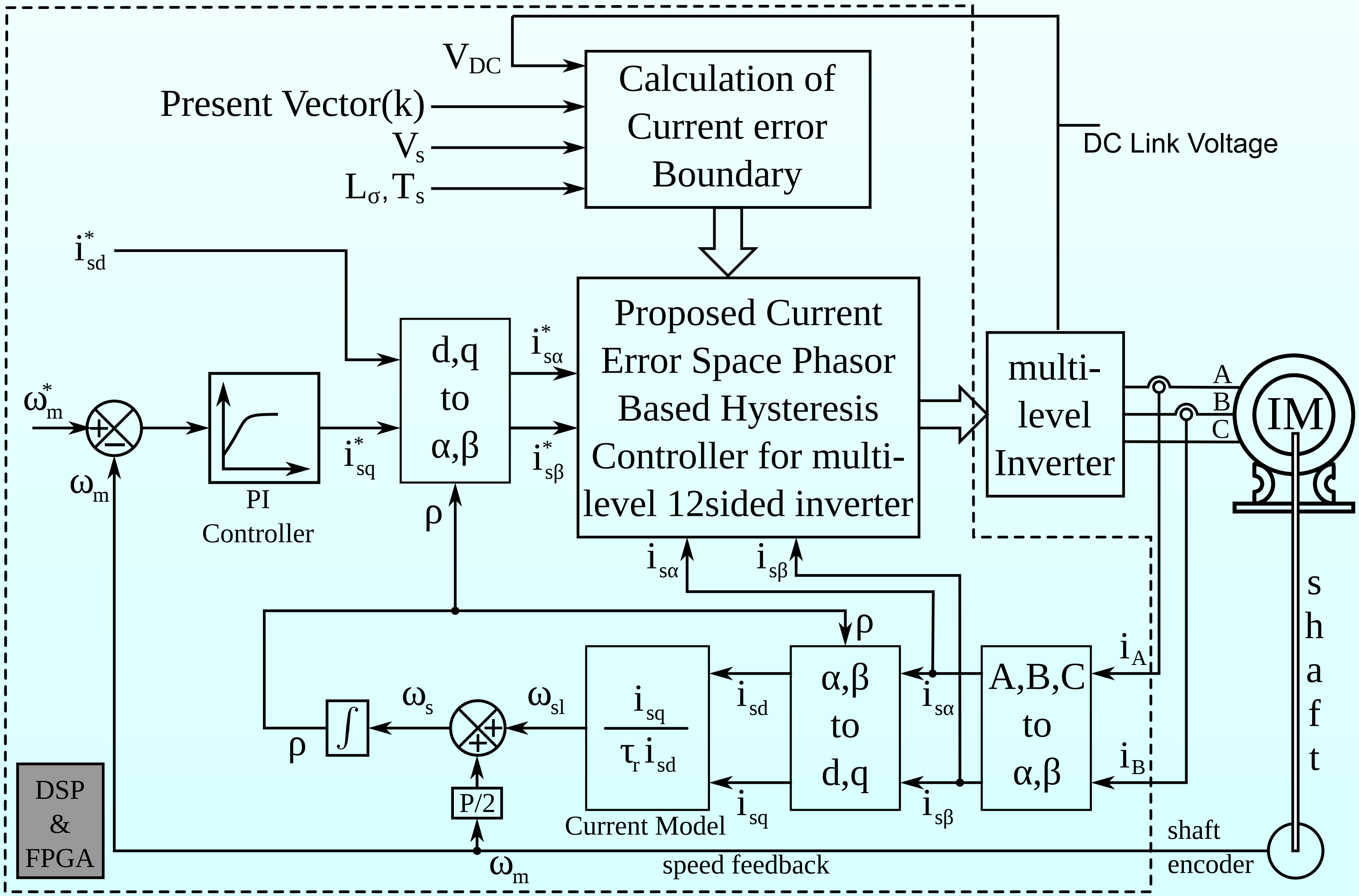
$$T_2^{'} = \frac{2|V_2|T_2\cos(15) - |V_p^{'}|T_p^{'}}{2|V_2^{'}|\cos(15)}$$

# Timing Calculation - Summary

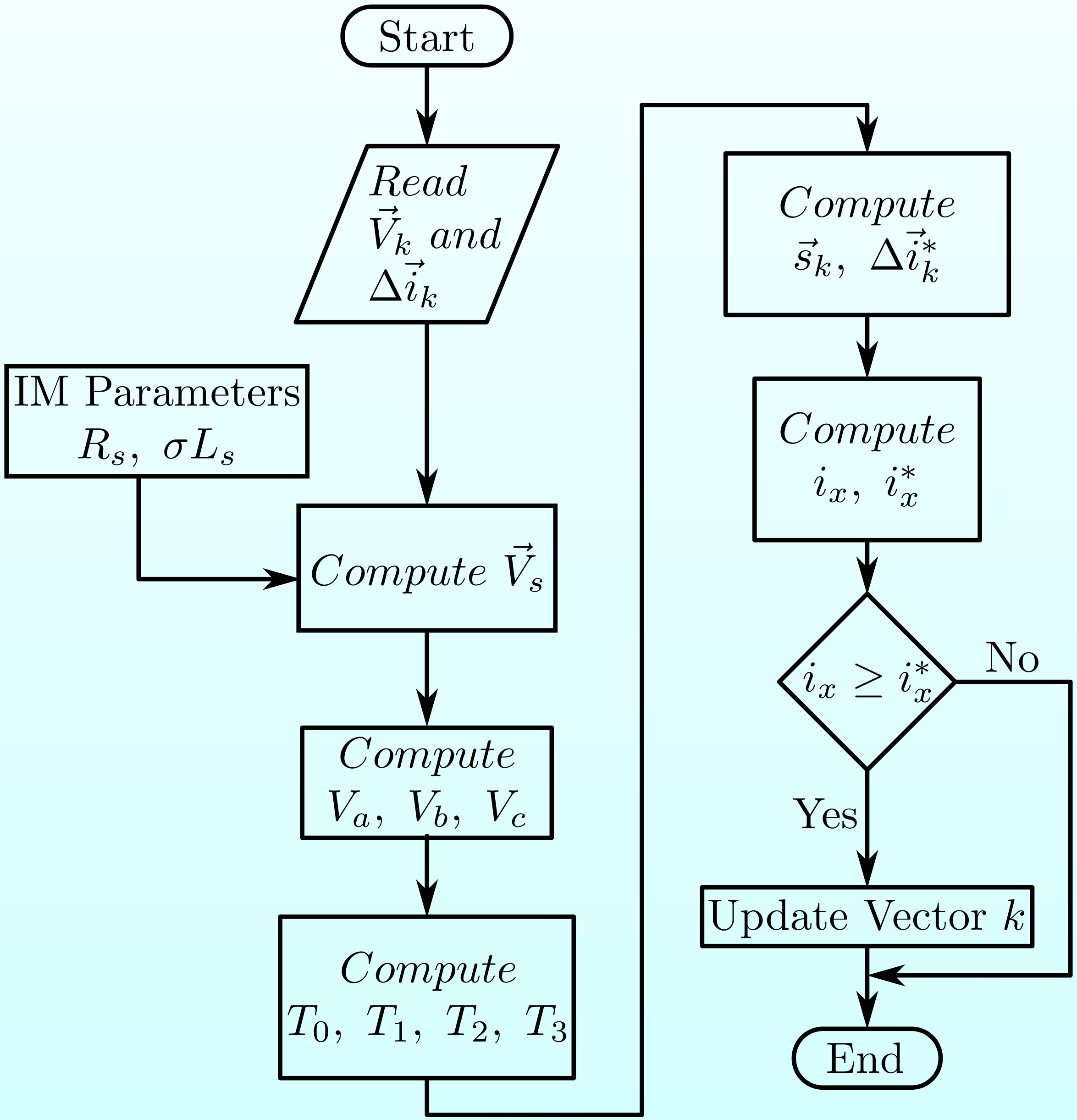
- Compute three phase reference voltages ($V_a$, $V_b$, $V_c$) from $V_s$
- Find 12-sided sector (30$^o$ sector) and its active vector dwell times
- Find sub-sector (15$^\circ$ sector) and its active vector dwell times
- Find vector dwell times of all the triangular regions inside identified sub-sector
- Find triangular region with all positive vector dwell times
- Map identified triangular region to a triangle in the space-vector diagram

# Block Diagram of the Proposed Controller

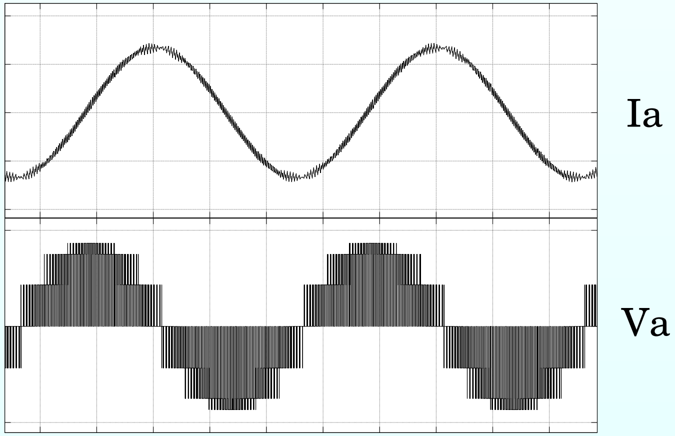
DSP → TI TMS320LF2812A



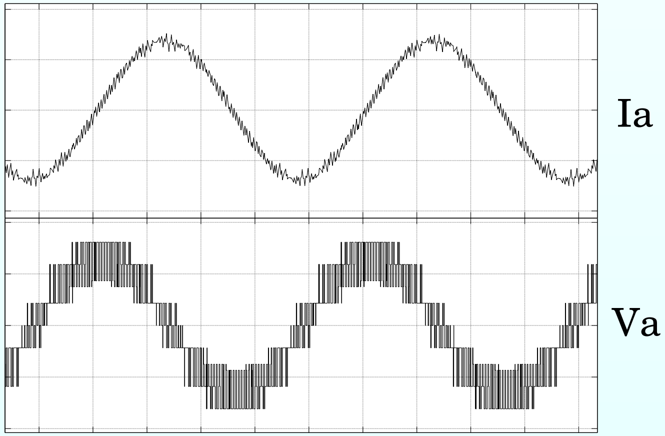
# Flow Chart of the Proposed Controller



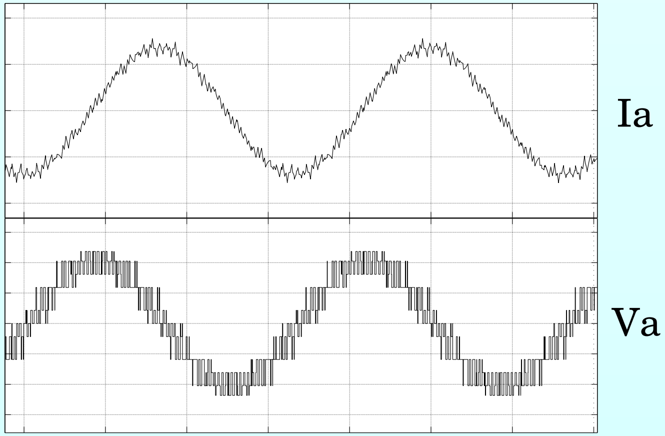
# Simulation Results - Phase Voltage & Current




10 Hz steady state, Ia (0.5 A/div), Va (50 V/div), X-axis 20 ms/div

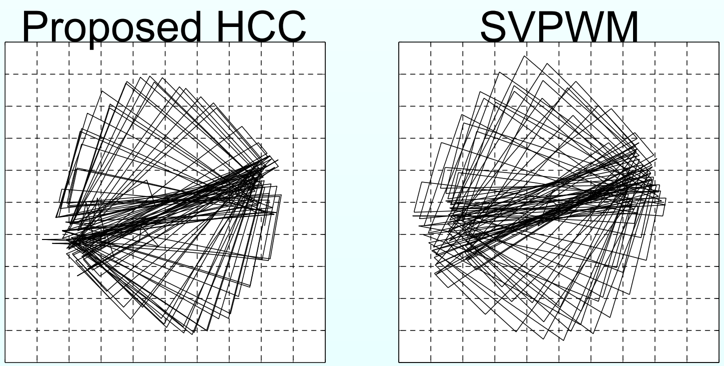



20 Hz steady state, Ia (0.5 A/div), Va (50 V/div), X-axis 10 ms/div

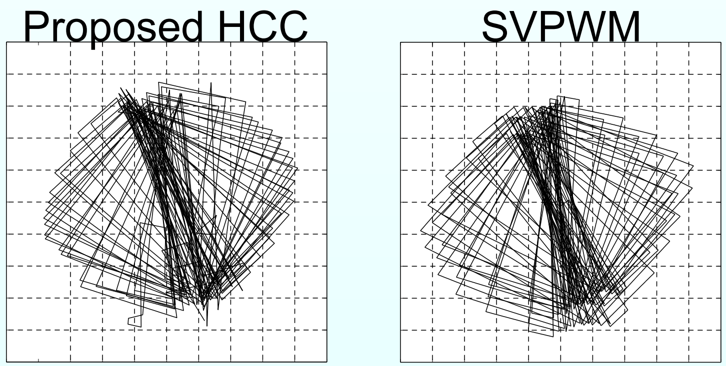



30 Hz steady state, Ia (0.5 A/div), Va (50 V/div), X-axis 10 ms/div

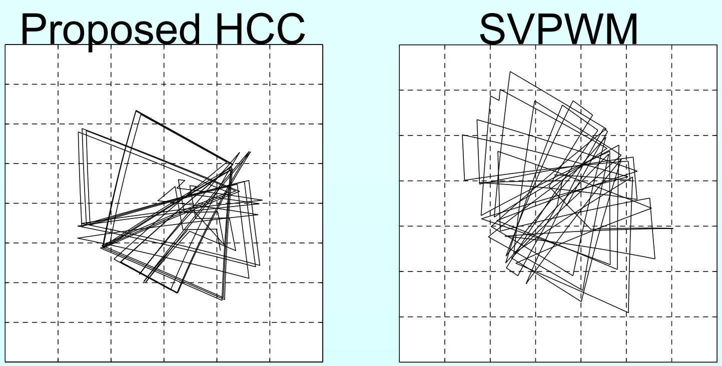
# Current Error Space Phasor




10Hz, sect 0 (X & Y Axes 20 mA/div)



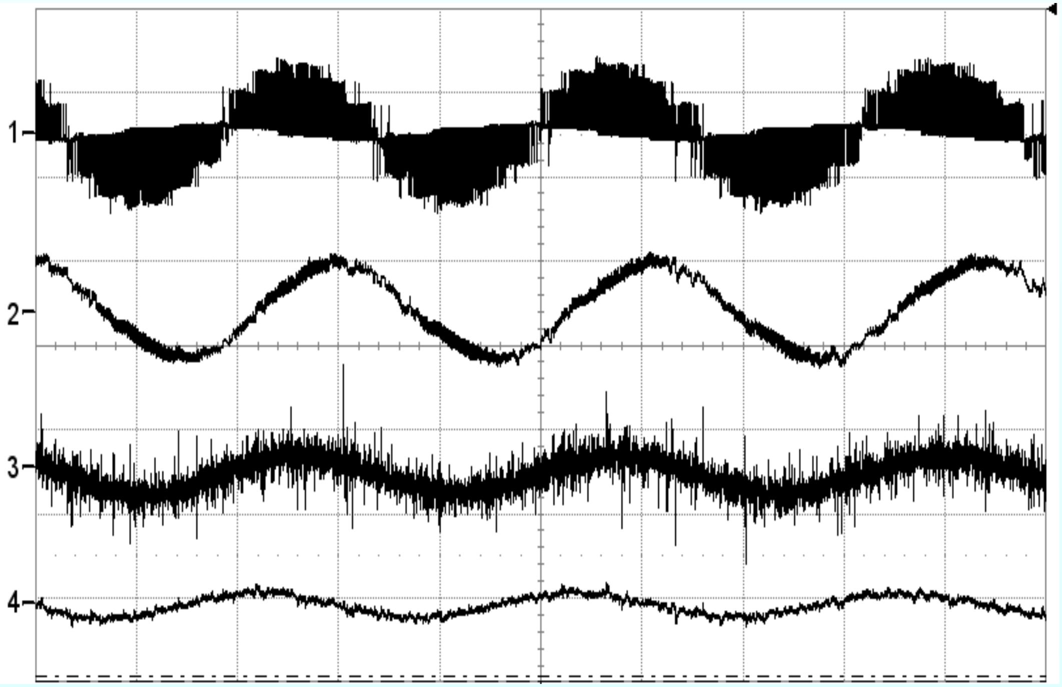

10Hz, sect 3 (X & Y Axes 20 mA/div)



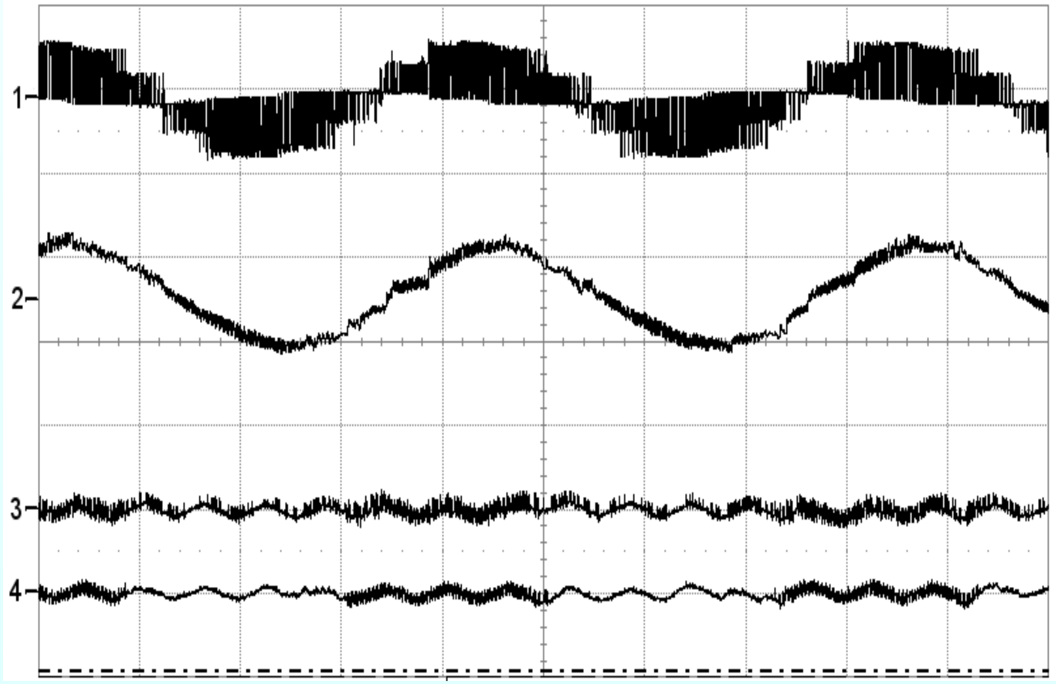

20Hz, sect 25 (X & Y Axes 5 mA/div)

# Experimental Results

Steady State waveforms @6.5 Hz




(a)

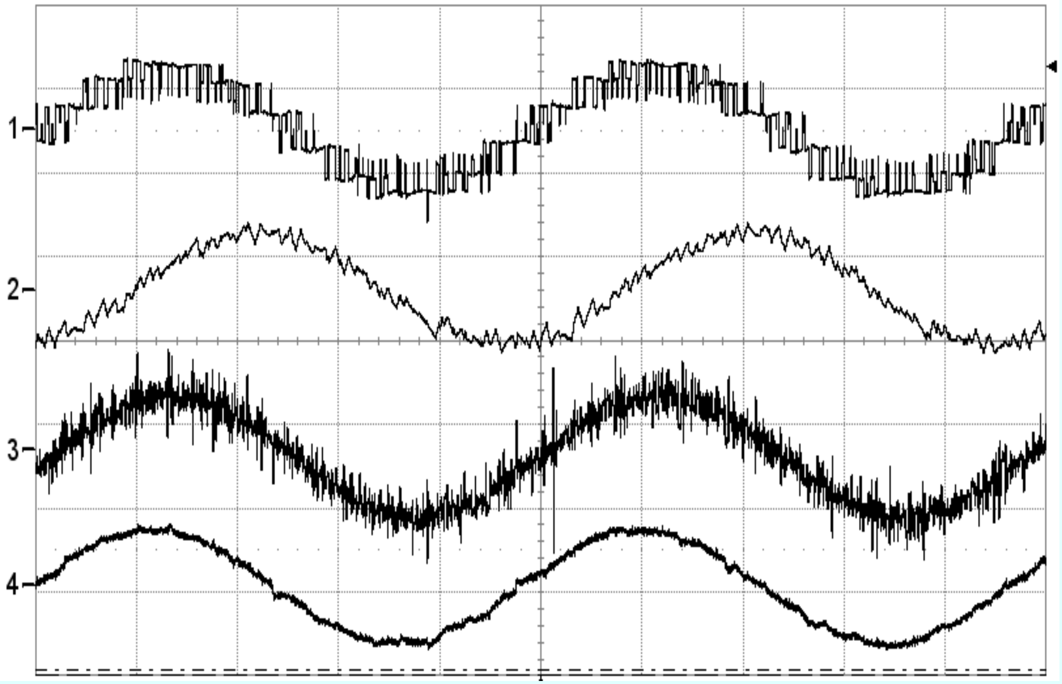



(b)

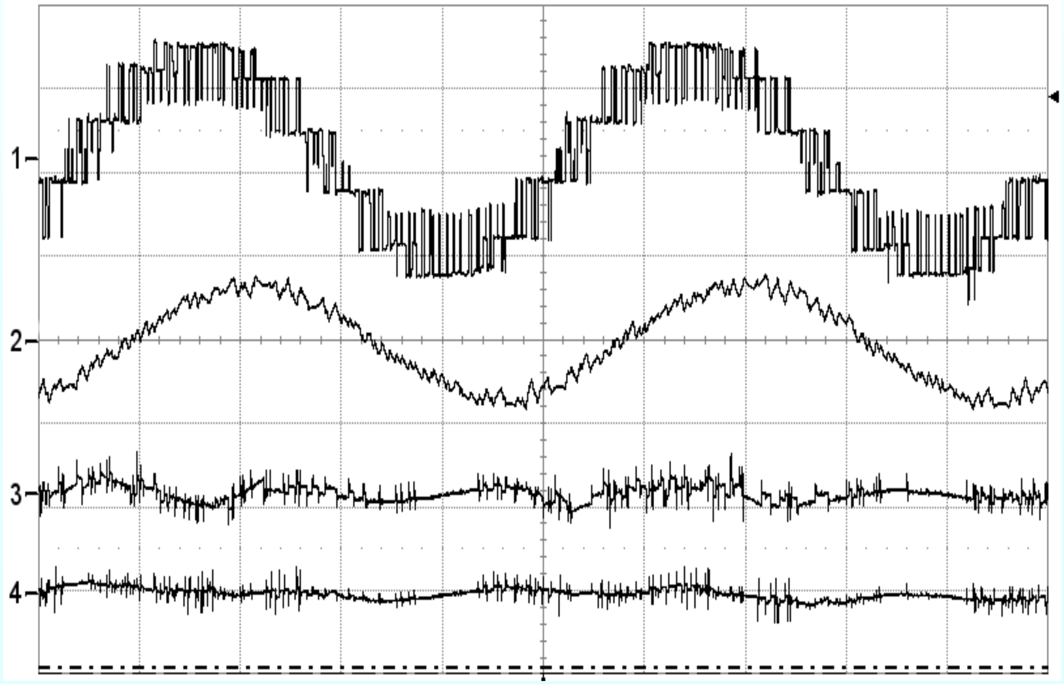
a1:Phase Voltage (50 V/div), a2:Phase Current (0.5 A/div),
a3:Estimated Stator Voltage (50 V/Div) and a4:Filtered estimated voltage (50 V/Div);
b1:Phase Voltage (100 V/div), b2:Phase Current (0.5 A/div),
b3:Capacitor Voltage C1 (5 V/div) and b4:Capacitor Voltage C4 (2 V/Div)
(X-axis 50 ms/div)

# Experimental Results

Steady State waveforms @20 Hz




(a)

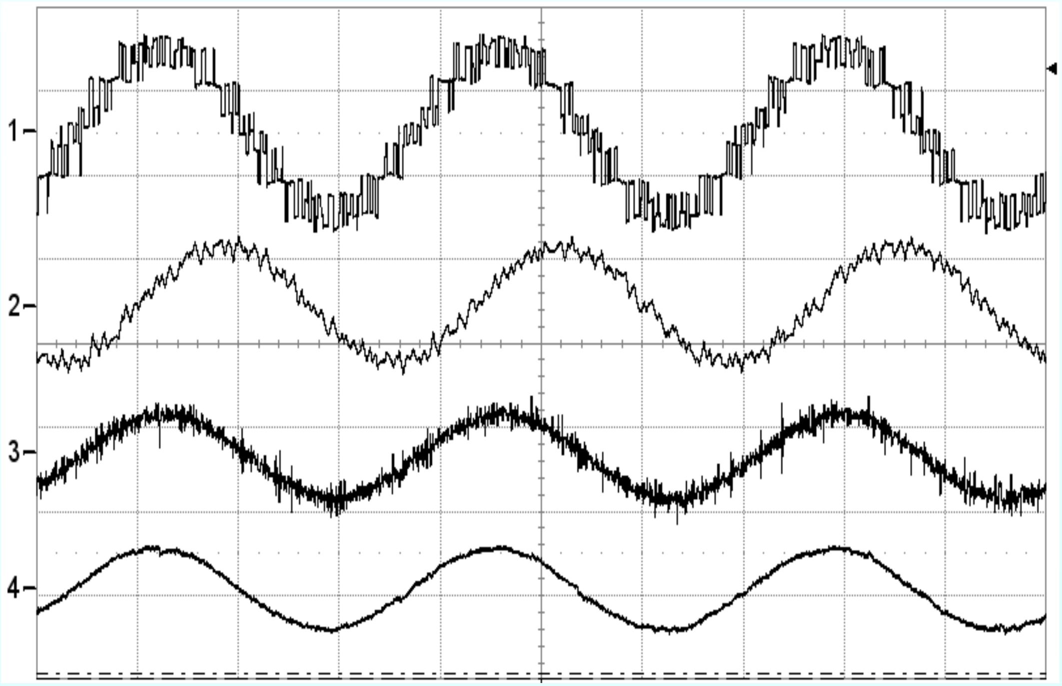



(b)

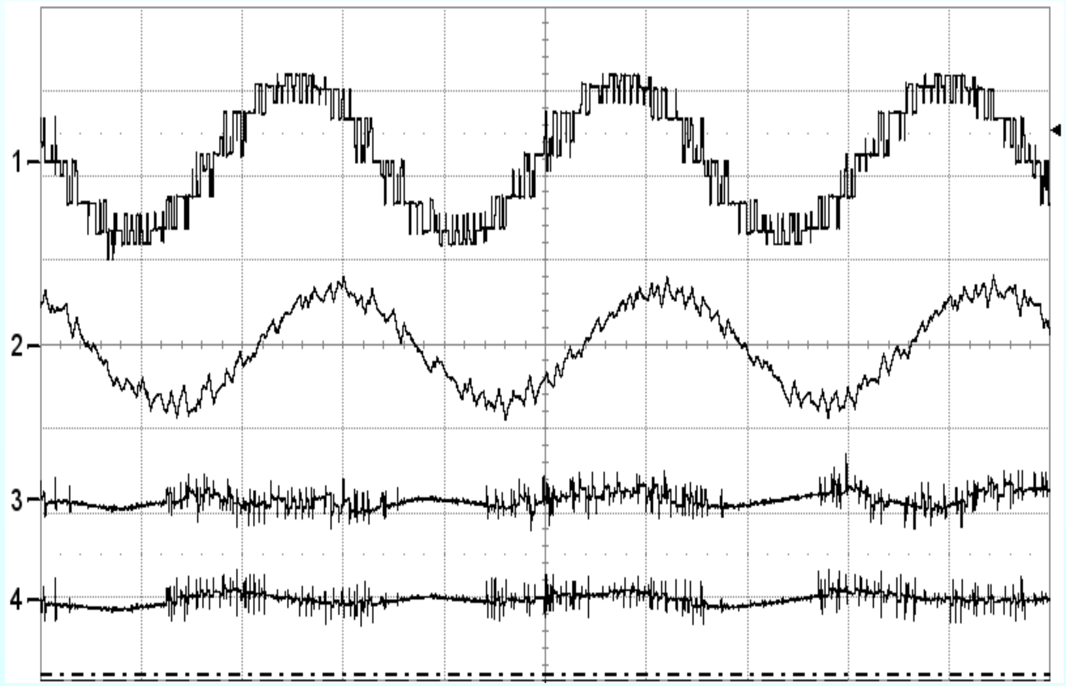
a1:Phase Voltage (100 V/div), a2:Phase Current (0.5 A/div),
a3:Estimated Stator Voltage (50 V/Div) and a4:Filtered estimated voltage (50 V/Div);
b1:Phase Voltage (100 V/div), b2:Phase Current (0.5 A/div),
b3:Capacitor Voltage C1 (5 V/div) and b4:Capacitor Voltage C4 (2 V/Div)
(X-axis 10 ms/div)

# Experimental Results

Steady State waveforms @30 Hz




(a)

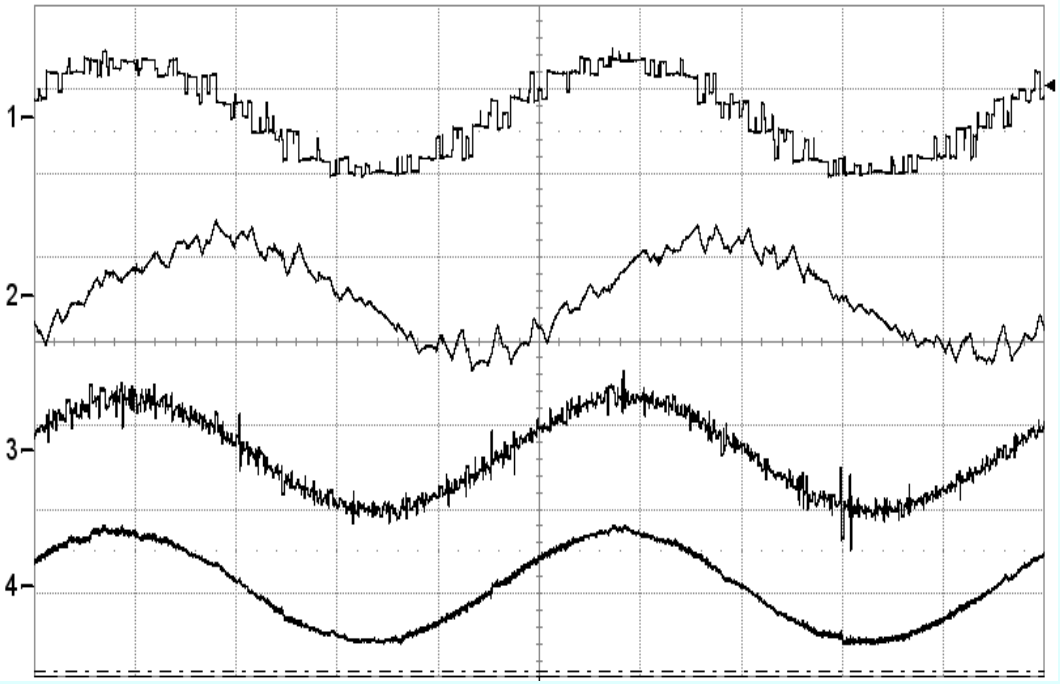



(b)

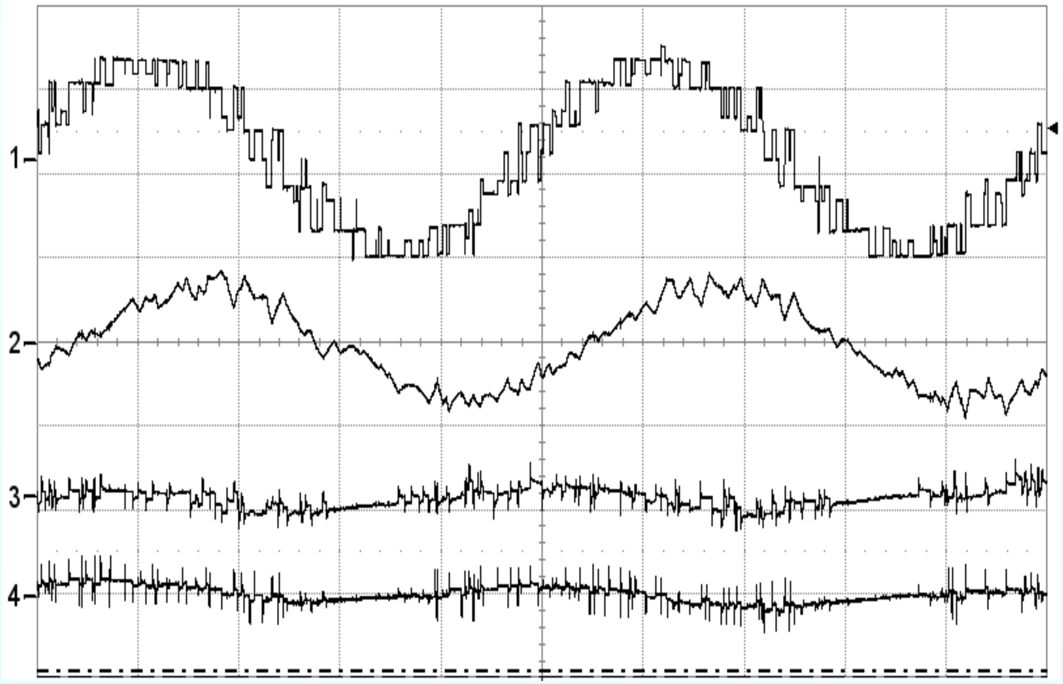
a1:Phase Voltage (100 V/div), a2:Phase Current (0.5 A/div),
a3:Estimated Stator Voltage (100 V/Div) and a4:Filtered estimated voltage (100 V/Div);
b1:Phase Voltage (200 V/div), b2:Phase Current (0.5 A/div),
b3:Capacitor Voltage C1 (5 V/div) and b4:Capacitor Voltage C4 (2 V/Div)
(X-axis 10 ms/div)

# Experimental Results

Steady State waveforms @40Hz




(a)

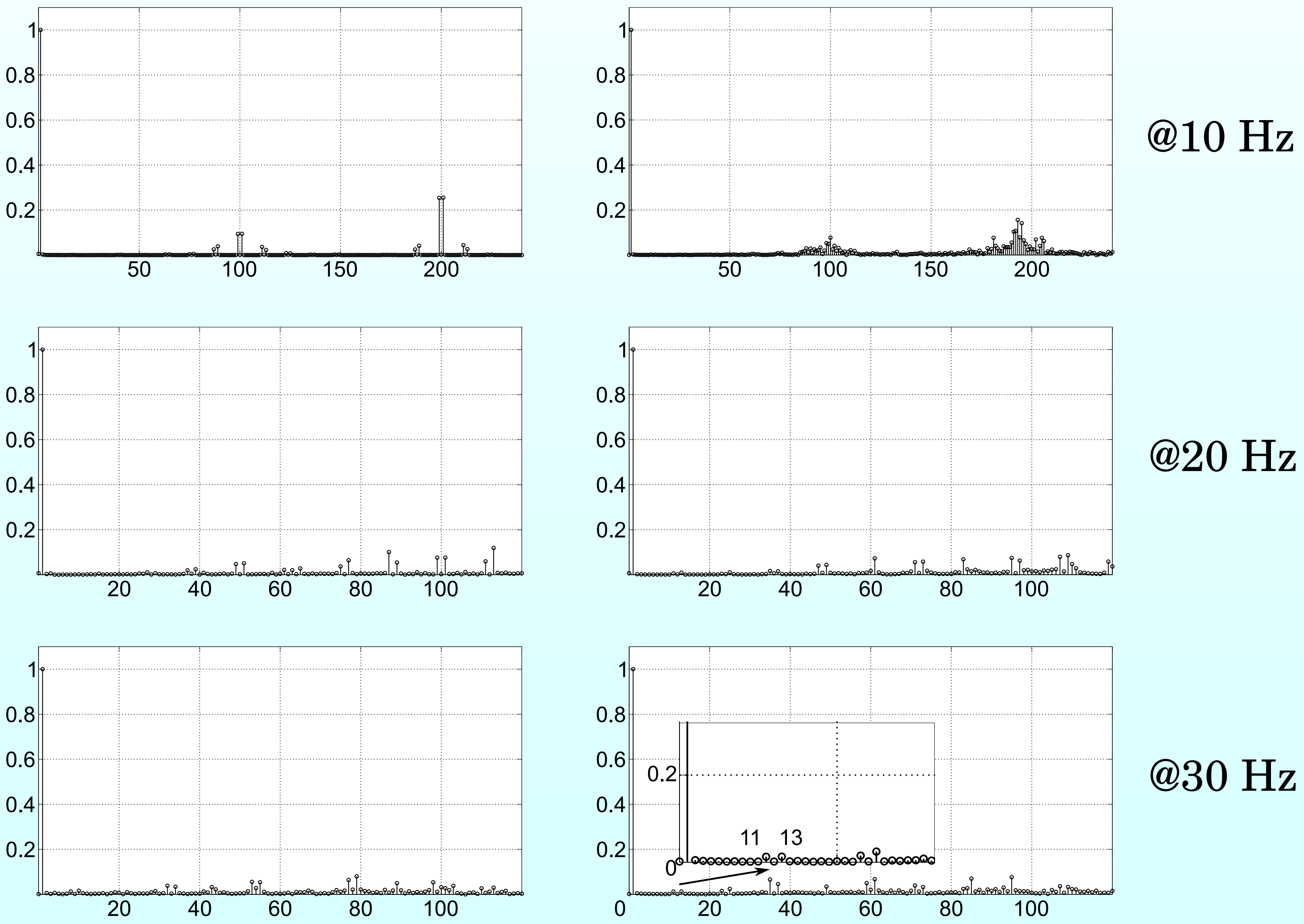



(b)

a1:Phase Voltage (200 V/div), a2:Phase Current (0.5 A/div),
a3:Estimated Stator Voltage (100 V/Div) and a4:Filtered estimated voltage (100 V/Div);
b1:Phase Voltage (200 V/div), a2:Phase Current (0.5 A/div),
b3:Capacitor Voltage C1 (5 V/div) and b4:Capacitor Voltage C4 (2 V/Div)
(X-axis 5 ms/div)

# FFT of phase Voltage

Normalized Harmonic Spectrum (FFT) of phase Voltage

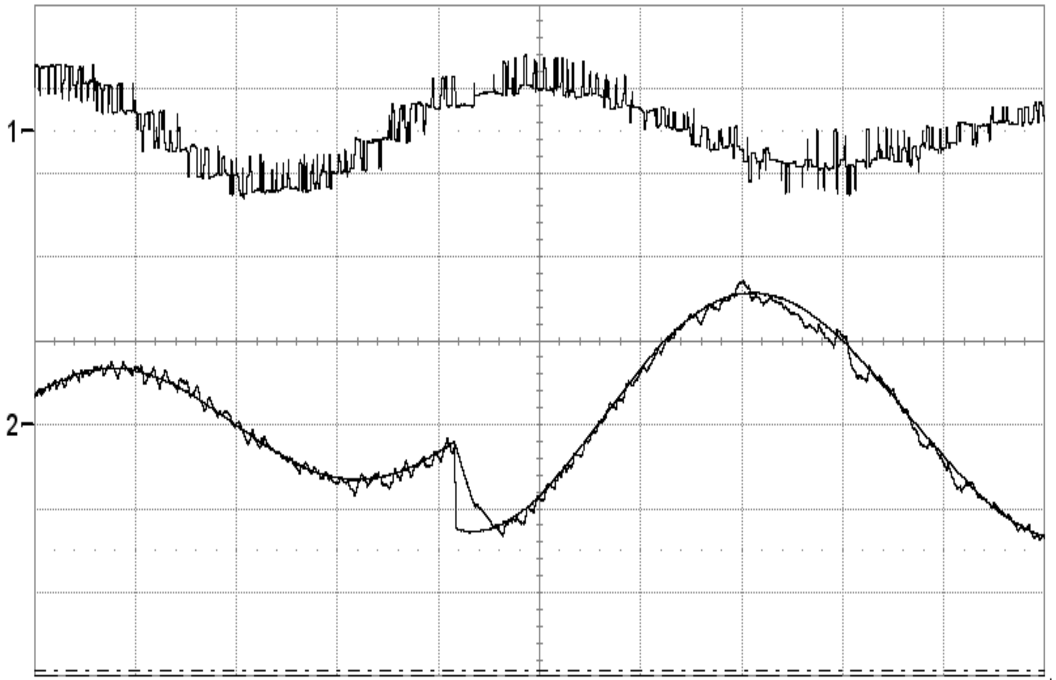



VC-SVPWM

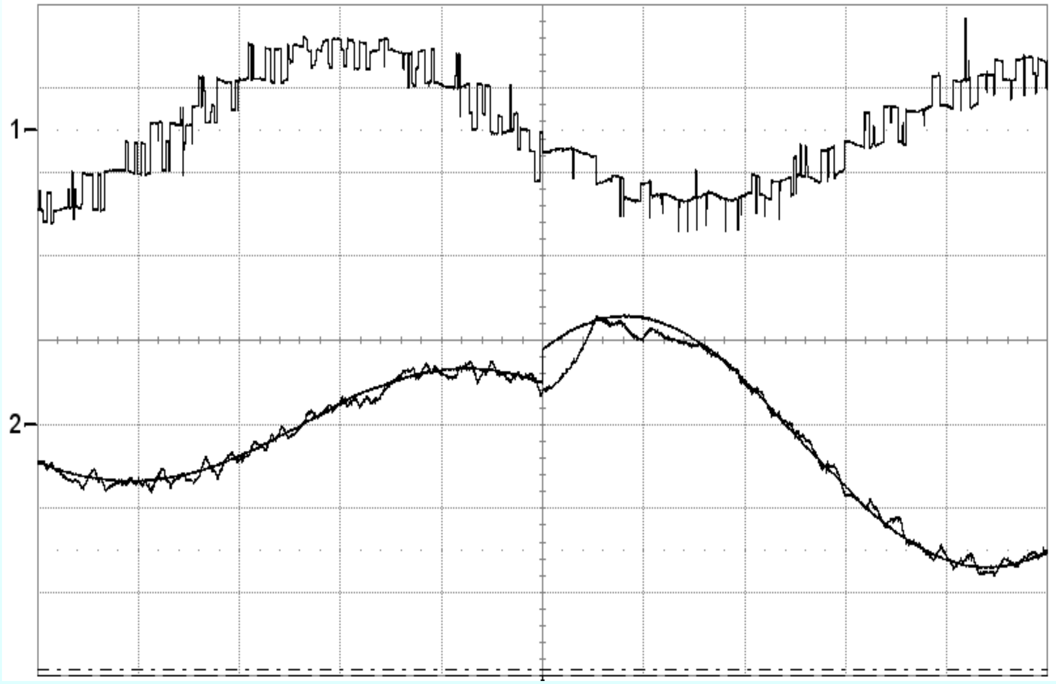
Proposed Controller

# Transient Experimental Results

Proposed Hysteresis Controller characteristics when a sudden change in Isq* is applied




(a)

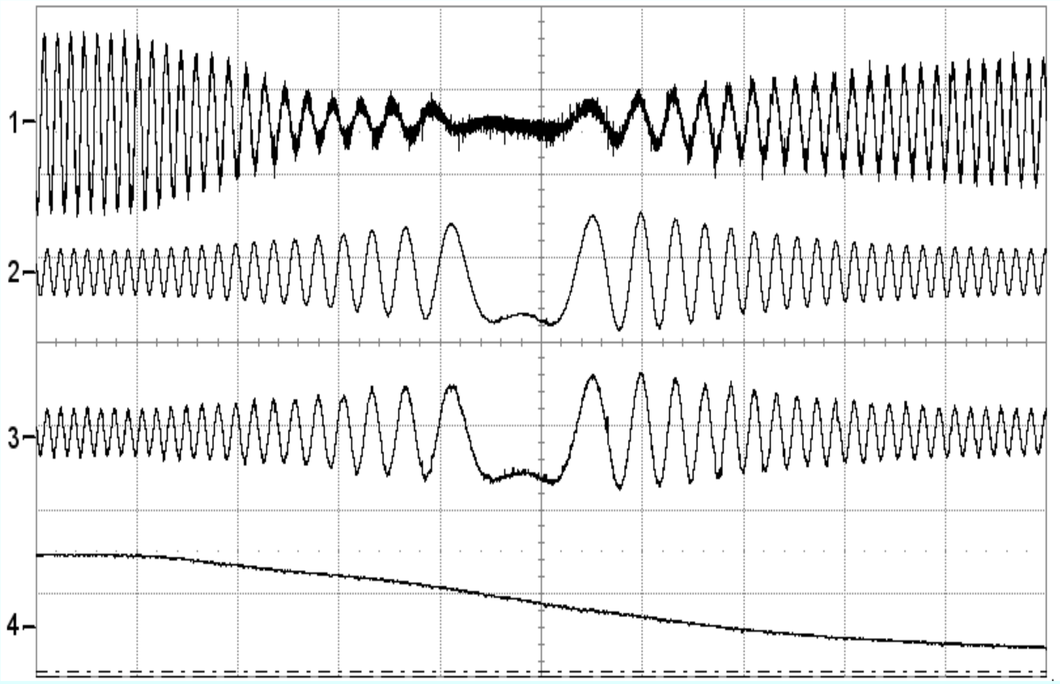



(b)

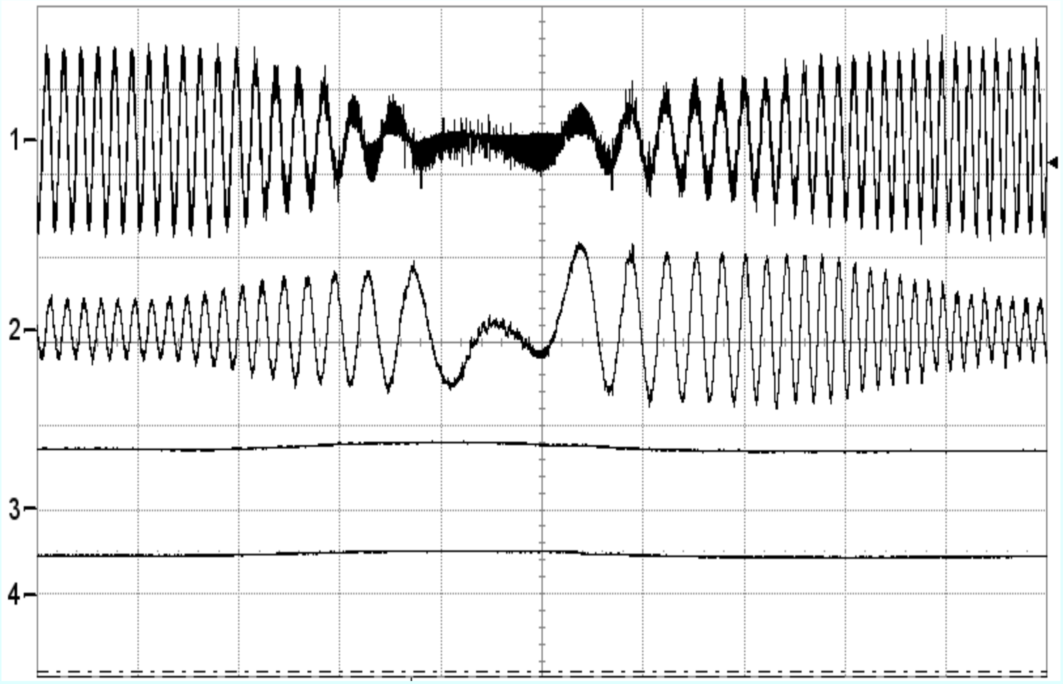
a1:Phase Voltage (100 V/div), a2:Reference and Actual Phase Currents (0.5 A/div) when 3 A isq step is applied at 20 Hz (X-axis 20 ms/div)
b1:Phase Voltage (100 V/div), b2:Reference and Actual Phase Currents (0.5 tA/div) when 3 A isq step is applied at 30 Hz (X-axis 5 ms/div)

# Transient Experimental Results

Speed reversal from 30 Hz to -30 Hz




(a)




(b)

a1:Phase Voltage (100 V/div), a2:Reference Phase Current (1 A/div),
a3:Actual Phase Current (1 A/div) and a4:frequency (50 Hz/div) (X-axis 500 ms/div)
b1:Phase Voltage (100 V/div), b2:Phase Current (1 A/div),
b3:Capacitor Voltage C4 (20 V/Div) and b4:Capacitor Voltage C1 (50 V/Div)
(X-axis 200 ms/div)

# Conclusion

- Current hysteresis controller for multilevel dodecagonal voltage space vector VSI fed IM drive
- Proposed controller has steady state switching frequency pattern similar to that of VC-SVPWM multilevel dodecagonal inverter
- All advantages of space phasor based HCC -
  - adjacent voltage vector switching,
  - excellent dynamic performance, simple control
- All advantages of multilevel dodecagonal voltage space -
  - elimination of $6(n\pm1)$, ($n$=odd) harmonics
  - extended linear modulation range
  - reduced dv/dt stress and EMI problems

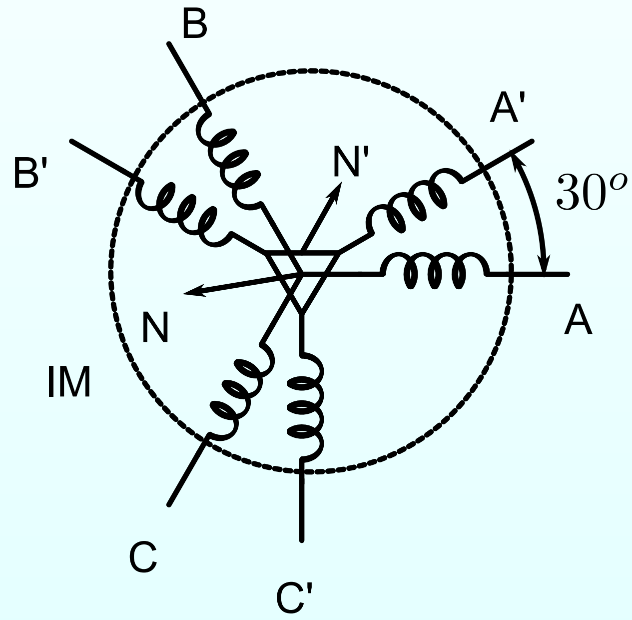
# A 5th and 7th Order Harmonic Suppression Scheme for Open-end Winding Split-phase IM Drive Using Capacitor-fed Inverters

# Organization

- Split-phase (asymmetrical six-phase) motors
- Two-level VSI fed split-phase IM
- Space vector decomposition
- Harmonic suppression
- Proposed Scheme
- Simulation and Experimental Results
- Conclusion

# Split-phase Induction Motors

- phase belt of 3-phase IM split into two halves with 30° electrical separation

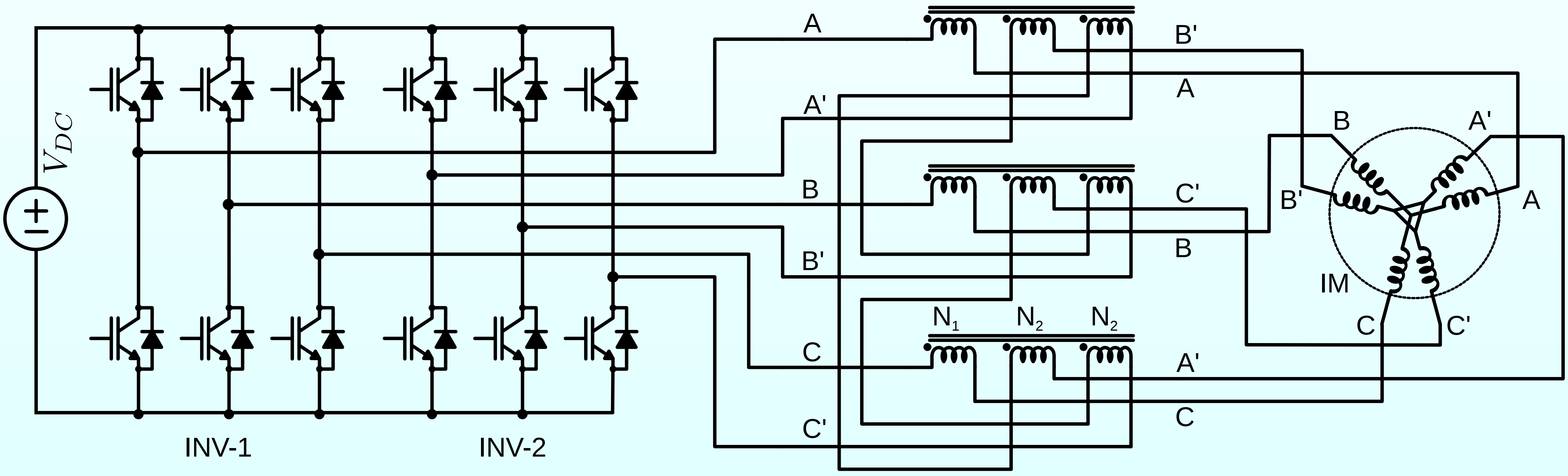



- Advantages
  - 5th and 7th order harmonics completely eliminated from flux and rotor currents
  - Reduced DC-link requirement
  - Improved Reliability
- Disadvantages
  - large 5th and 7th order harmonic currents in the stator windings

# Existing Harmonic Suppression Schemes

- Carrier-based PWM
  - Poor DC bus utlization
- Inductive filters
  - Bulky and costly
- Special PWM technique using four active vectors instead of two in SVPWM
  - High switching frequency and complex computations
- Specially designed motors - increase leakage inductance
  - Custom motor designs are expensive

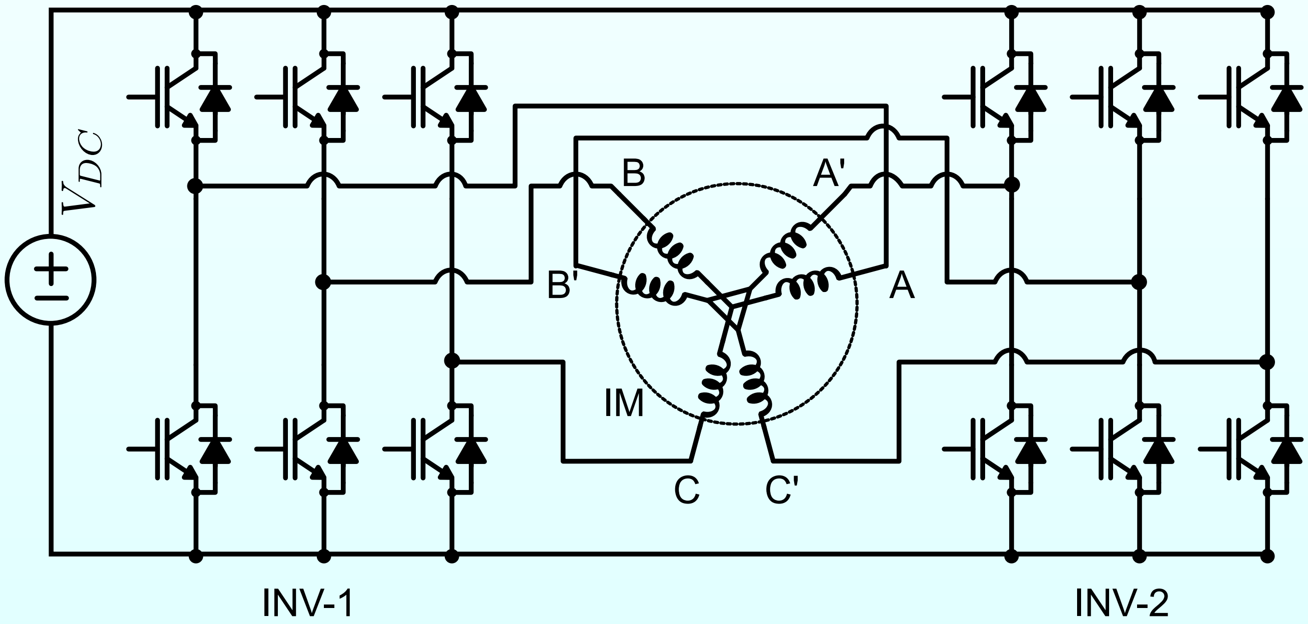
# Harmonic Suppression using Inductive Filters



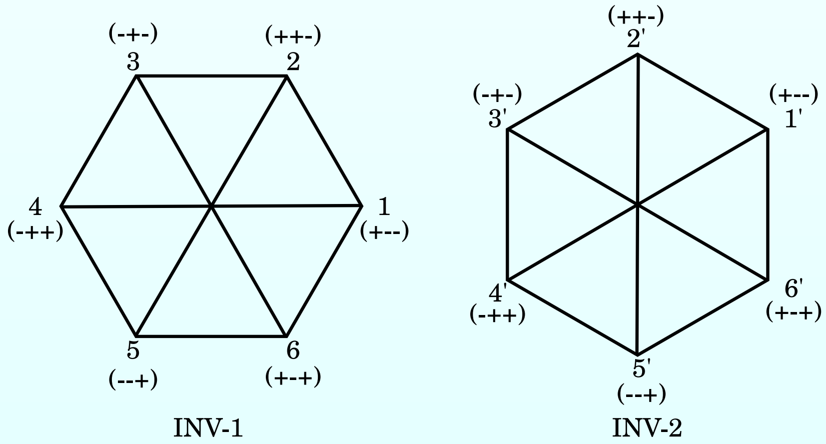

Split-phase IM fed from VSI, with inductive filters

- Three transformers, nine windings
- Bulky and costly

# VSI fed Split-phase Induction Motor



Split-phase IM fed from VSI



Voltage space vectors of the individual inverters.

- Two 2-level inverters
- Switching state vectors in six-dimensional vector space

# Space Vector Orthogonal Decomposition

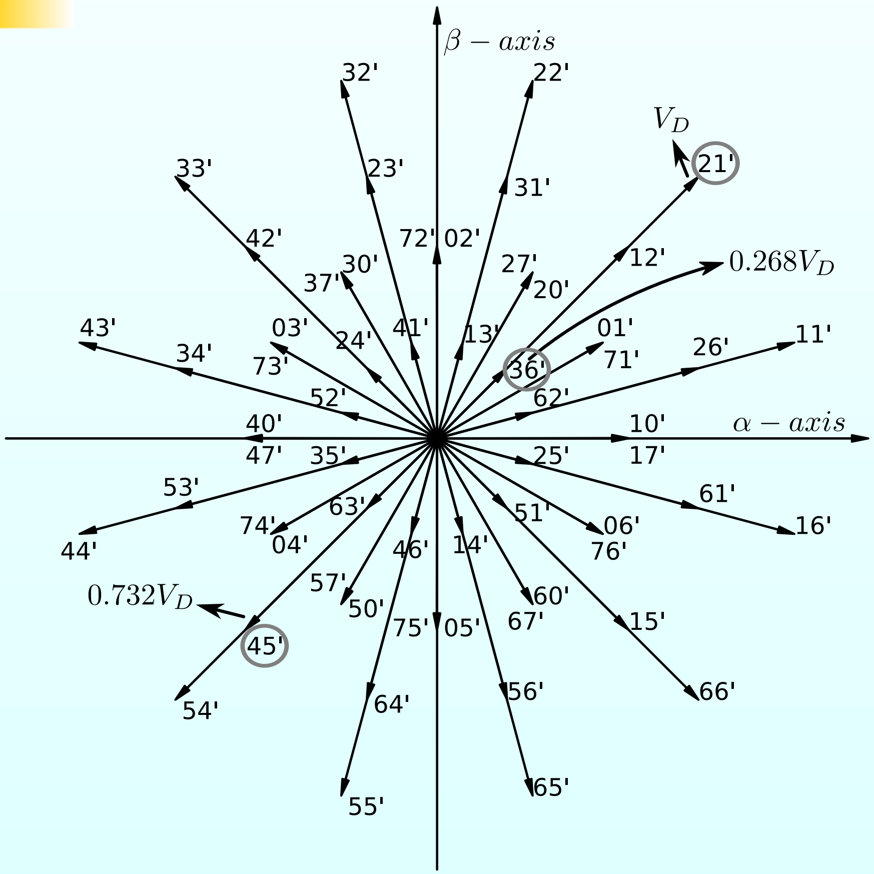
- Transform to three mutually orthogonal subspaces

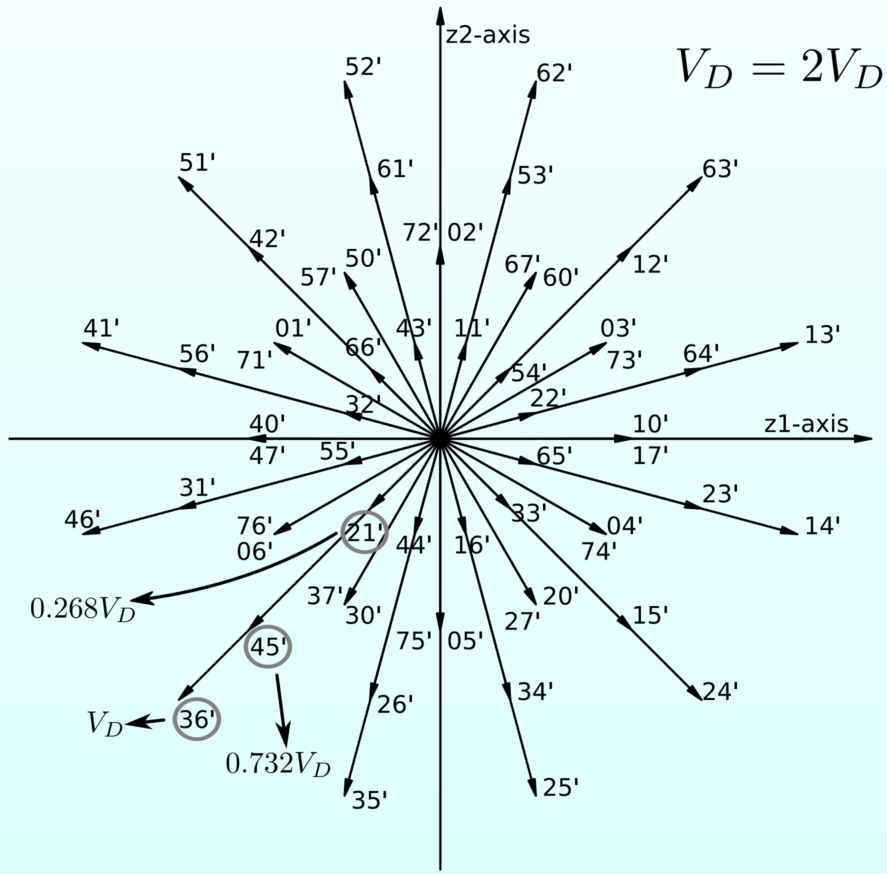
$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_{z1} \\ V_{z2} \\ V_{o1} \\ V_{o2} \end{bmatrix} = \begin{bmatrix} 1 & \cos 4\theta & \cos 8\theta & \cos\theta & \cos 5\theta & \cos 9\theta \\ 0 & \sin 4\theta & \sin 8\theta & \sin\theta & \sin 5\theta & \sin 9\theta \\ 1 & \cos 8\theta & \cos 4\theta & \cos 5\theta & \cos\theta & \cos 9\theta \\ 0 & \sin 8\theta & \sin 4\theta & \sin 5\theta & \sin\theta & \sin 9\theta \\ 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \\ V_{A'} \\ V_{B'} \\ V_{C'} \end{bmatrix}$$

- α-β sub-space : fundamental and harmonics of order k = 12m ± 1 (m = 1, 2, · · · )
  - contribute to the electromechanical energy conversion
- z1-z2 subspace: harmonics of order k = 6m ± 1 (m = 1, 3, 5, · · · )
  - no contribution to the rotating air-gap flux; new zero sequence
- o1-o2 subspace: triple-n order harmonics
  - conventional zero sequence components

# Space Vector Locations

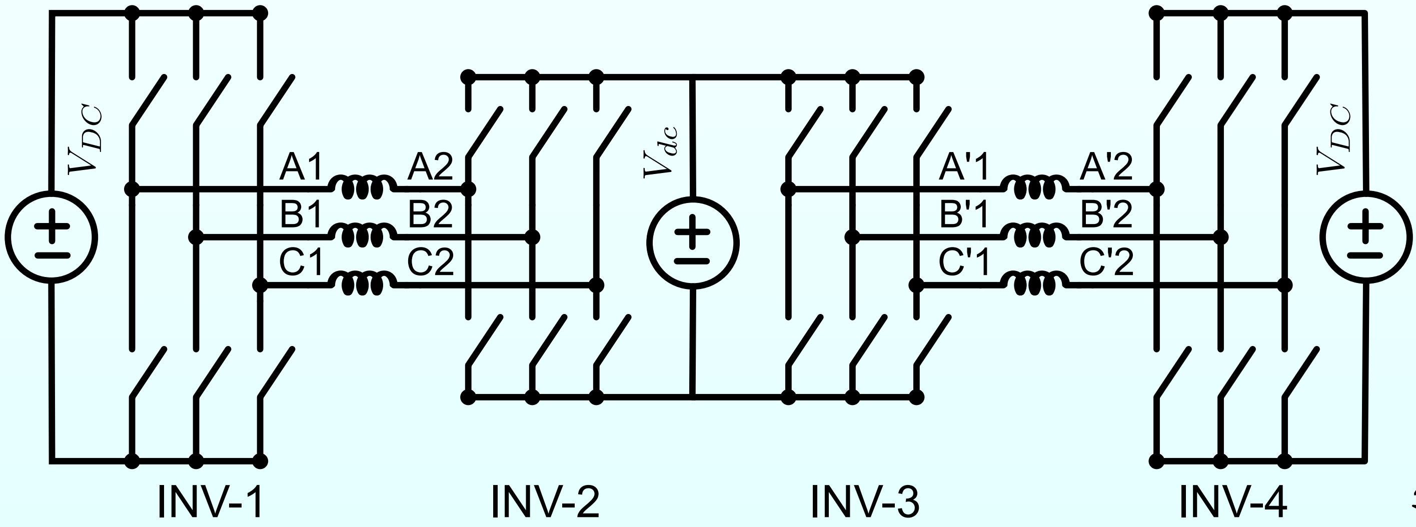
$V_D = 2V_{DC} cos15^o$



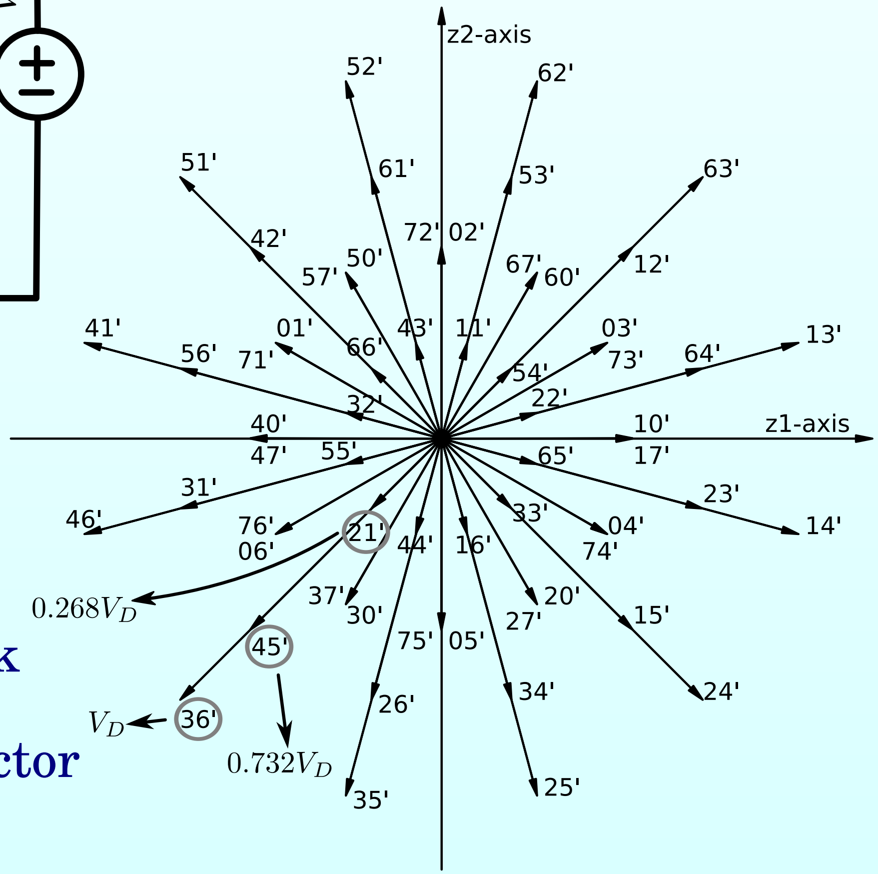




- vector locations represented as combination of individual three-phase inverters
  - e.g: vector 21' : vector 2 from INV-1 and vector 1' from INV-2
- SVPWM uses vectors lying on the outermost 12-sided polygon in α-β subspace
  - significant projection in z1-z2 subspace

# Suppressing 5$^{th}$ and 7$^{th}$ Order Harmonics




Open-end winding split-phase IM fed
with asymmetrical DC links

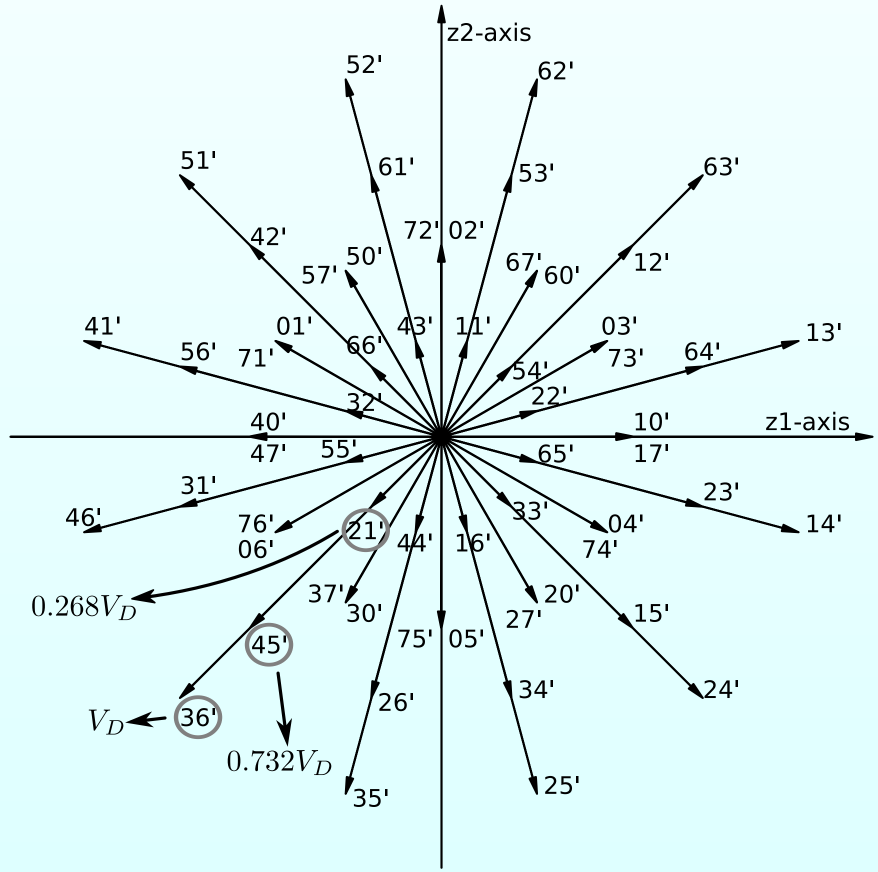



z1-z2 plane

- Feed from open end side with asymmetrical DC-link
- Two possible vectors lying on same side as main vector
  - e.g: vector 21' : vectors 45' and 36'
- Requires DC-link scaling

# Suppressing 5$^{th}$ and 7$^{th}$ Order Harmonics Contd...

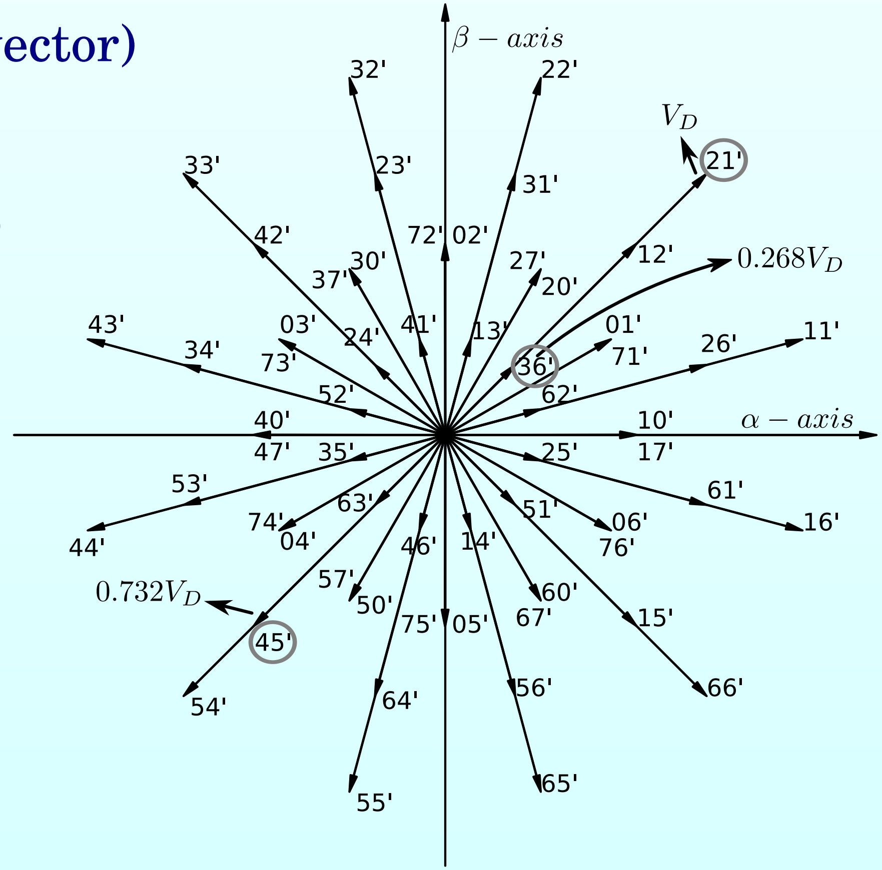
- Projection on z1-z2 plane for same DC-link
  - main vector 21' = 0.268 $V_D$
  - secondary vector 45' = 0.732 $V_D$
  - secondary vector 36' = 1 $V_D$
- DC-link Scaling
  - secondary vector 45' $\rightarrow$ 0.268/0.732 = 0.366
  - secondary vector 36' $\rightarrow$ 0.268/1 = 0.268




z1-z2 plane

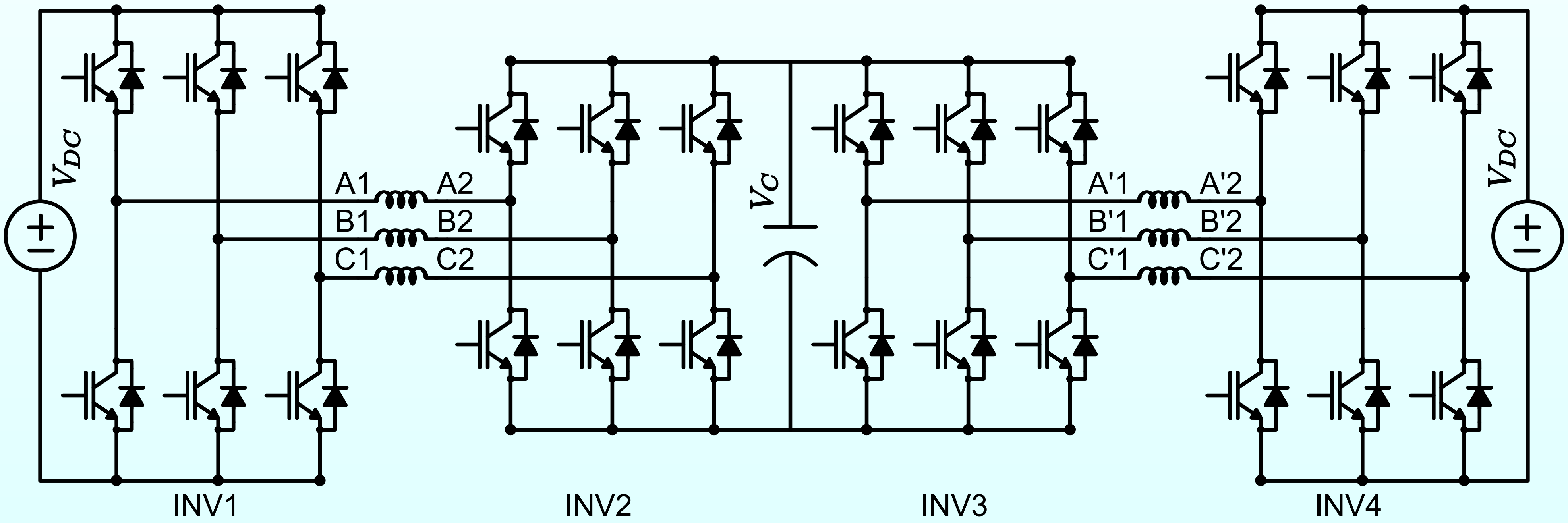
# Suppressing $5^{th}$ and $7^{th}$ Order Harmonics Contd…

- Effect in α-β plane
  - secondary vector 45' aids main vector 21'
    => DC-link $V_{dc}$ supplies power (discharging vector)
  - secondary vector 36' opposes main vector 21'
    => DC-link $V_{dc}$ sinks power (charging vector)




α-β plane

# Proposed Power Circuit




- Replace DC-link $V_{dc}$ with capacitor of voltage $V_c$
- Average the two possible (45' and 36') vectors to take zero net power from the capacitor

# Proposed Scheme Design

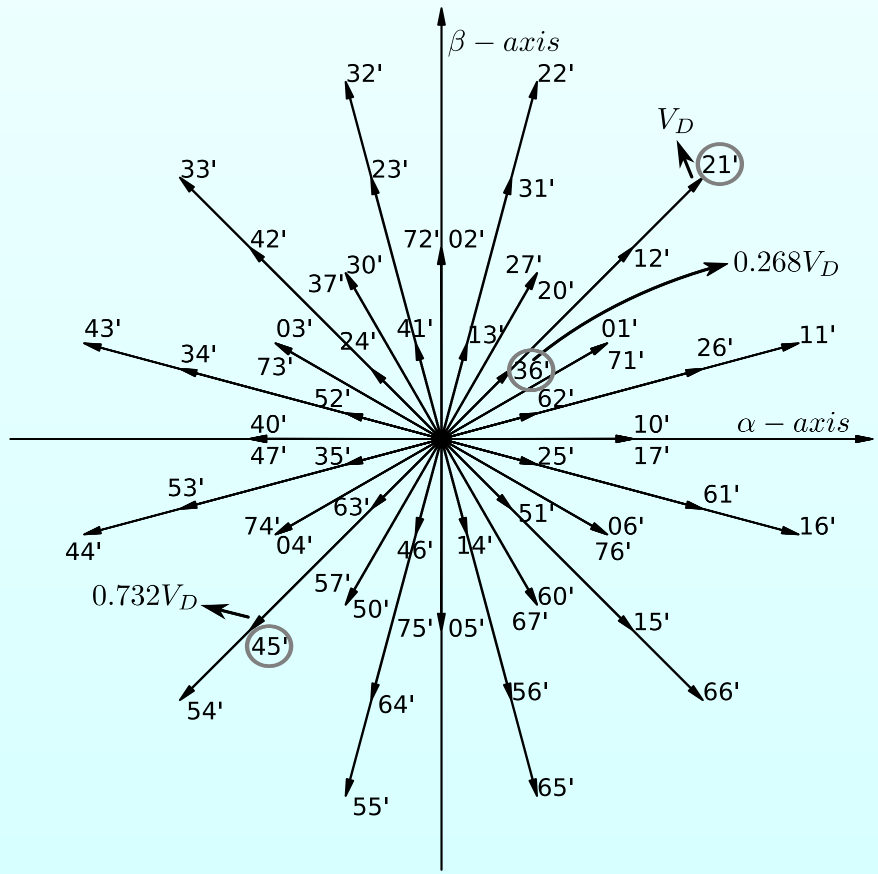
- Choose capacitor voltage $V_C$
- Find relative switching time duration of the two vectors from the open-end side
  - Charging vector (36') applied for $k*T_x$
  - Discharging vector (45') applied for $(1-k)*T_x$

# Finding time duration of the two vectors

$$V_D = 2V_{DC}cos15^o$$

$$V_d = 2V_c cos15^o$$

- Use volt-sec balance in α-β plane
  - net zero power due to two secondary vectors
  - $V_{dischrg} \cdot (1 - k)T_x = V_{chrg} \cdot k\ T_x$
  - $0.732V_d \cdot (1 - k)T_x = 0.268V_d \cdot k\ T_x$
  - $k = 0.732$



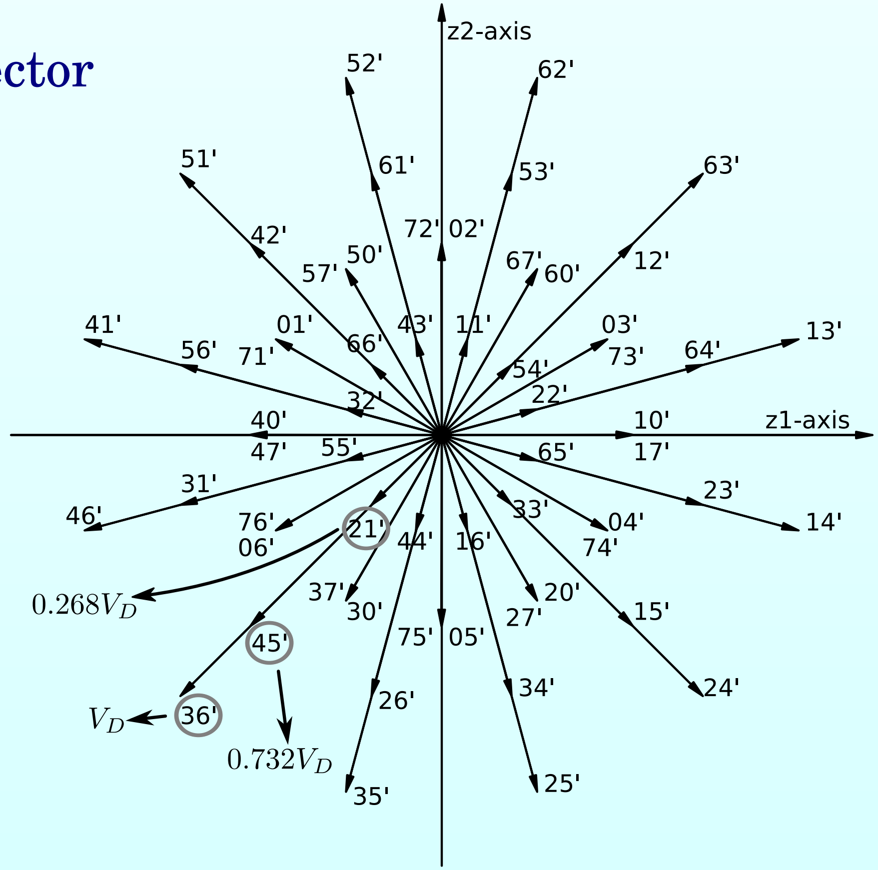

α-β plane

# Finding Required Capacitor Voltage

$$V_D = 2V_{DC}cos15^o$$

$$V_d = 2V_c cos15^o$$

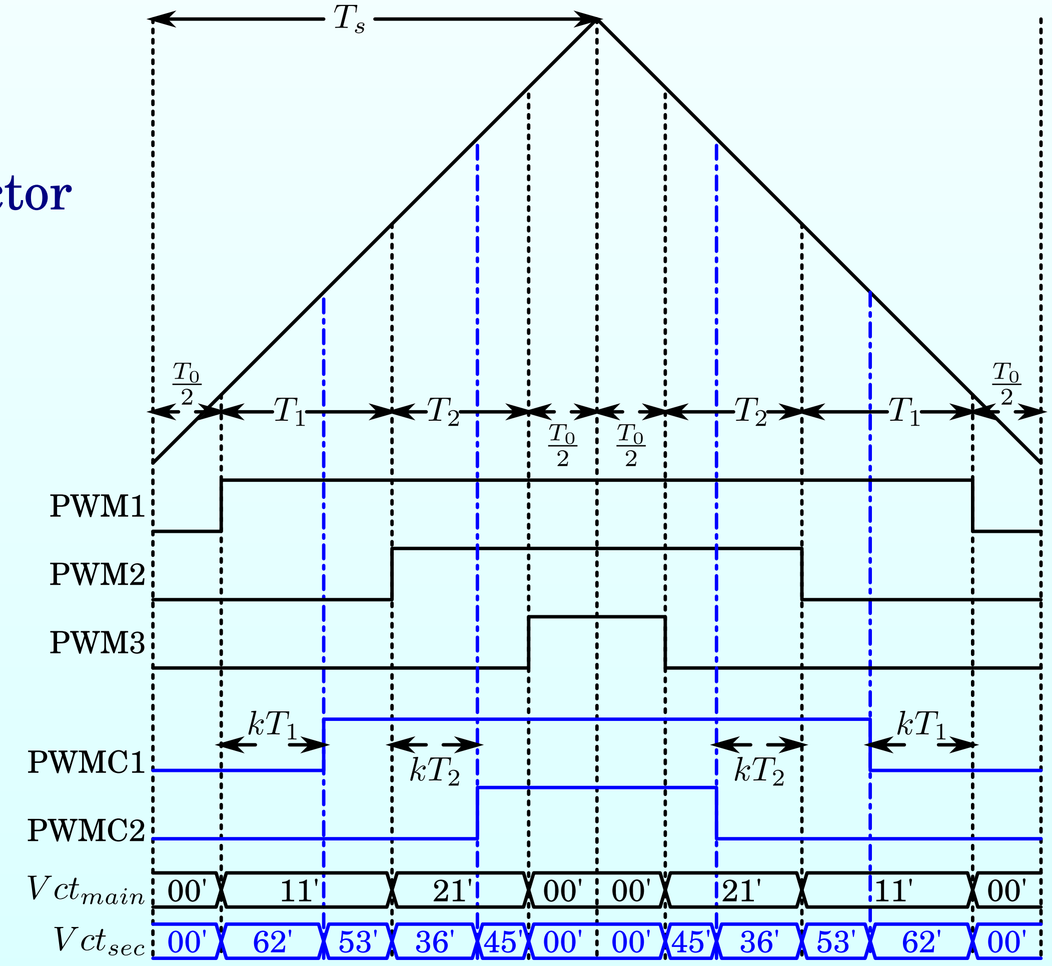
- Use volt-sec balance in z1-z2 plane
  - cancel 5th and 7th harmonics due to main vector
  - $V_{chrg} \cdot kT_x + V_{dischrg} \cdot (1 - k)T_x = V_{main} \cdot T_x$
  - $V_d \cdot kT_x + 0.732V_d \cdot (1 - k)T_x = 0.268V_D \cdot T_x$
  - using k = 0.732, gives $V_d = 0.289V_D$



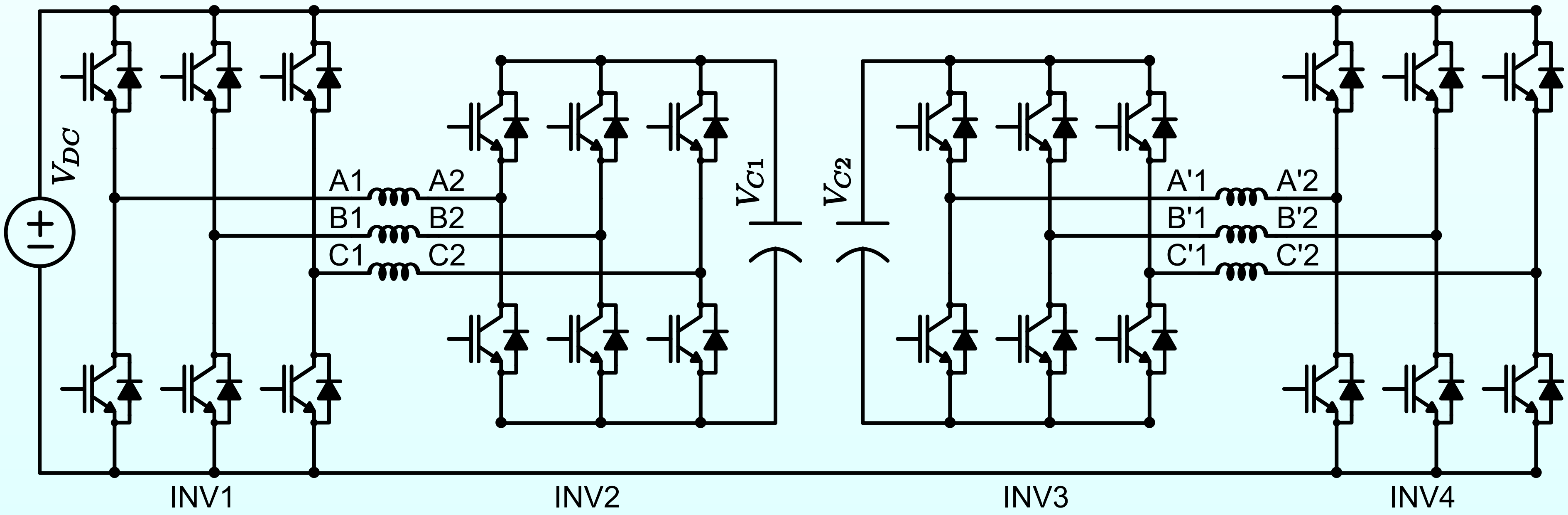

z1-z2 plane

# PWM Scheme

- Synchronized PWM with two sample per sector
- Conventional SVPWM for main inverter
- Two additional PWM for secondary inverter
  - one for each active vector
  - selects charging/discharging vector



# Alternate Power Circuit

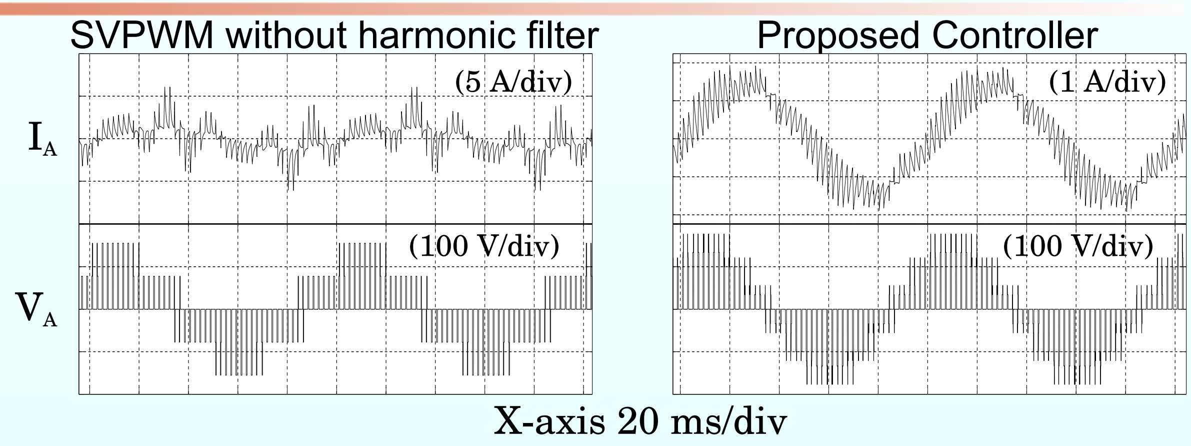



- Use two capacitors instead of one
- Replace two DC-link power supplies with single power supply

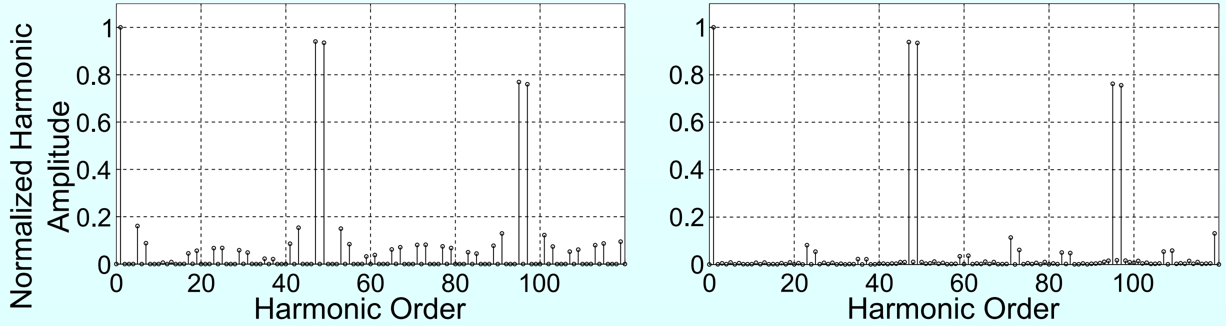
# Simulation Results - Phase Voltage & Current

Steady State waveforms @10 Hz

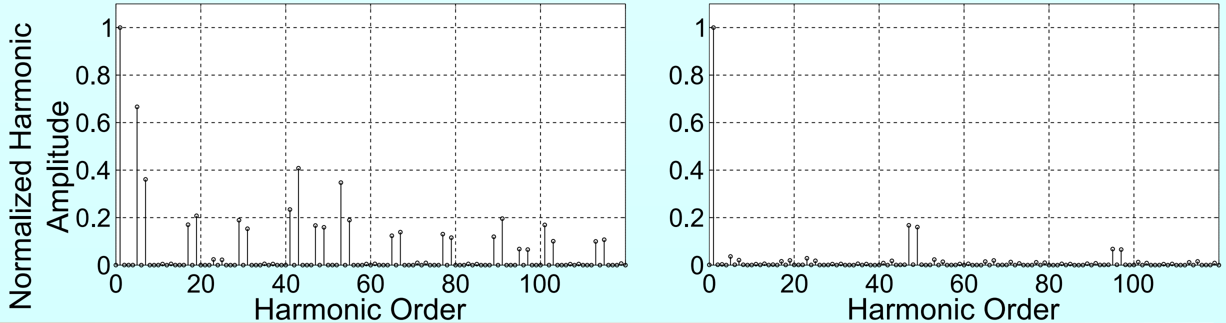
- SVPWM without harmonic filtering
  - Phase voltage : ~18% 5th Harmonic
  - Phase current : ~70% 5th Harmonic
- Proposed Controller
  - Phase voltage : <1% 5th Harmonic
  - Phase current : <5% 5th Harmonic




Normalized Harmonic Spectrum (FFT) of phase voltage



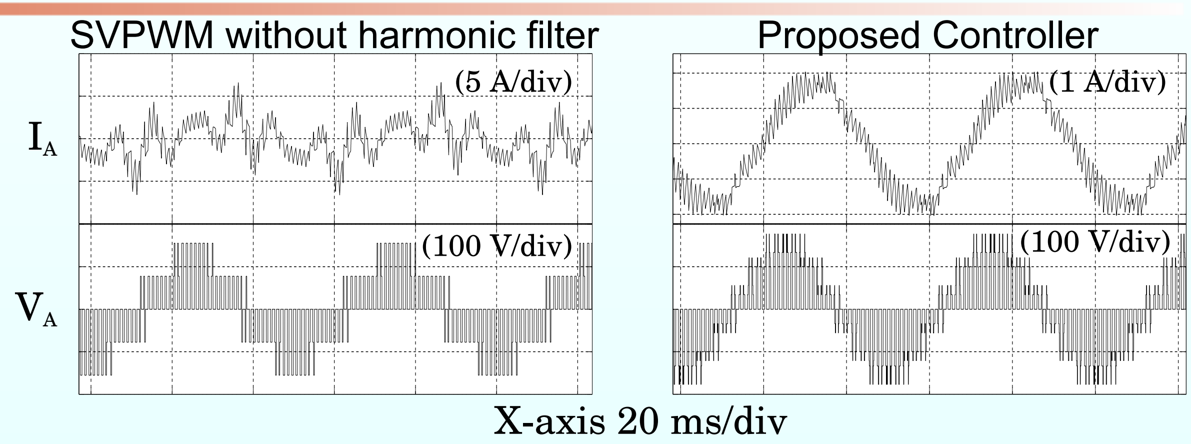

Normalized Harmonic Spectrum (FFT) of phase current



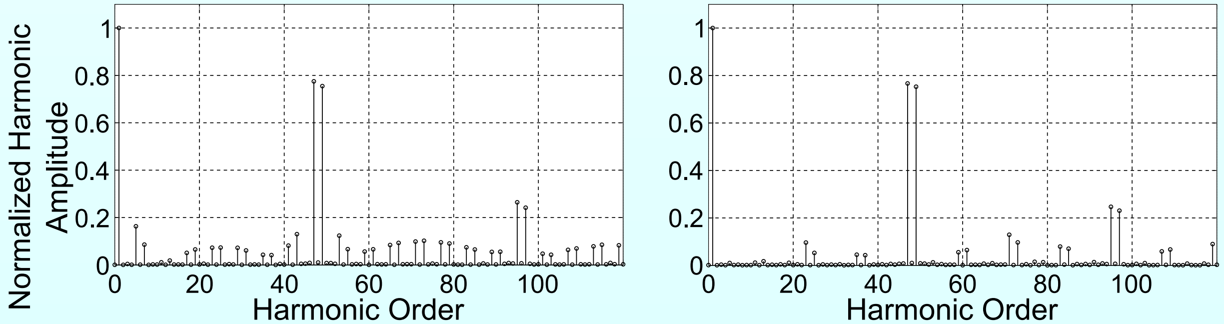
# Simulation Results - Phase Voltage & Current

Steady State waveforms @20 Hz

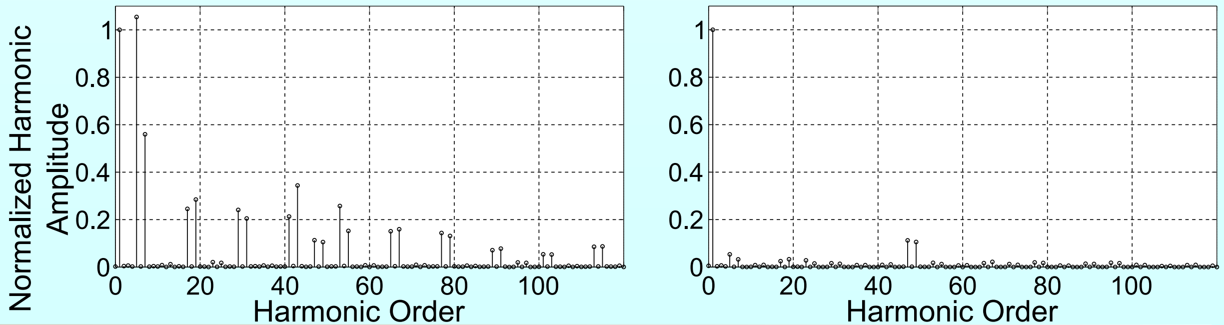
- SVPWM without harmonic filtering
  - Phase voltage : ~19% 5th Harmonic
  - Phase current : ~105% 5th Harmonic
- Proposed Controller
  - Phase voltage : <1% 5th Harmonic
  - Phase current : ~5% 5th Harmonic




Normalized Harmonic Spectrum (FFT) of phase voltage



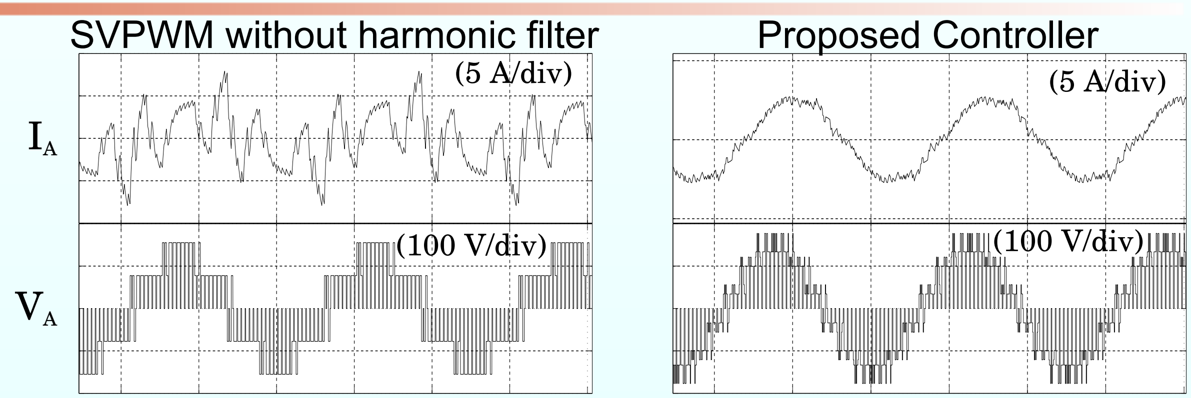

Normalized Harmonic Spectrum (FFT) of phase current



# Simulation Results - Phase Voltage & Current

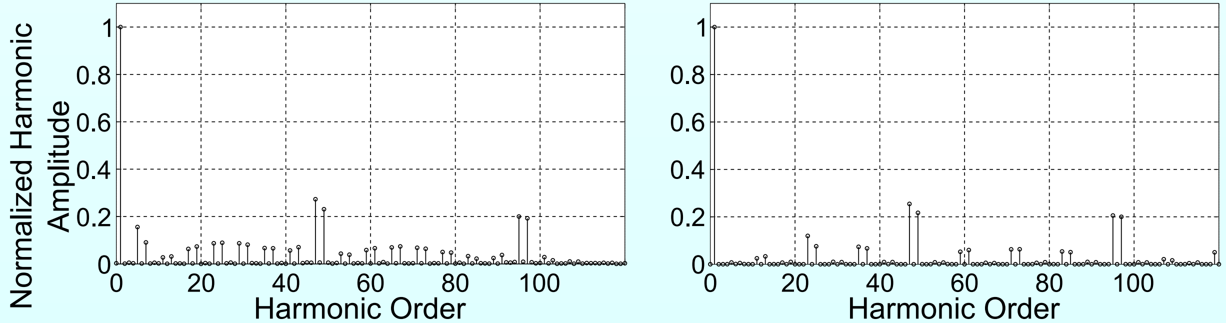
Steady State waveforms @40 Hz

- SVPWM without harmonic filtering
  - Phase voltage : ~19% 5th Harmonic
  - Phase current : ~122% 5th Harmonic
- Proposed Controller
  - Phase voltage : <1% 5th Harmonic
  - Phase current : <10% 5th Harmonic

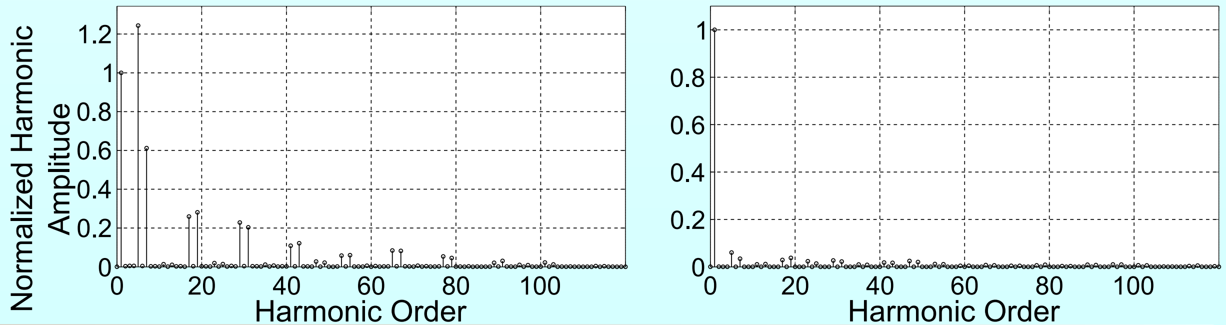



X-axis 10 ms/div

Normalized Harmonic Spectrum (FFT) of phase voltage



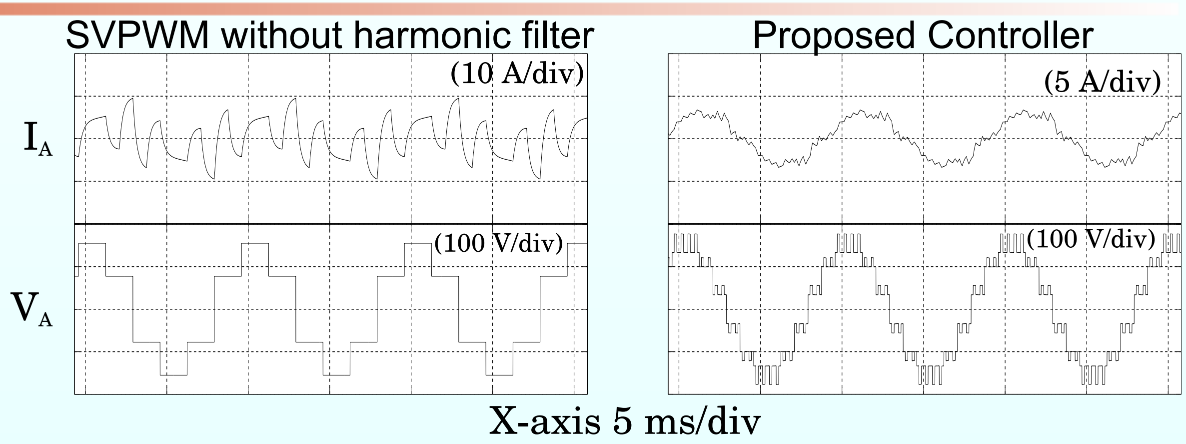

Normalized Harmonic Spectrum (FFT) of phase current



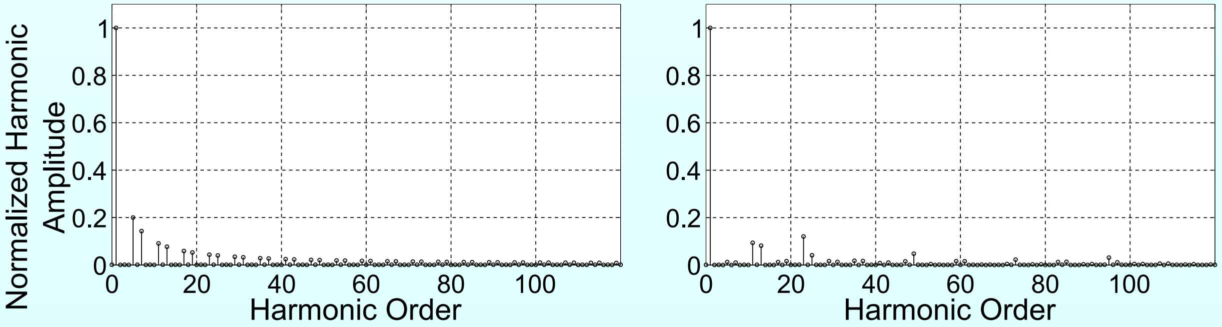
# Simulation Results - Phase Voltage & Current

Steady State waveforms @50 Hz

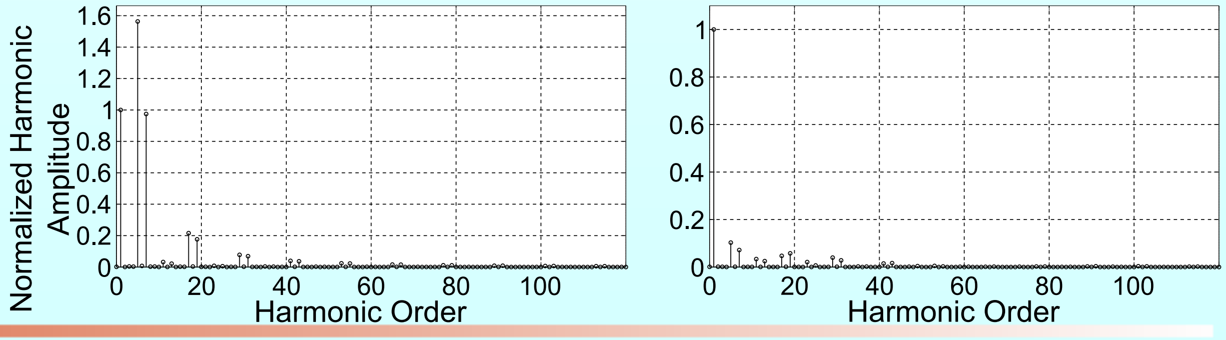
- SVPWM without harmonic filtering
  - Phase voltage : ~20% 5th Harmonic
  - Phase current : ~158% 5th Harmonic
- Proposed Controller
  - Phase voltage : <1% 5th Harmonic
  - Phase current : ~10% 5th Harmonic




Normalized Harmonic Spectrum (FFT) of phase voltage



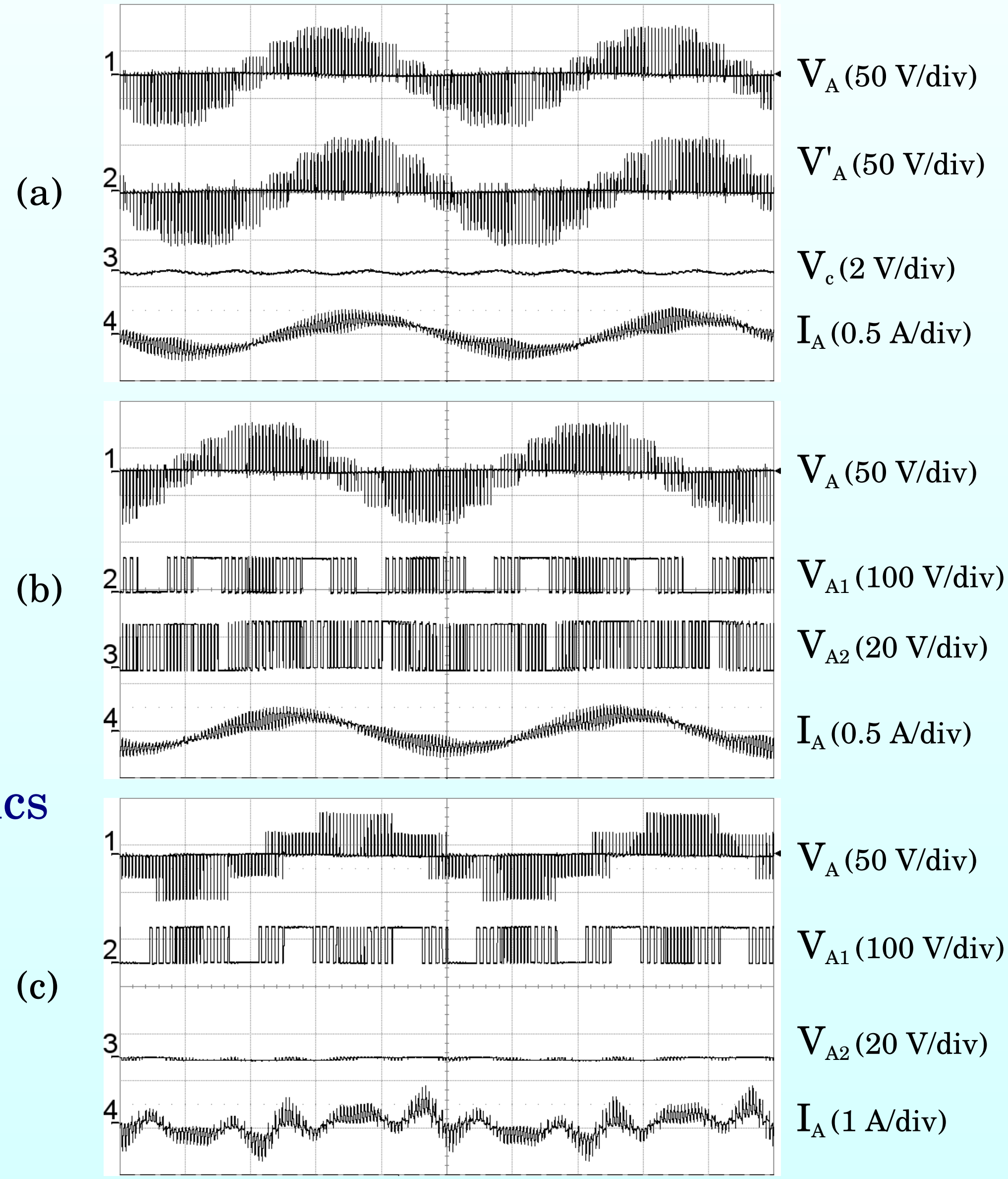

Normalized Harmonic Spectrum (FFT) of phase current



# Experimental Results

Steady State waveforms @10 Hz

- (a) and (b) Proposed Controller
  - Current - nearly sinusoidal
  - Capacitor voltage tightly controlled
- (c) SVPWM without filtering
  - Secondary inverters not switched
  - Current - high 5th and 7th order harmonics

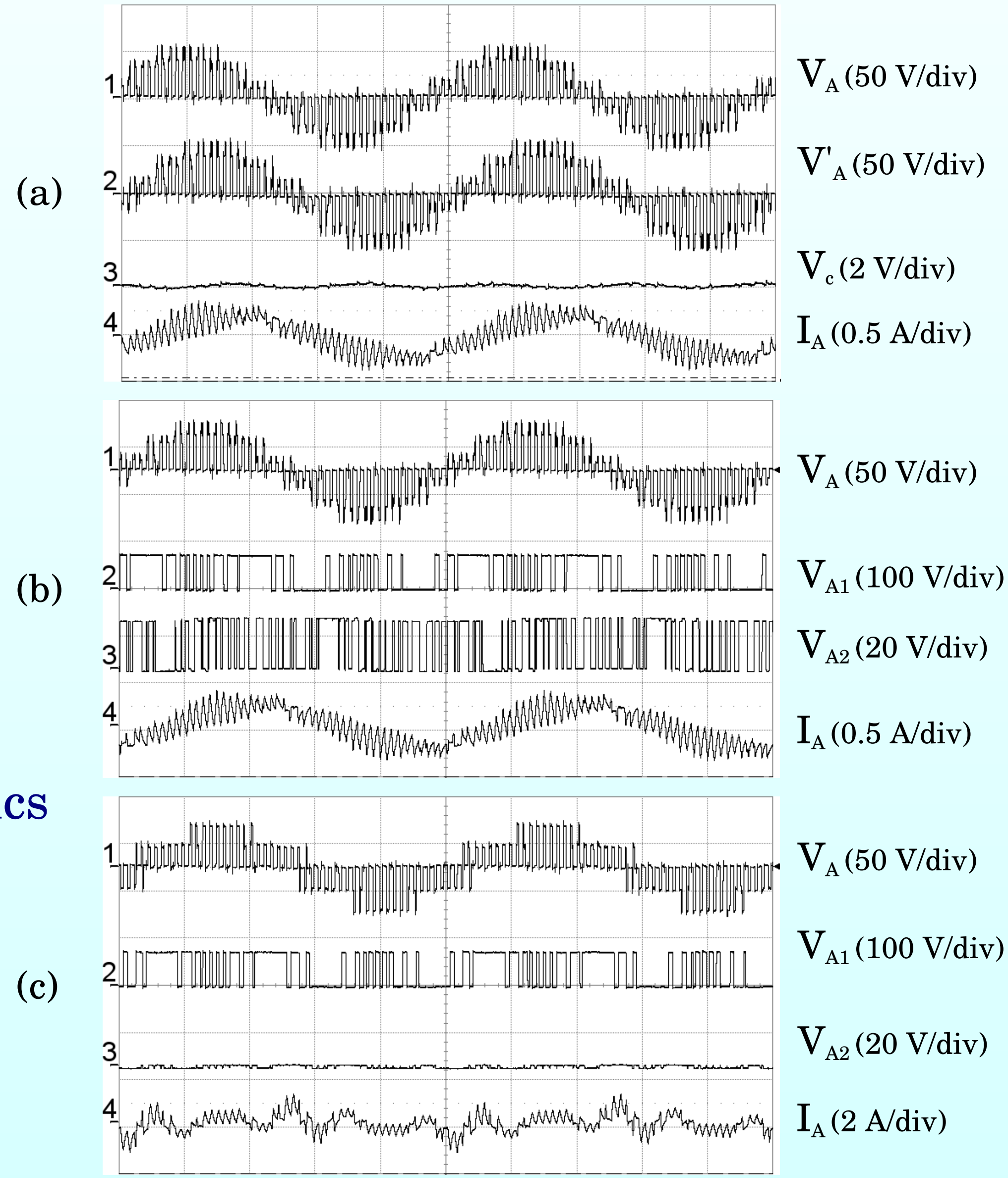



(X-axis 20 ms/div).

# Experimental Results

Steady State waveforms @20 Hz

- (a) and (b) Proposed Controller
  - Current - nearly sinusoidal
  - Capacitor voltage tightly controlled
- (c) SVPWM without filtering
  - Secondary inverters not switched
  - Current - high 5th and 7th order harmonics

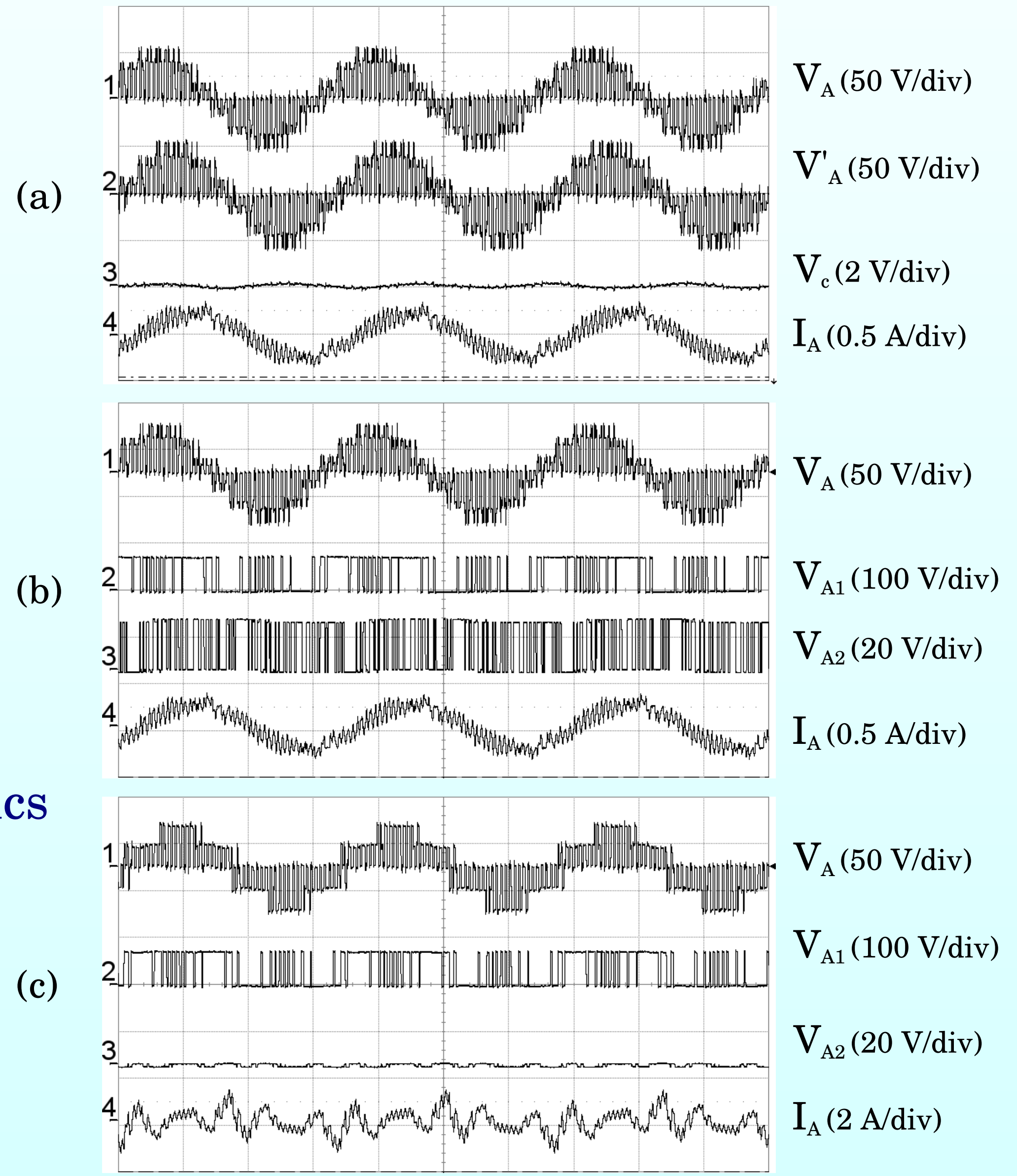



(X-axis 10 ms/div).

# Experimental Results

Steady State waveforms @30 Hz

- (a) and (b) Proposed Controller
  - Current - nearly sinusoidal
  - Capacitor voltage tightly controlled
- (c) SVPWM without filtering
  - Secondary inverters not switched
  - Current - high 5th and 7th order harmonics

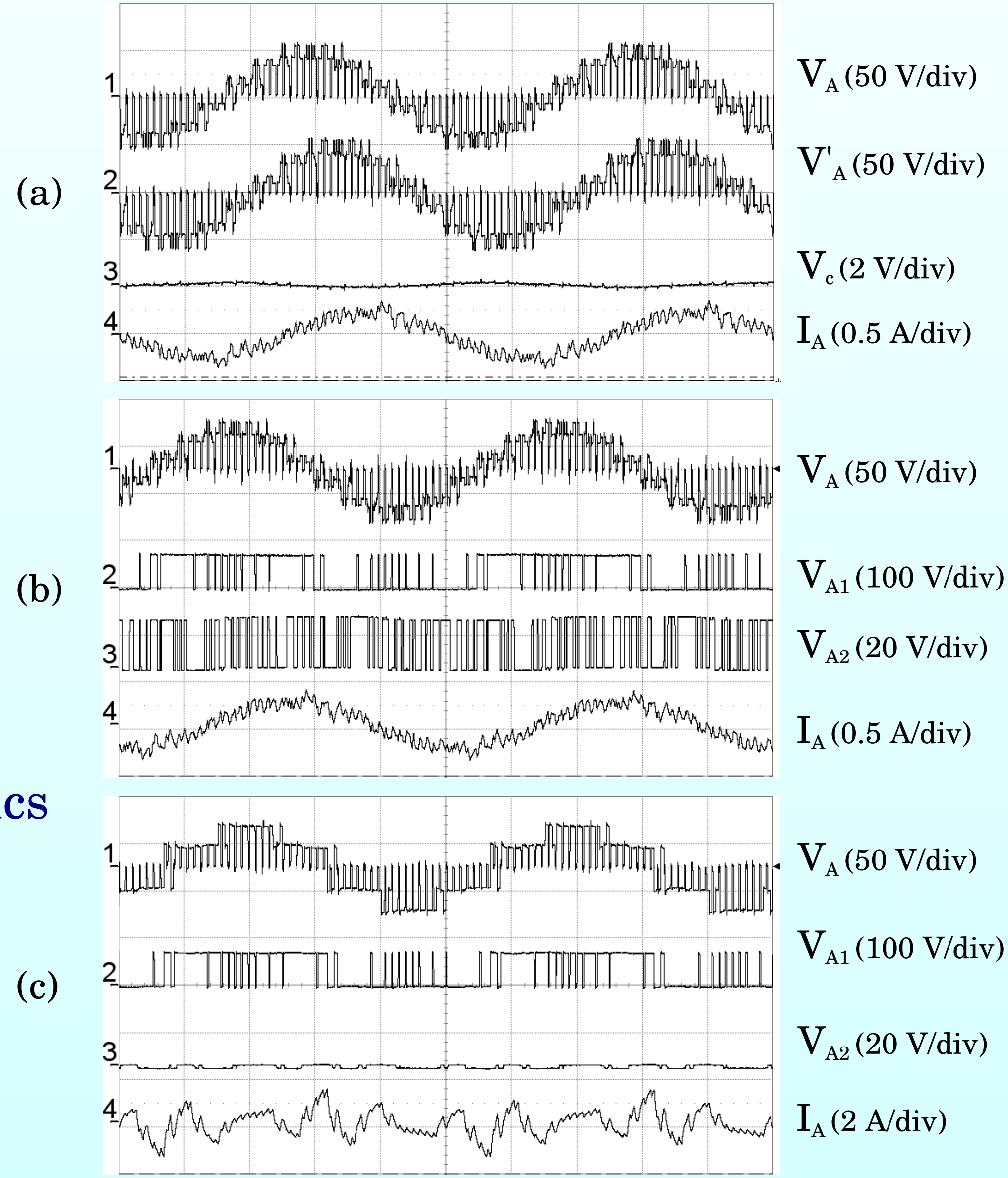



(X-axis 10 ms/div).

# Experimental Results

Steady State waveforms @40 Hz

- (a) and (b) Proposed Controller
  - Current - nearly sinusoidal
  - Capacitor voltage tightly controlled
- (c) SVPWM without filtering
  - Secondary inverters not switched
  - Current - high 5th and 7th order harmonics

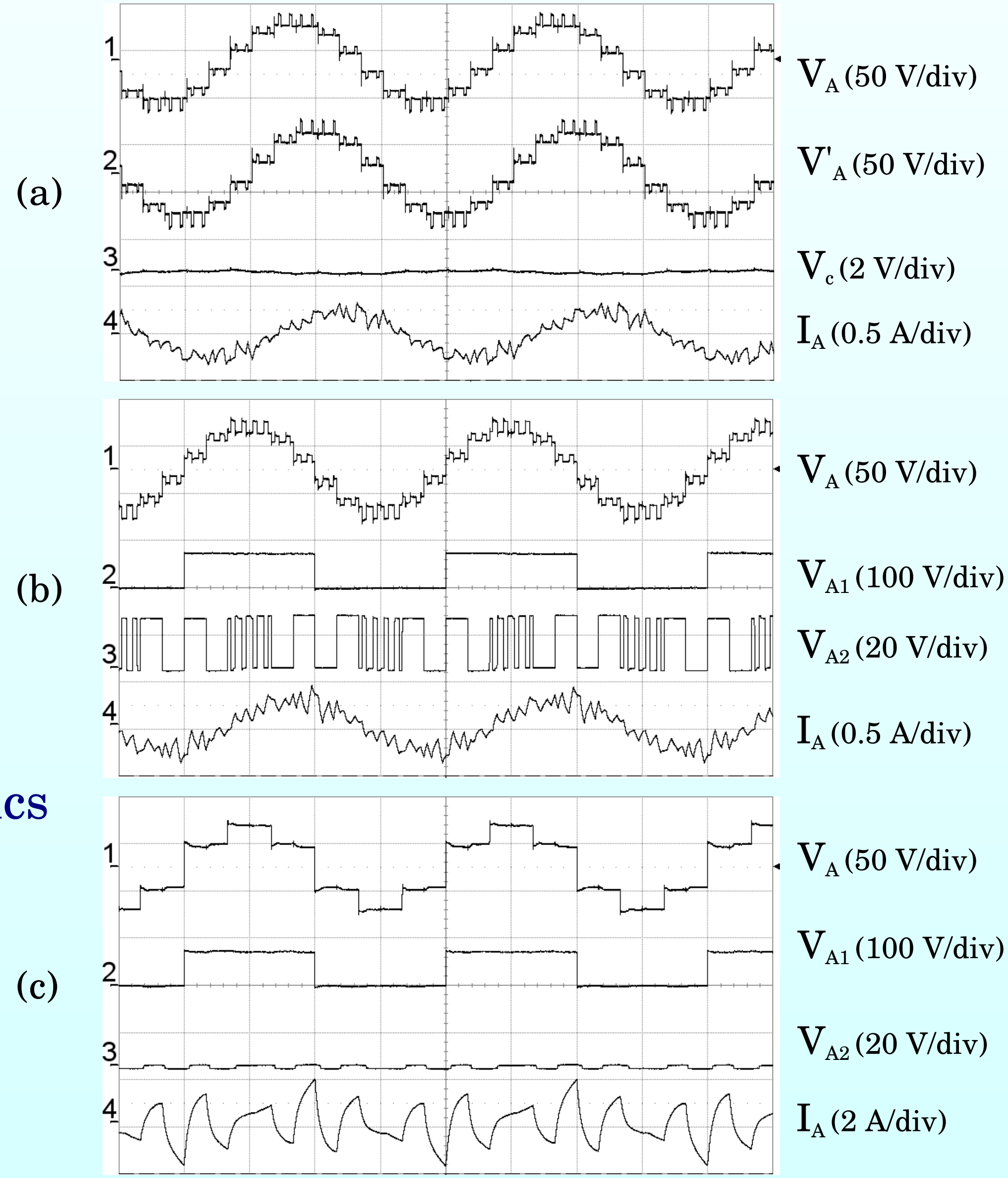



(X-axis 5 ms/div).

# Experimental Results

Steady State waveforms @50 Hz

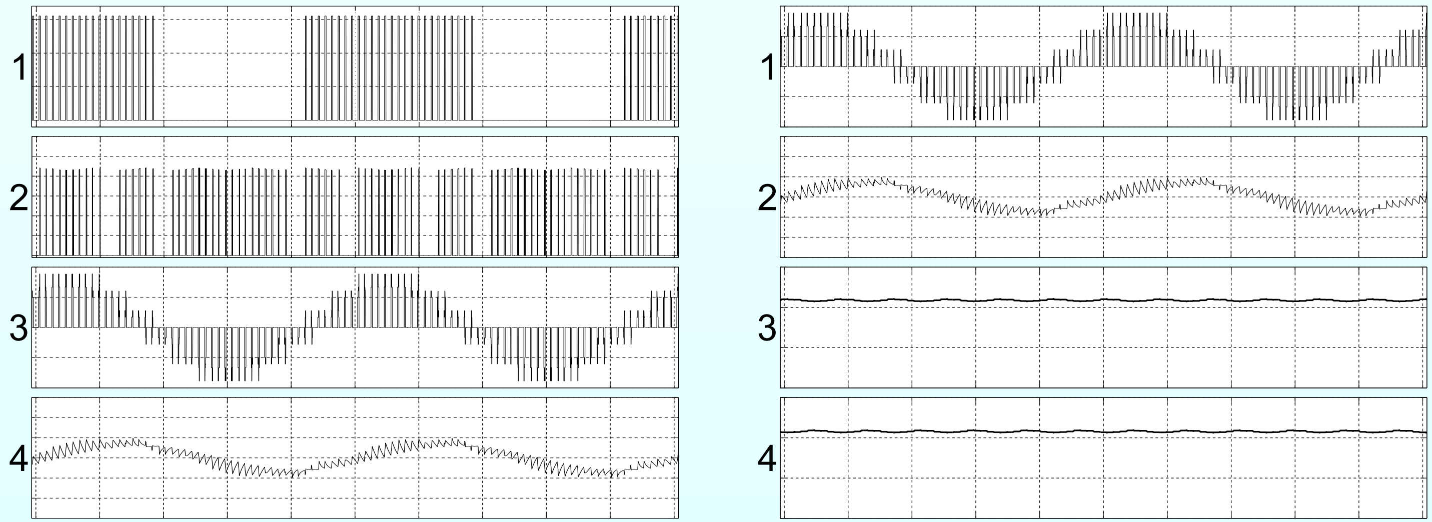
- (a) and (b) Proposed Controller
  - Current - nearly sinusoidal
  - Capacitor voltage tightly controlled
- (c) SVPWM without filtering
  - Secondary inverters not switched
  - Current - high 5th and 7th order harmonics




(X-axis 5 ms/div).

# Simulation Results -Alternate Scheme

Steady State waveforms @10 Hz




(a) (b)

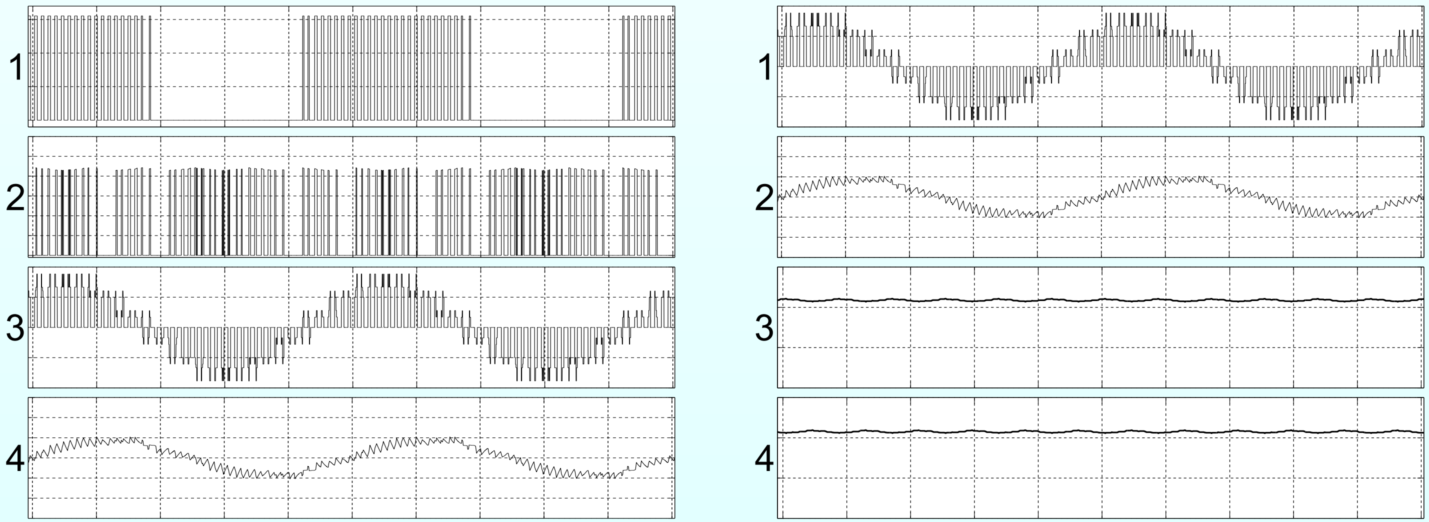
a1:Pole Voltage at A1 (50 V/div), a2:Pole Voltage at A2 (10 V/div)
a3:Phase Voltage (100 V/div), a4: Phase Current (2 A/div)

b1:Voltage of Phase A (100 V/div), b2:Current of Phase A (2 A/div)
b3:Capacitor Voltage $V_{C1}$ (20 V/div), b4:Capacitor Voltage $V_{C2}$ (20 V/div)

(X-axis 20 ms/div)

# Simulation Results -Alternate Scheme

Steady State waveforms @20 Hz




(a) (b)

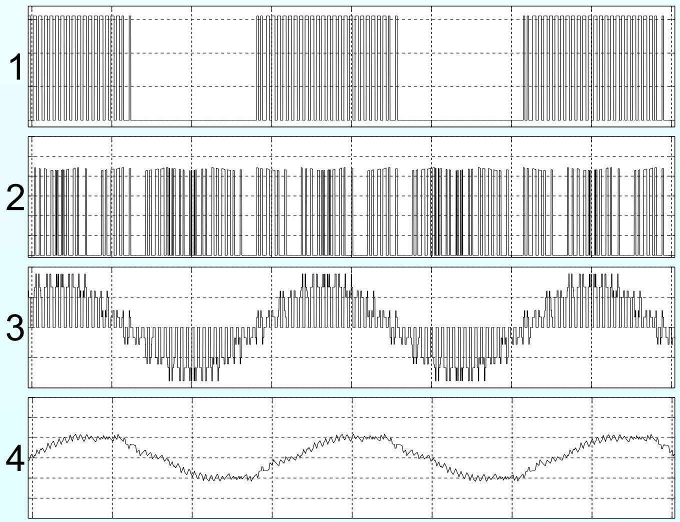
a1:Pole Voltage at A1 (50 V/div), a2:Pole Voltage at A2 (10 V/div)
a3:Phase Voltage (100 V/div), a4: Phase Current (2 A/div)

b1:Voltage of Phase A (100 V/div), b2:Current of Phase A (2 A/div)
b3:Capacitor Voltage $V_{C1}$ (20 V/div), b4:Capacitor Voltage $V_{C2}$ (20 V/div)

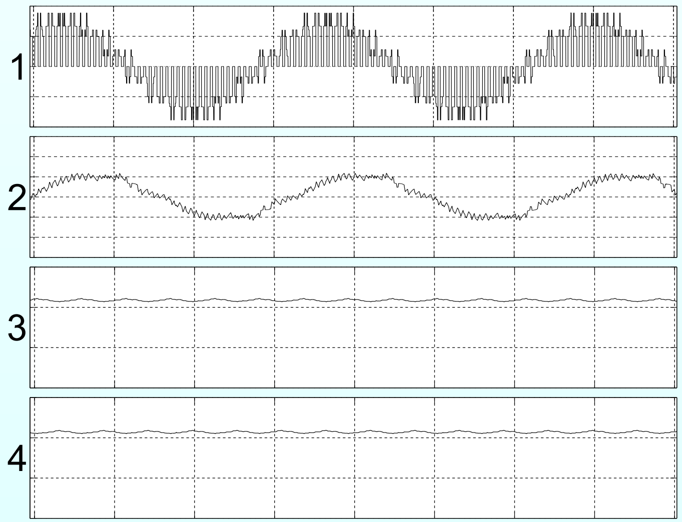
(X-axis 10 ms/div)

# Simulation Results -Alternate Scheme

Steady State waveforms @30 Hz



(a)



(b)

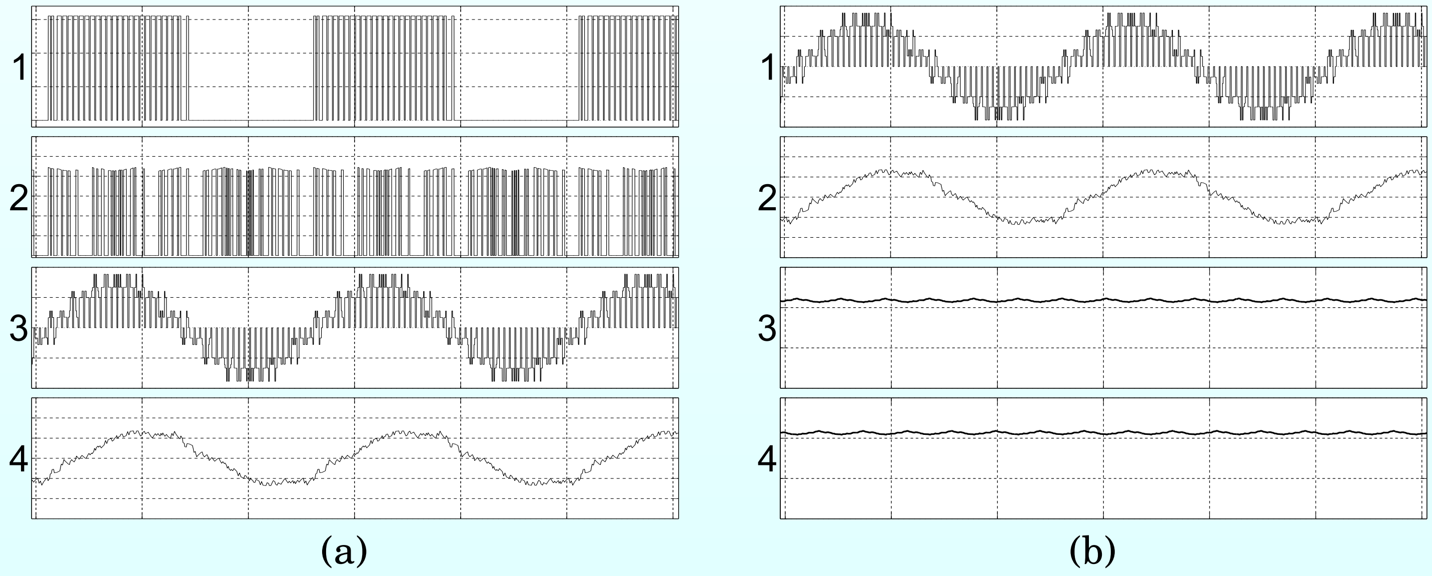
a1:Pole Voltage at A1 (50 V/div), a2:Pole Voltage at A2 (10 V/div)
a3:Phase Voltage (100 V/div), a4: Phase Current (2 A/div)

b1:Voltage of Phase A (100 V/div), b2:Current of Phase A (2 A/div)
b3:Capacitor Voltage $V_{C1}$ (20 V/div), b4:Capacitor Voltage $V_{C2}$ (20 V/div)

(X-axis 10 ms/div)

# Simulation Results -Alternate Scheme

Steady State waveforms @40 Hz



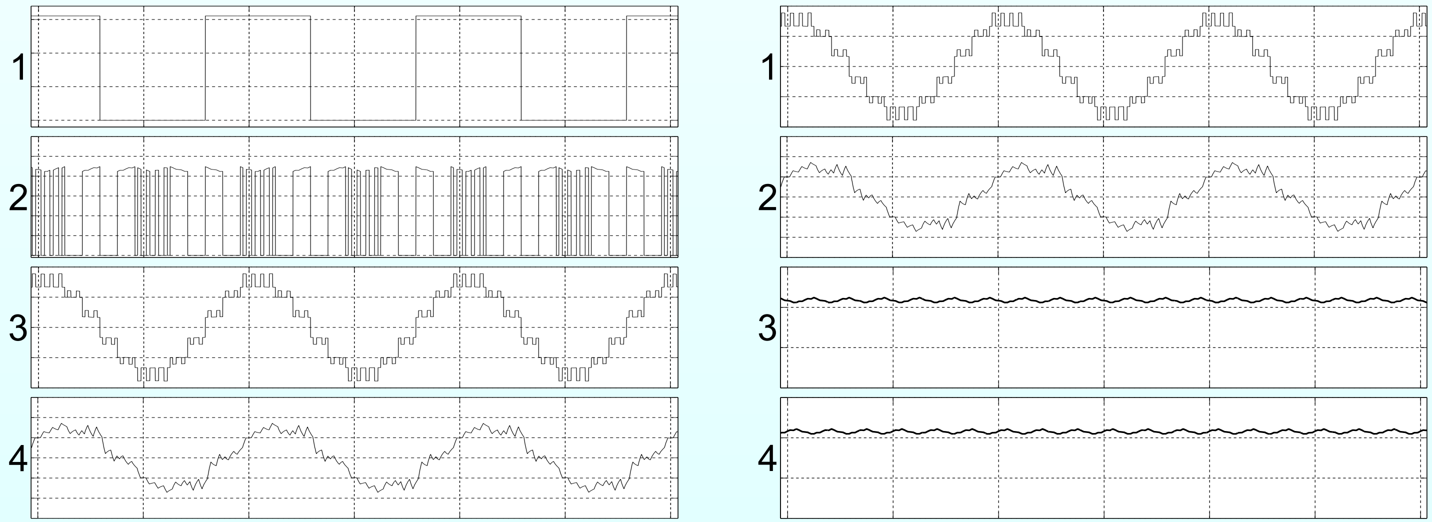

a1:Pole Voltage at A1 (50 V/div), a2:Pole Voltage at A2 (10 V/div)
a3:Phase Voltage (100 V/div), a4: Phase Current (2 A/div)

b1:Voltage of Phase A (100 V/div), b2:Current of Phase A (2 A/div)
b3:Capacitor Voltage $V_{C1}$ (20 V/div), b4:Capacitor Voltage $V_{C2}$ (20 V/div)

(X-axis 10 ms/div)

# Simulation Results -Alternate Scheme

Steady State waveforms @50 Hz



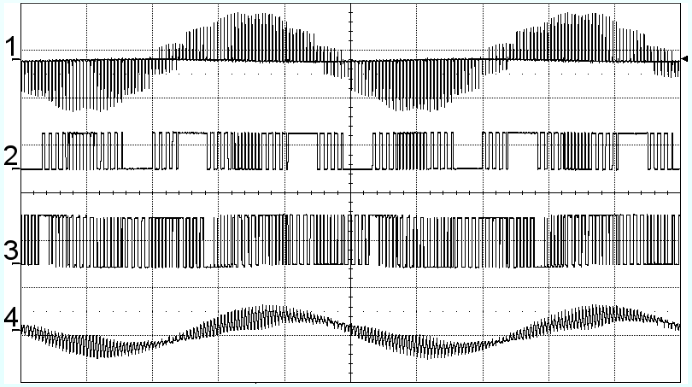

a1:Pole Voltage at A1 (50 V/div), a2:Pole Voltage at A2 (10 V/div)
a3:Phase Voltage (100 V/div), a4: Phase Current (2 A/div)

b1:Voltage of Phase A (100 V/div), b2:Current of Phase A (2 A/div)
b3:Capacitor Voltage $V_{C1}$ (20 V/div), b4:Capacitor Voltage $V_{C2}$ (20 V/div)

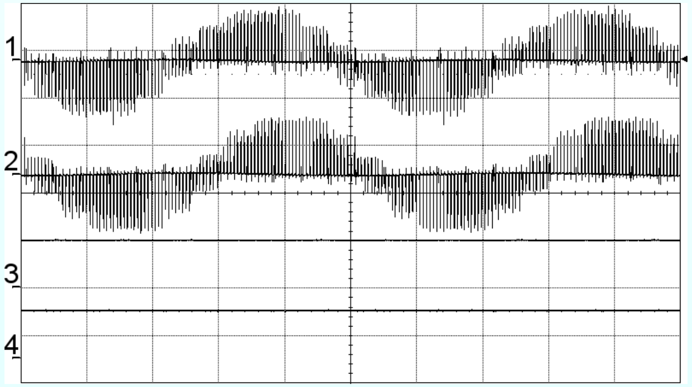
(X-axis 10 ms/div)

# Experimental Results - Alternate Scheme

Steady State waveforms @10 Hz




(a)




(b)

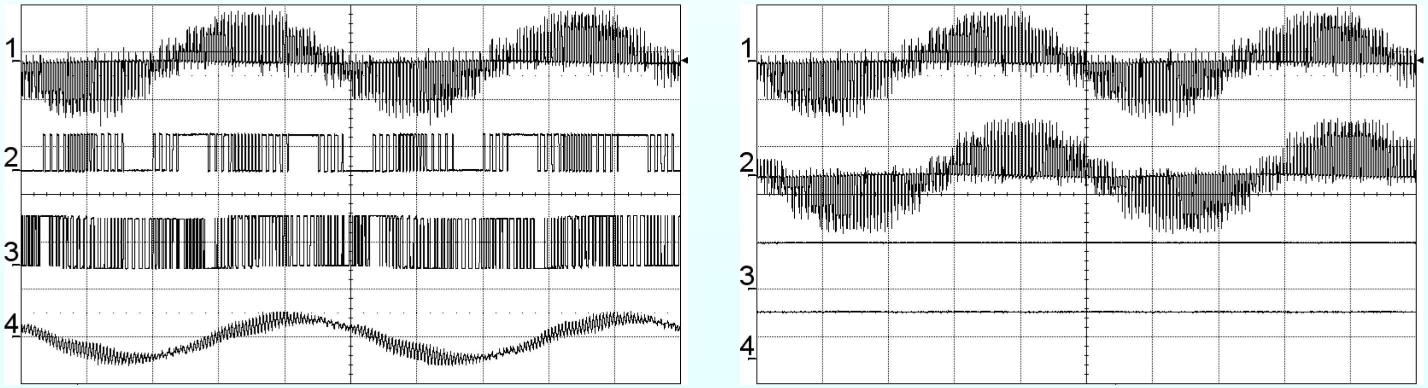
a1:Phase Voltage (50 V/div), a2:Pole Voltage at A1 (100 V/div),
a3: Pole Voltage at A2 (20 V/div), a4:Phase Current (0.5 A/div)

b1:Phase Voltage A (50 V/div), b2:Phase Voltage A' (50 V/div),
b3:Capacitor Voltage $V_{C1}$ (20 V/div), 4:Capacitor Voltage $V_{C2}$ (20 V/div)

(X-axis 20 ms/div).

# Experimental Results - Alternate Scheme

Steady State waveforms @20Hz




(a) (b)

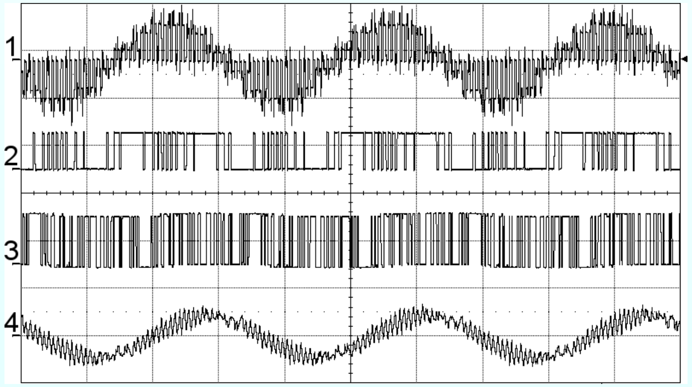
a1:Phase Voltage (50 V/div), a2:Pole Voltage at A1 (100 V/div),
a3: Pole Voltage at A2 (20 V/div), a4:Phase Current (0.5 A/div)

b1:Phase Voltage A (50 V/div), b2:Phase Voltage A' (50 V/div),
b3:Capacitor Voltage $V_{C1}$ (20 V/div), 4:Capacitor Voltage $V_{C2}$ (20 V/div)

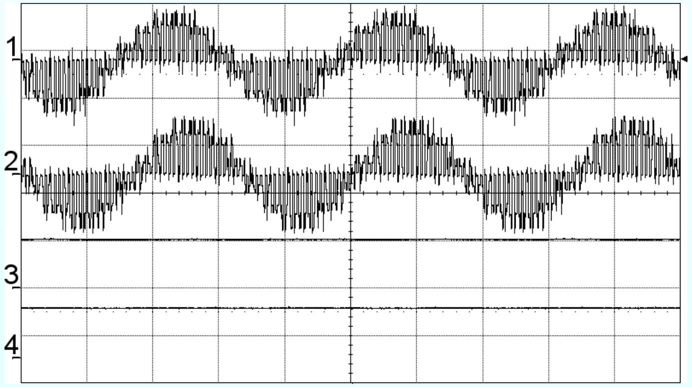
(X-axis 10 ms/div).

# Experimental Results - Alternate Scheme

Steady State waveforms @30Hz




(a)




(b)

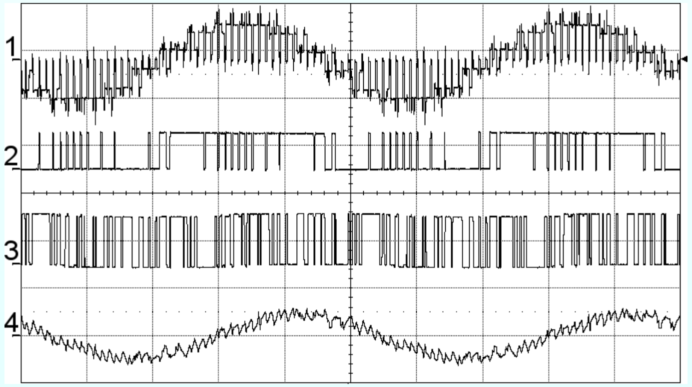
a1:Phase Voltage (50 V/div), a2:Pole Voltage at A1 (100 V/div),
a3: Pole Voltage at A2 (20 V/div), a4:Phase Current (0.5 A/div)

b1:Phase Voltage A (50 V/div), b2:Phase Voltage A' (50 V/div),
b3:Capacitor Voltage $V_{C1}$ (20 V/div), 4:Capacitor Voltage $V_{C2}$ (20 V/div)

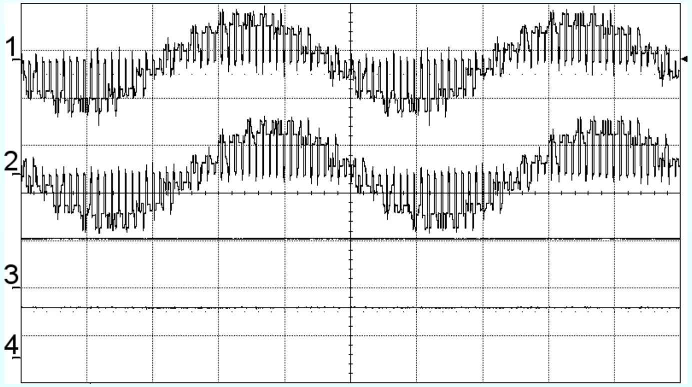
(X-axis 10 ms/div).

# Experimental Results - Alternate Scheme

Steady State waveforms @40Hz




(a)




(b)

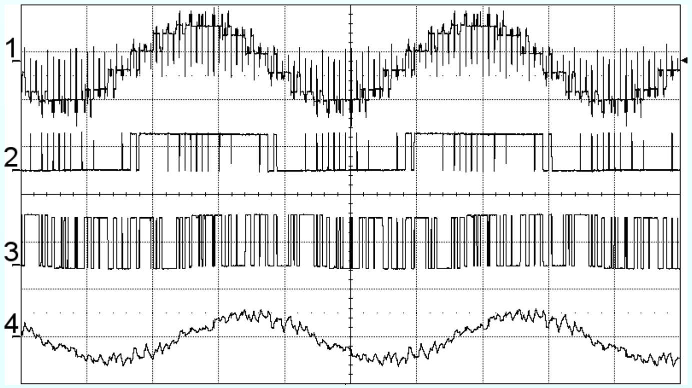
a1:Phase Voltage (50 V/div), a2:Pole Voltage at A1 (100 V/div),
a3: Pole Voltage at A2 (20 V/div), a4:Phase Current (0.5 A/div)

b1:Phase Voltage A (50 V/div), b2:Phase Voltage A' (50 V/div),
b3:Capacitor Voltage $V_{C1}$ (20 V/div), 4:Capacitor Voltage $V_{C2}$ (20 V/div)

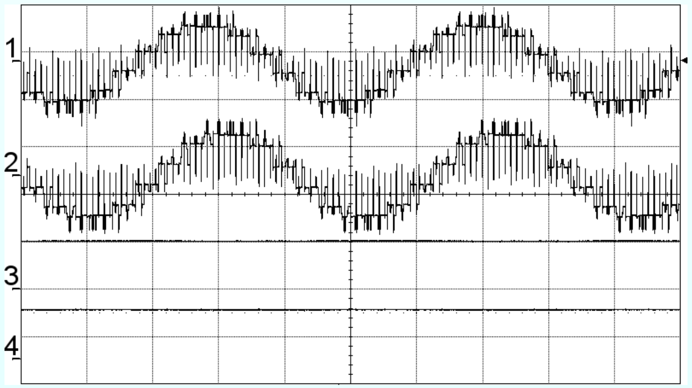
(X-axis 5 ms/div).

# Experimental Results - Alternate Scheme

Steady State waveforms @48Hz




(a)




(b)

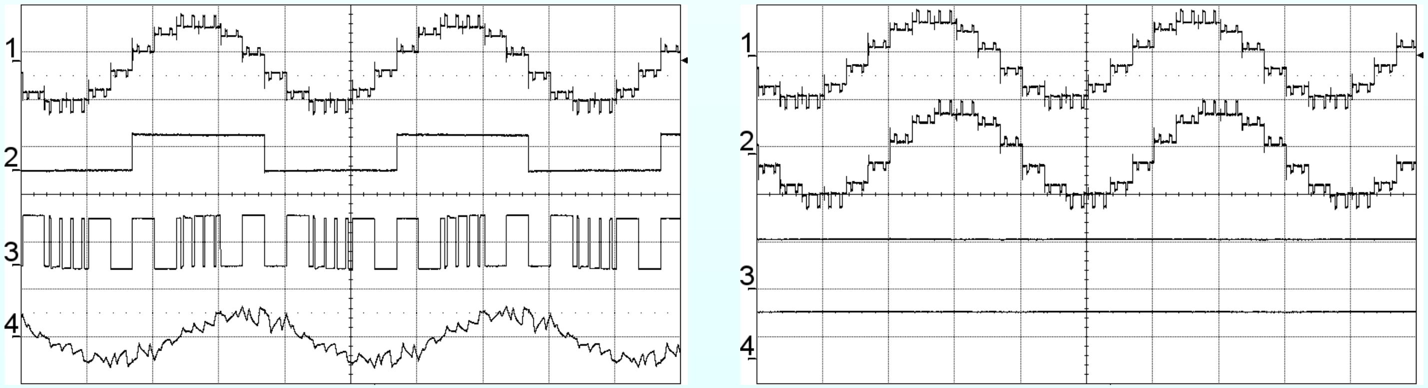
a1:Phase Voltage (50 V/div), a2:Pole Voltage at A1 (100 V/div),
a3: Pole Voltage at A2 (20 V/div), a4:Phase Current (0.5 A/div)

b1:Phase Voltage A (50 V/div), b2:Phase Voltage A' (50 V/div),
b3:Capacitor Voltage $V_{C1}$ (20 V/div), 4:Capacitor Voltage $V_{C2}$ (20 V/div)

(X-axis 5 ms/div).

# Experimental Results - Alternate Scheme

Steady State waveforms @50Hz




(a) (b)

a1:Phase Voltage (50 V/div), a2:Pole Voltage at A1 (100 V/div),
a3: Pole Voltage at A2 (20 V/div), a4:Phase Current (0.5 A/div)

b1:Phase Voltage A (50 V/div), b2:Phase Voltage A' (50 V/div),
b3:Capacitor Voltage $V_{C1}$ (20 V/div), 4:Capacitor Voltage $V_{C2}$ (20 V/div)

(X-axis 5 ms/div).

# Conclusion

- New scheme for harmonic suppression in split-phase IM
  - No need of bulky inductive filters, or complex PWM techniques
- Secondary inverters for harmonic suppression
- Simple PWM technique
- Valid upto full modulation range (square wave mode operation of main inverter)
  - 5th harmonic reduced from 158% to less than 10% (@ Square wave operation)

# Journal Papers

- “A nearly constant switching frequency Current Error Space Vector Based Hysteresis Controller for an IM drive with 12-sided polygonal voltage space vectors” – Najath Abdul Azeez, Anubrata Dey, K. Mathew, Jaison Mathew, K. Gopakumar, accepted for publication in EPE( European Power Electronics Association) journal.

- “A Medium Voltage Inverter Fed IM Drive using Multilevel 12-sided polygonal Vectors, with Nearly Constant Switching Frequency Current Hysteresis Controller,” Najath Abdul Azeez; Gopakumar, K.; Mathew, J.; K, M.; Dey, A.; Kazmierkowski, M., accepted for publication in IEEE Transactions on Industrial Electronics.

- "A Harmonic Suppression Scheme for Open-End Winding Split-Phase IM Drive Using Capacitive Filters, For The Full Speed Range"
Najath Abdul Azeez, Jaison Mathew, K. Gopakumar and Carlo Cecati
under review in IEEE Transactions on Industrial Electronics.

# Conference Papers

- “A 5th and 7th Order Harmonic Suppression Scheme for Open-end winding Asymmetrical Six-phase IM Drive Using Capacitor-fed Inverter” – Najath Abdul Azeez, Jaison Mathew, K. Gopakumar, Carlo Cecati, accepted for IECON 2013

- “A nearly constant switching frequency current hysteresis controller with generalized parabolic boundaries using 12-sided polygonal voltage space vectors for IM drives,” Najath Abdul Azeez; Dey, A.; Mathew, K.; Mathew, J.; Gopakumar, K., XXth International Conference on Electrical Machines (ICEM), 2012 vol., no., pp.810-815, 2-5 Sept. 2012

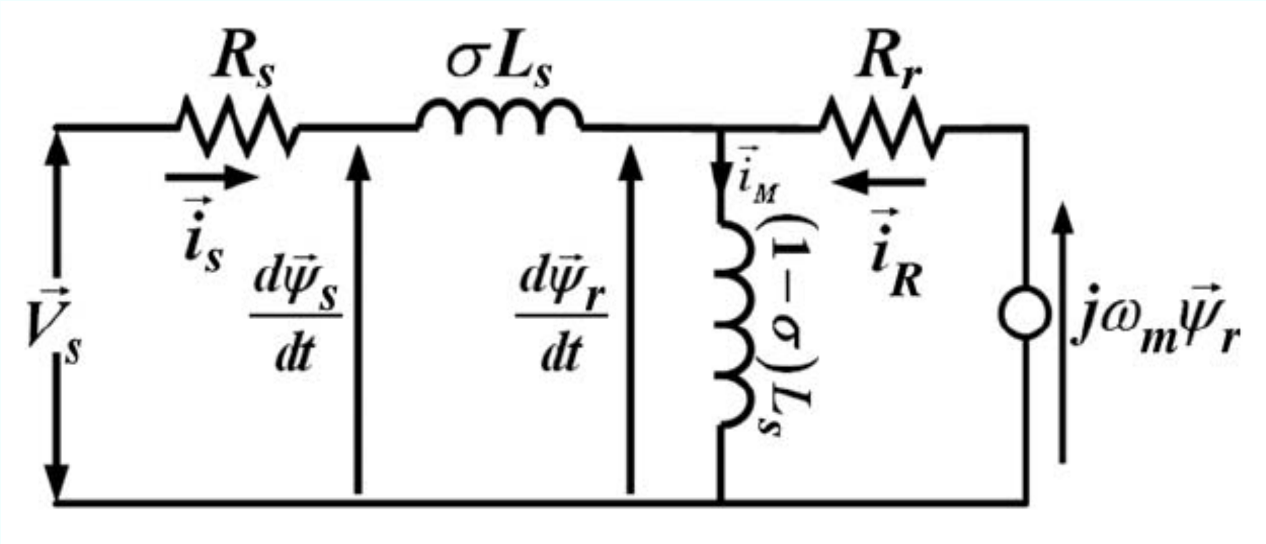
# Conclusion

## Conclusion

- HCC for single and multilevel dodecagonal VSI fed IM drives
- Harmonic suppression scheme for open-end winding split-phase IM

# Thank You

# Estimating of Fundamental Stator Voltage




Space phasor based equivalent circuit of IM in the stationary reference frame with rotor flux as reference vector

$$\vec{V}_k = R_s\vec{i}_s + \sigma L_s\frac{d\vec{i}_s}{dt} + \frac{d\vec{\Psi}_r}{dt};$$

$$\vec{i}_s = \vec{i}_s^* + \Delta\vec{i}_s$$

$$\vec{V}_k = R_s\left(\vec{i}_s^* + \Delta\vec{i}_s\right) + \sigma L_s\frac{d\left(\vec{i}_s^* + \Delta\vec{i}_s\right)}{dt} + \frac{d\vec{\Psi}_r}{dt}$$

$$taking \quad \vec{V}_s = R_s\vec{i}_s^* + \sigma L_s\frac{d\vec{i}_s^*}{dt} + \frac{d\vec{\Psi}_r}{dt}$$

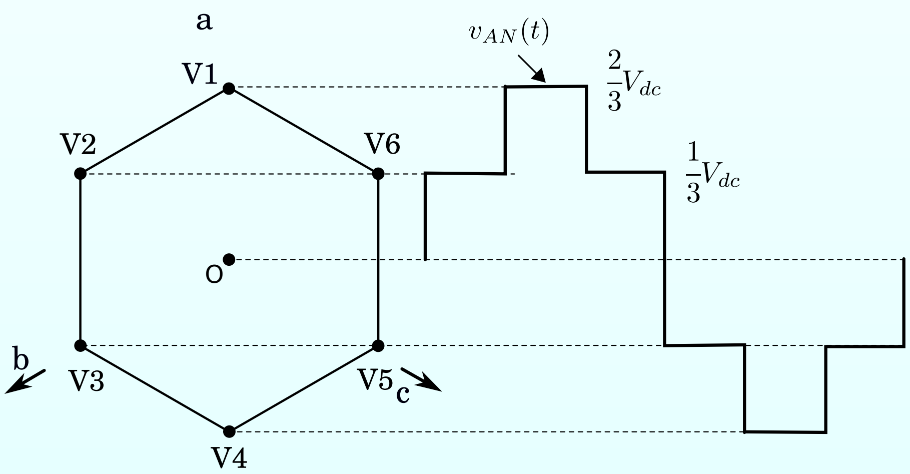
$$then \quad \vec{V}_k = \vec{V}_s + R_s\Delta\vec{i}_s + \sigma L_s\frac{d\Delta\vec{i}_s}{dt}$$

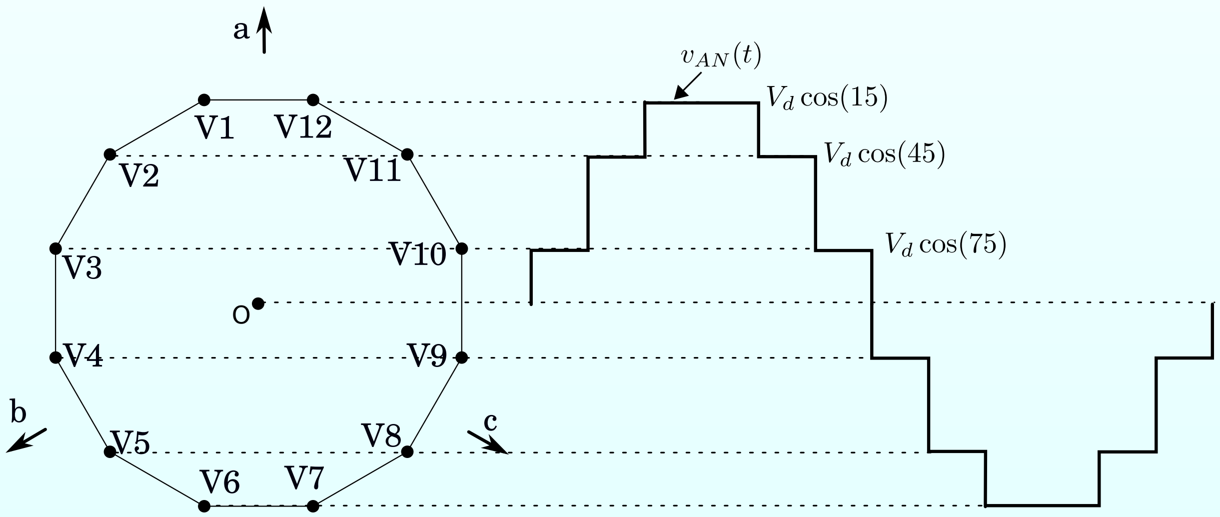
$$\Rightarrow \vec{V}_s = \vec{V}_k - R_s\Delta\vec{i}_s - \sigma L_s\frac{d\Delta\vec{i}_s}{dt} \quad . \quad \Longrightarrow$$

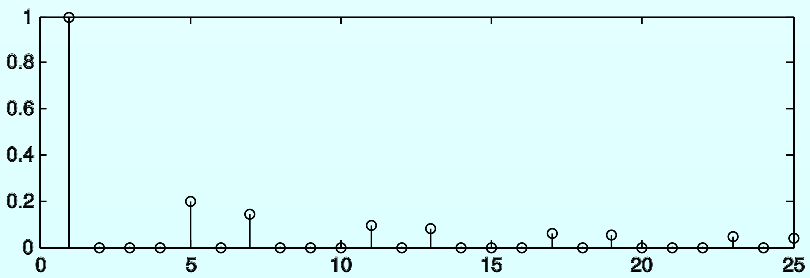
$$V_{s\alpha} = V_{k\alpha} - \Delta i_{s\alpha}R_s - \sigma L_s\frac{d\Delta i_{s\alpha}}{dt}$$

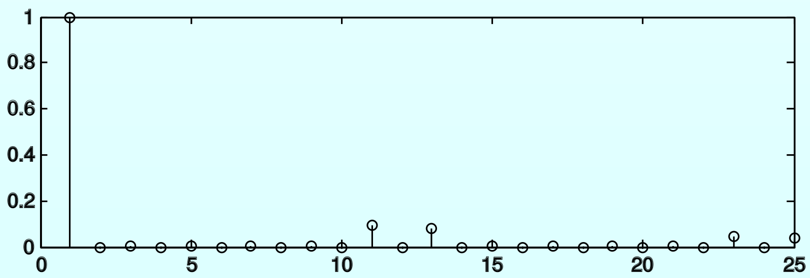
$$\& \ V_{s\beta} = V_{k\beta} - \Delta i_{s\beta}R_s - \sigma L_s\frac{d\Delta i_{s\beta}}{dt}$$

# Harmonic Analysis



# Dodecagon Vs Hexagon comparison

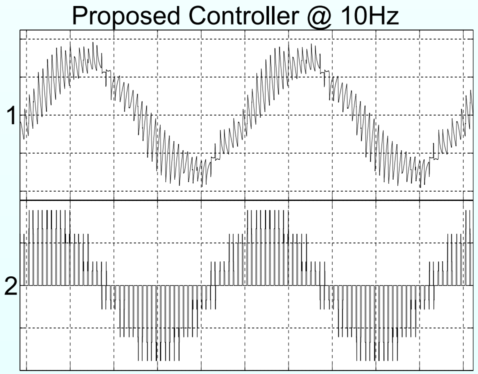
Maximum Fundamental voltage:

- hexagon = 0.637 $V_{DC}$
- dodecagon = 0.659 $V_d$
- same max voltage => $V_d$ = 0.966$V_{DC}$

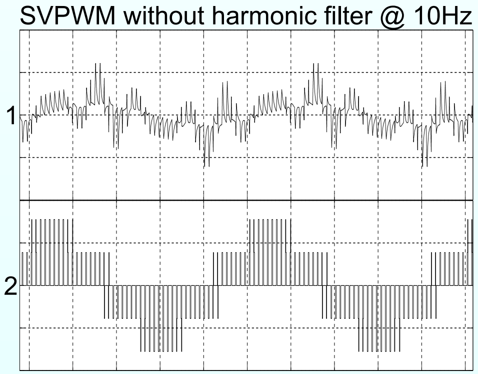
Maximum voltage at end of linear modulation:

- hexagon = $V_{DC}$ cos(pi/6)
- dodecagon = $V_d$ cos(pi/12)
- difference = 0.067

# Simulation Results - Phase Voltage & Current

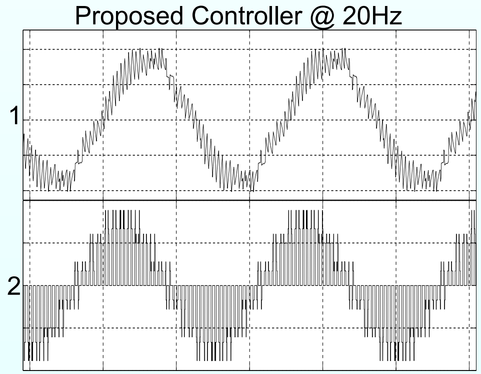



1:Phase Current (1 A/div),
2:Phase Voltage (100 V/div)

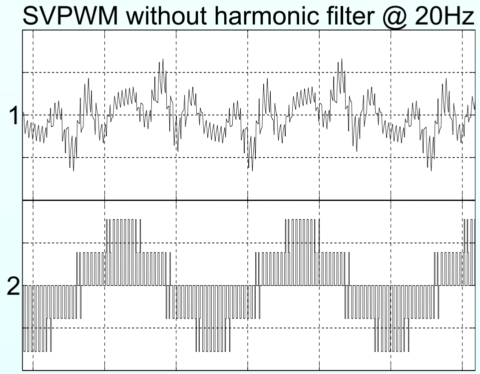



1:Phase Current (5 A/div),
2:Phase Voltage (100 V/div)

10Hz steady state, x-axis 20ms/div

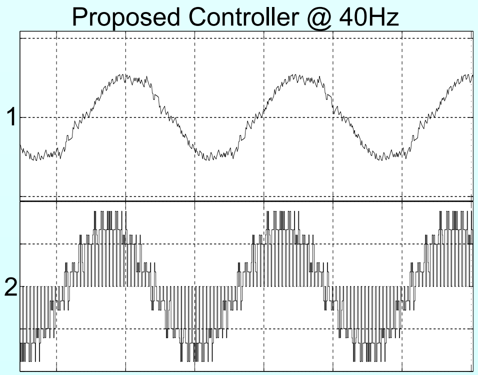



1:Phase Current (1 A/div),
2:Phase Voltage (100 V/div)

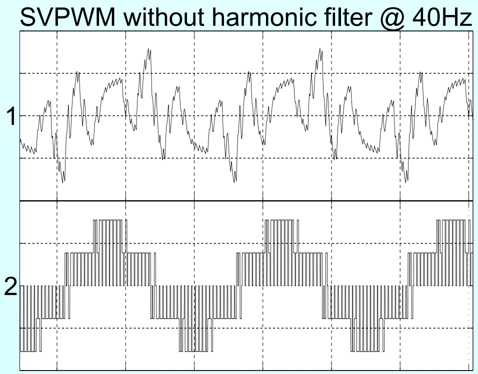



1:Phase Current (5 A/div),
2:Phase Voltage (100 V/div)

20Hz steady state, x-axis 20ms/div

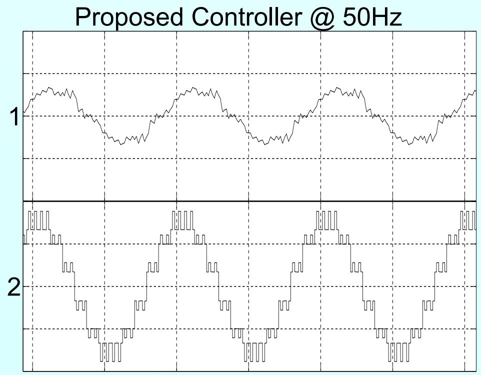



1:Phase Current (5 A/div),
2:Phase Voltage (100 V/div)

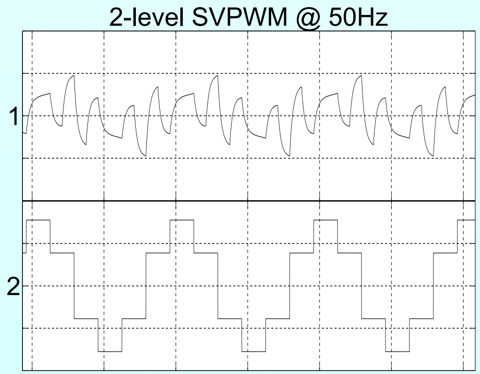



1:Phase Current (5 A/div),
2:Phase Voltage (100 V/div)

40Hz steady state, x-axis 10ms/div




1:Phase Current (5 A/div),
2:Phase Voltage (100 V/div)

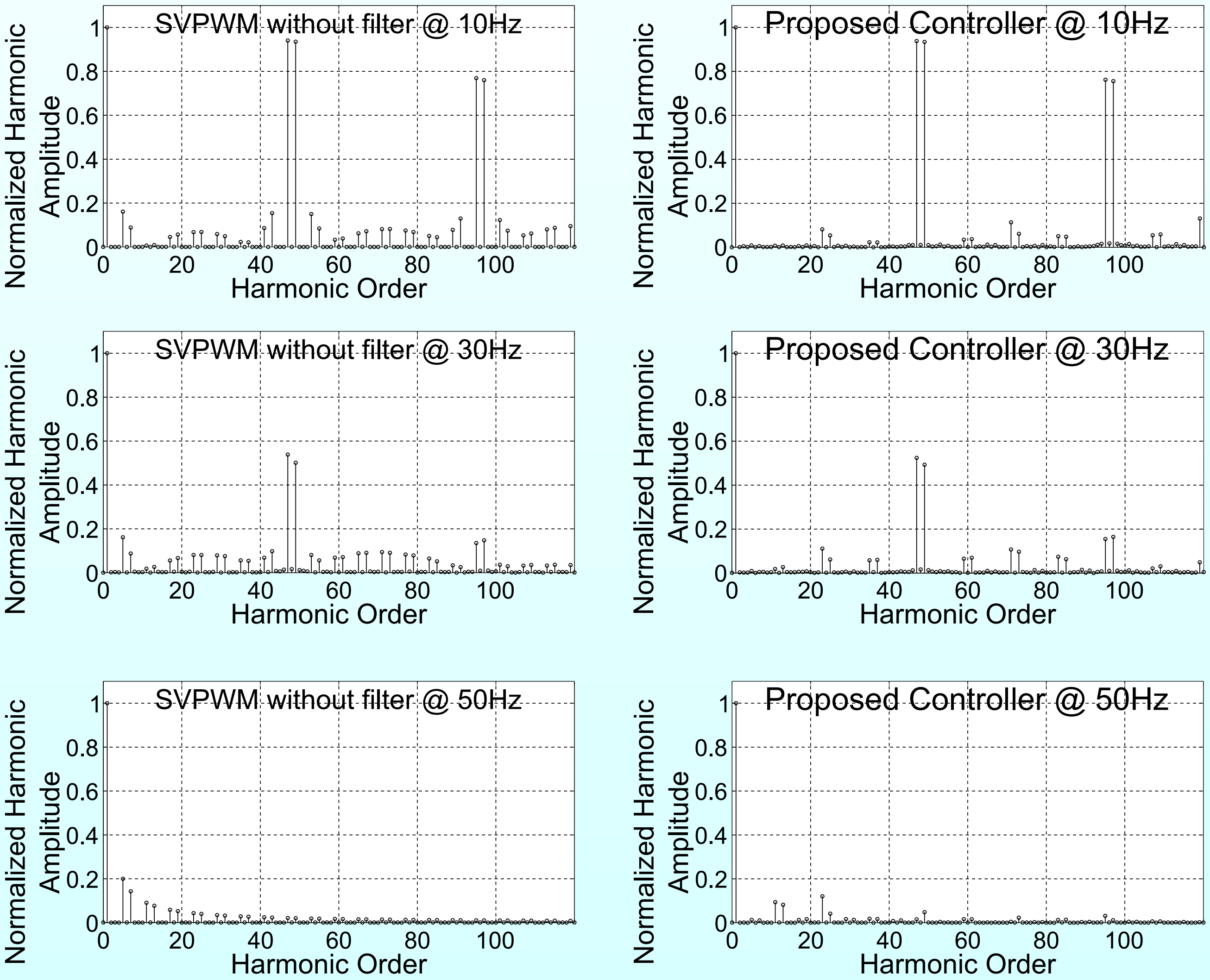



1:Phase Current (10 A/div),
2:Phase Voltage (100 V/div)

50Hz steady state, x-axis 5ms/div

# Simulation Results

## Normalized Harmonic Spectrum (FFT) of phase Voltage




@10Hz

@30Hz

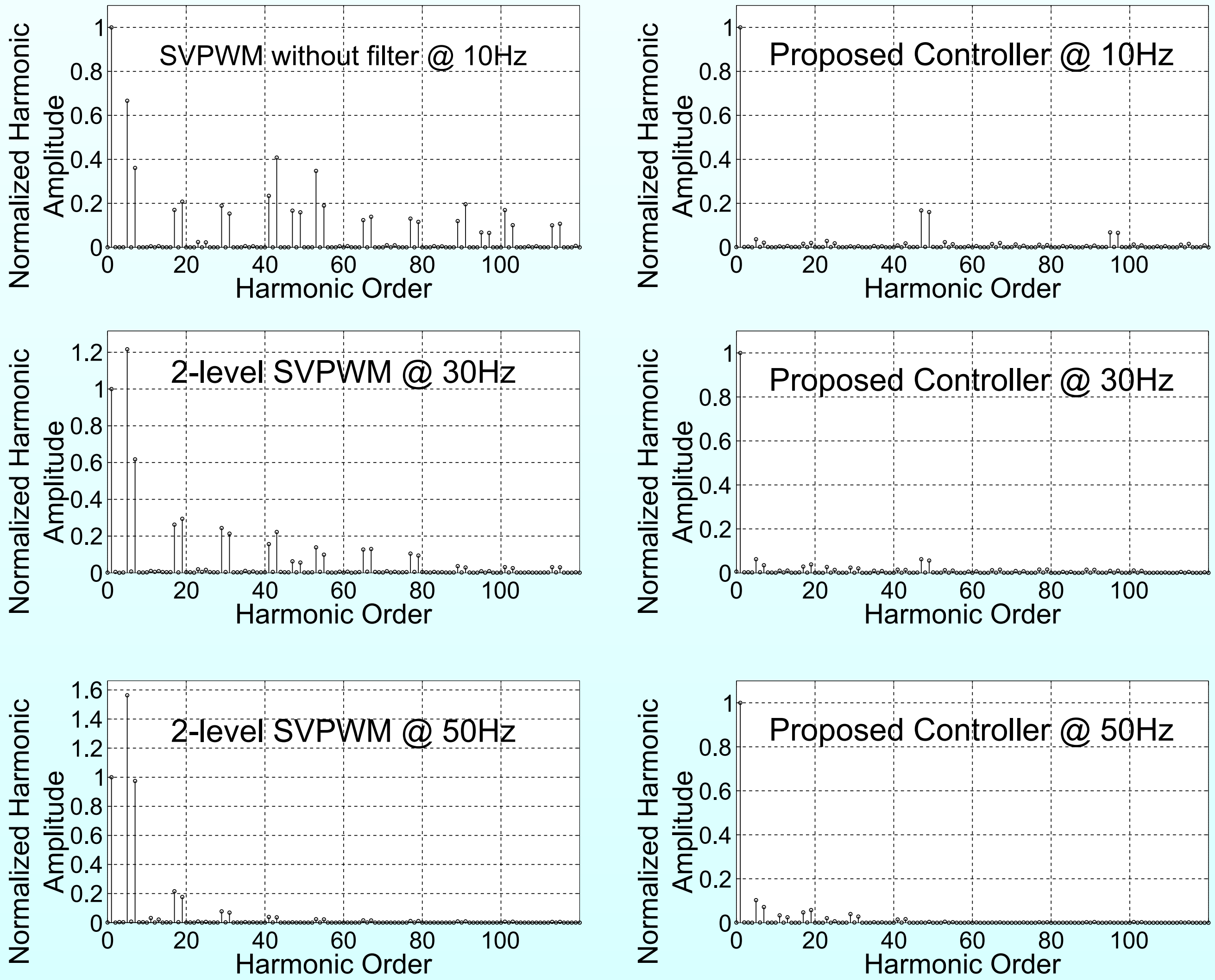
@50Hz

VC-SVPWM

Proposed Controller

# Simulation Results

## Normalized Harmonic Spectrum (FFT) of phase current




@10Hz

@30Hz

@50Hz

VC-SVPWM

Proposed Controller