Reduced Switch Count Multilevel Inverter Topologies for Open End Induction Motor Drives

Gopakumar

DESE, Indian Institute of Science

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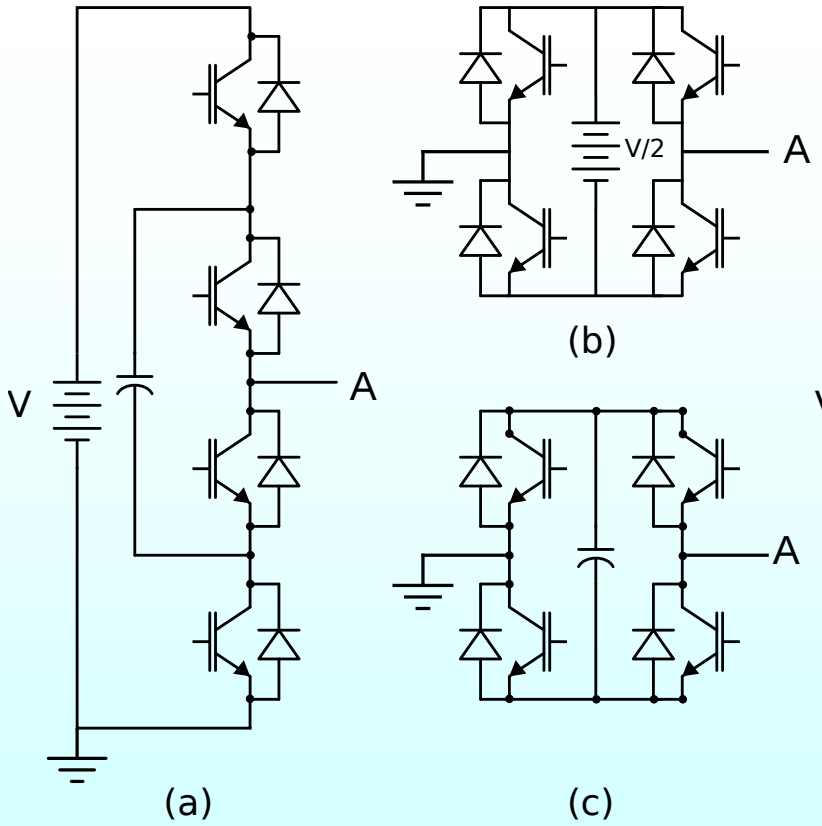
Introduction

Multilevel converters

Advantages of **multilevel voltage output** over conventional two level voltage output:

- Lower dV/dt
- Lower harmonics
- Reduced torque ripple
- Improved EMI/EMC performance

Existing Multilevel Inverter Topologies



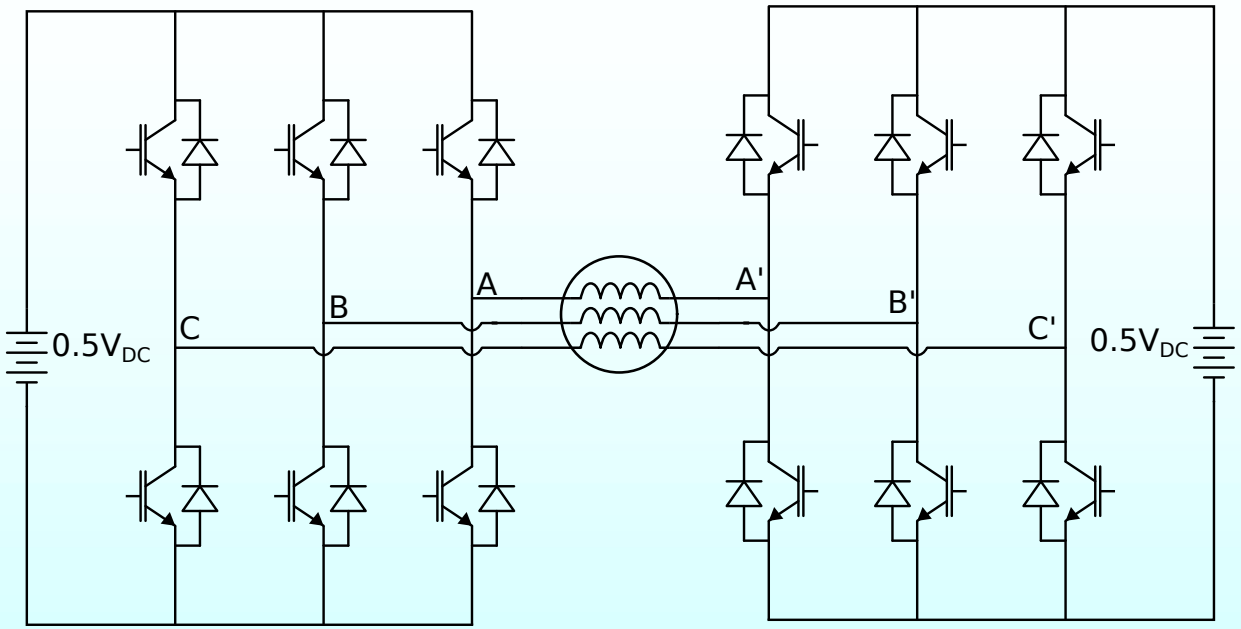
(a) Three level Flying Capacitor topology (one phase)

(b,c) Three level Cascaded H-Bridge Topology (one phase)

(d) Three level Neutral Point Clampded topology (one phase)

Open End IM Drives

Two Inverters connected to two ends of a **single IM**



Open End IM Drives

Advantages over single-ended drives:

- Single inverter replaced by **two inverters** with lower power and voltage ratings
- Possible with **any high power motor**: No modifications needed!
- **Redundancy**: reduced power **operation with one inverter** possible
- Effective multilevel output with **low switch count** (compared to single end drives)
- Ideal for **EV, traction** and general purpose drives applications

Open End IM Drives

Concerns with Open End Drives:

- **Six cables** instead of three: bad for long cable runs
- Isolated power supplies or spl. modulation required to eliminate **common mode currents**
- Both inverters must deliver power: reverse power flow can cause **DC bus overcharging**.

Contributions of the Thesis I

1. Two **low switch count** inverter topologies for open-end IM drives:
   - **Nine-level** inverter with 8 Switches per phase
   - **Seventeen-level** inverter with 12 Switches per phase
   - Both powered by two asymmetric, isolated DC links

2. **Switching state control** for both topologies to ensure:
   - All floating **capacitor voltages** are tightly controlled at switching frequency
   - No common mode currents or **DC bus overcharging**.

3. Level Shifted Carrier based **PWM scheme** with:
   - Only sampled reference magnitudes
   - Synchronous PWM over full modulation range

Contributions of the Thesis II

4. Elimination of **Dead time transients**:
   - **Digital state machine** to eliminate pole voltage transient during dead time
   - Programmatic **VHDL code generation** for FPGA deployment

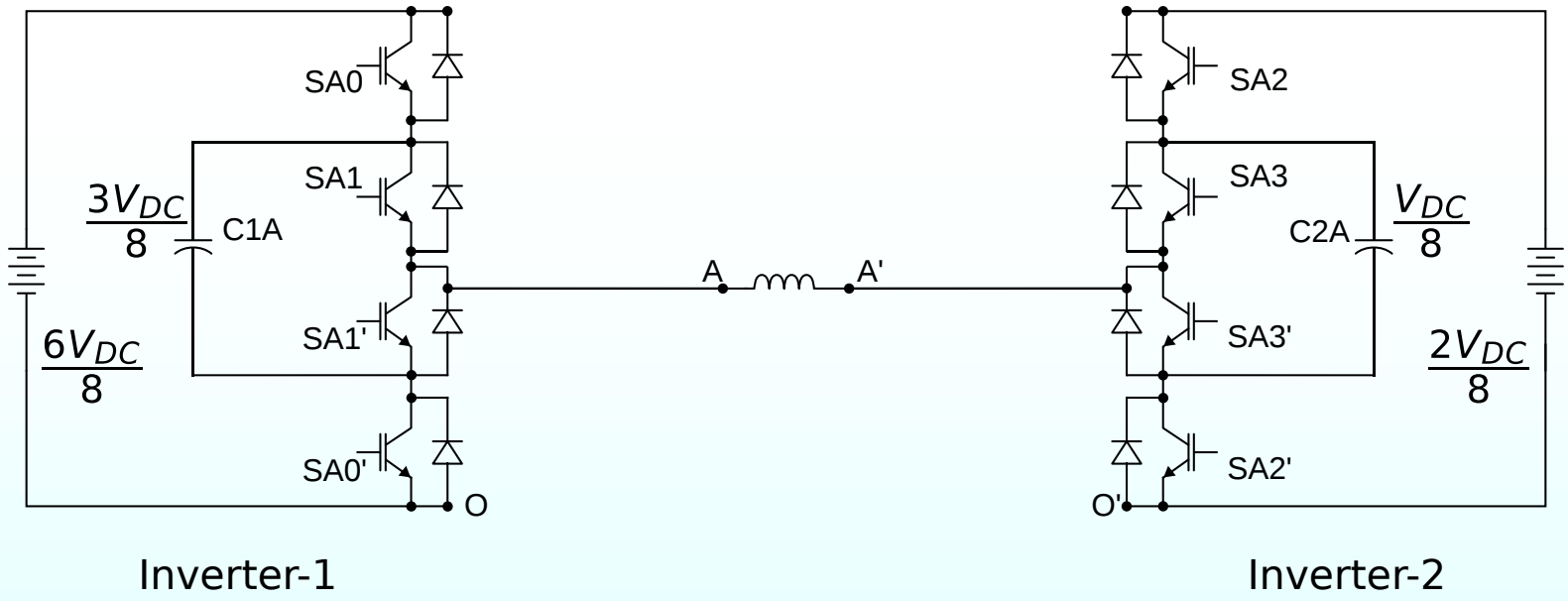
5. **Modelling** and Simulation using MATLAB/Simulink

6. **Experimental verification**:
   - On a 400V 1.1KW induction motor
   - Steady state and transient operation

Nine Level Inverter Topology for Open End Induction Motor Drive

Power Circuit Topology

Per-phase circuit, for A-phase



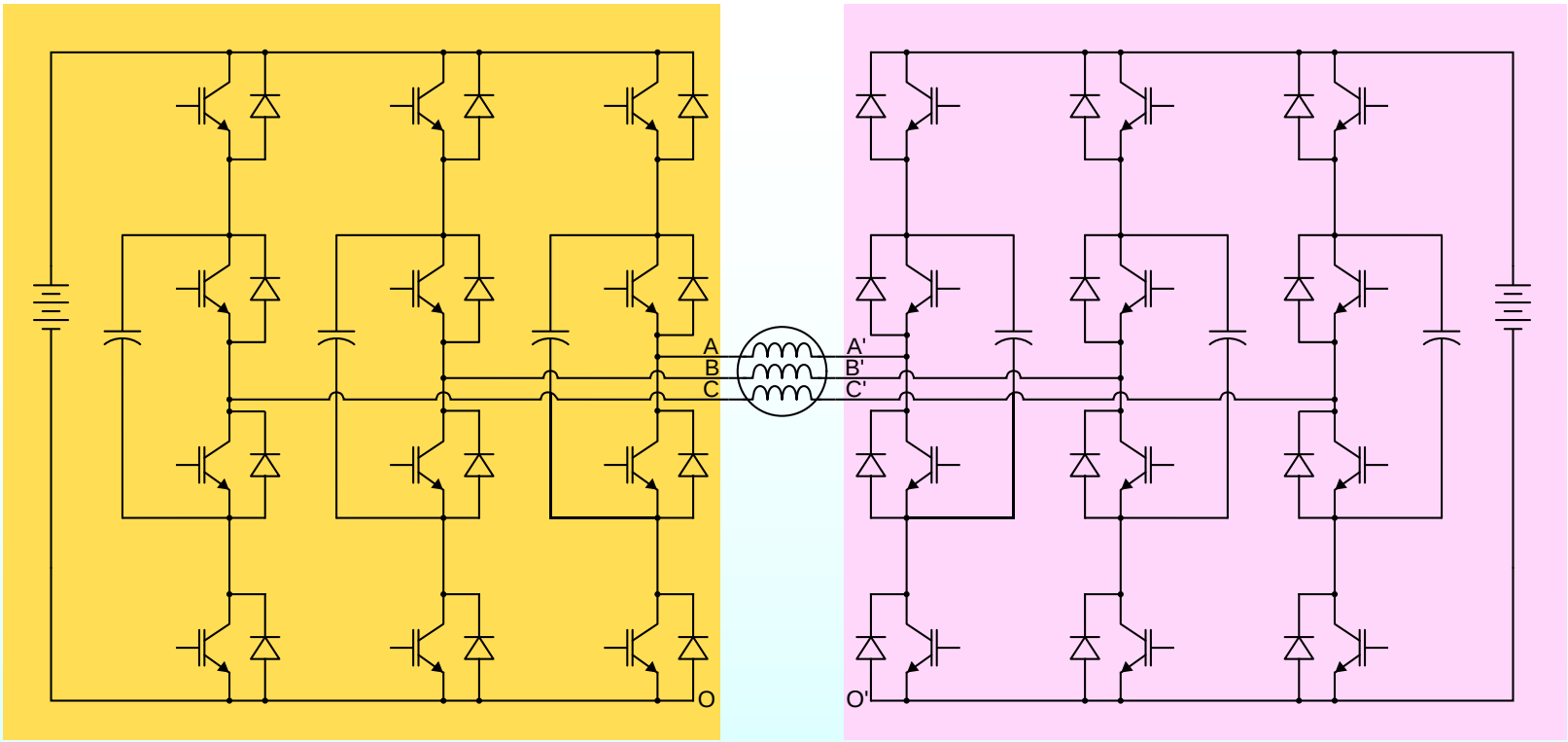
- 2 Three-Level Inverters

- 8 Switches per phase:
  Complementary pairs (SA0, SA0'), (SA1, SA1'), ...

- 2 DC capacitors per phase:
  C1A and C2A

Power Circuit Topology

(For all phases)



- Two 3-level inverters

Power Circuit Topology

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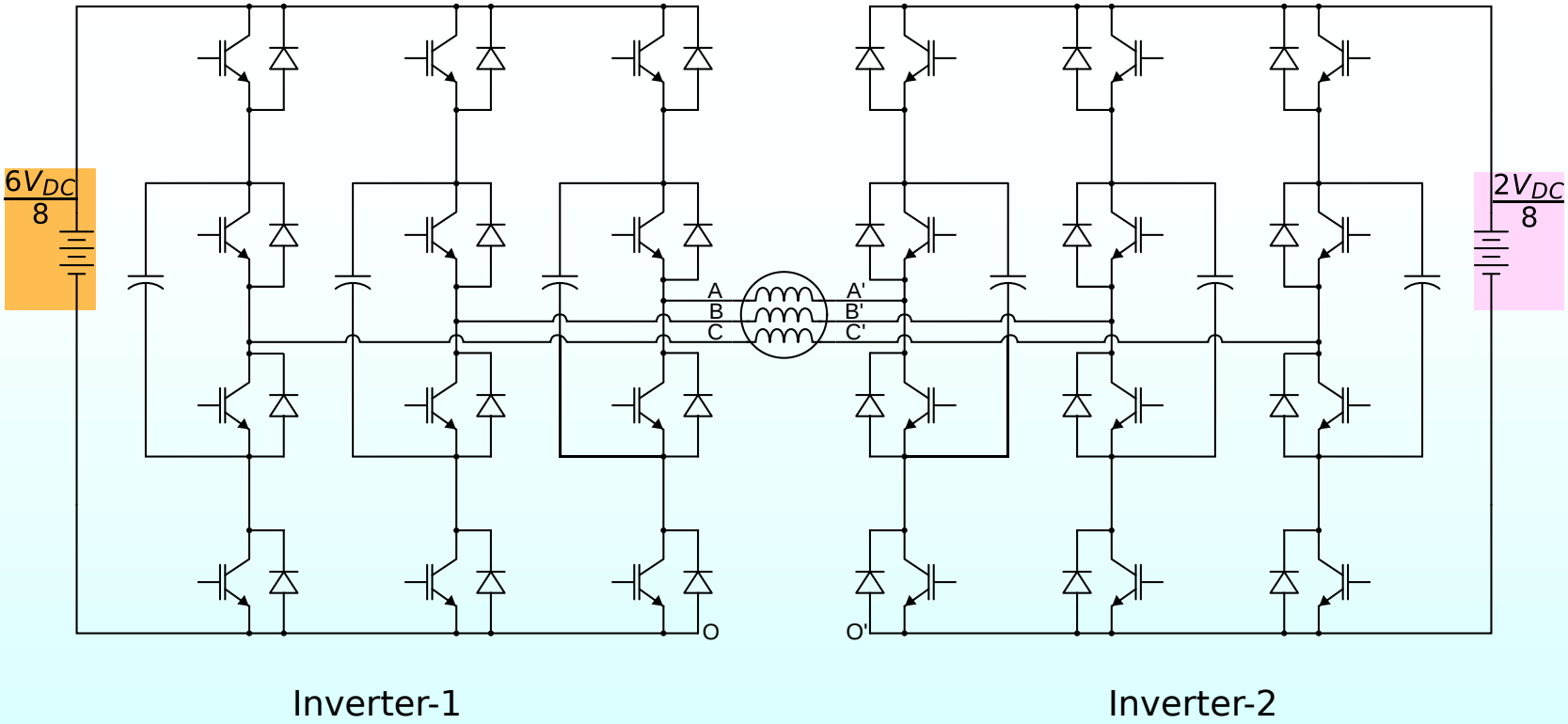

- Two 3-level inverters
- DC Supplies of $6V_{DC}/8$ and $2V_{DC}/8$

Power Circuit Topology

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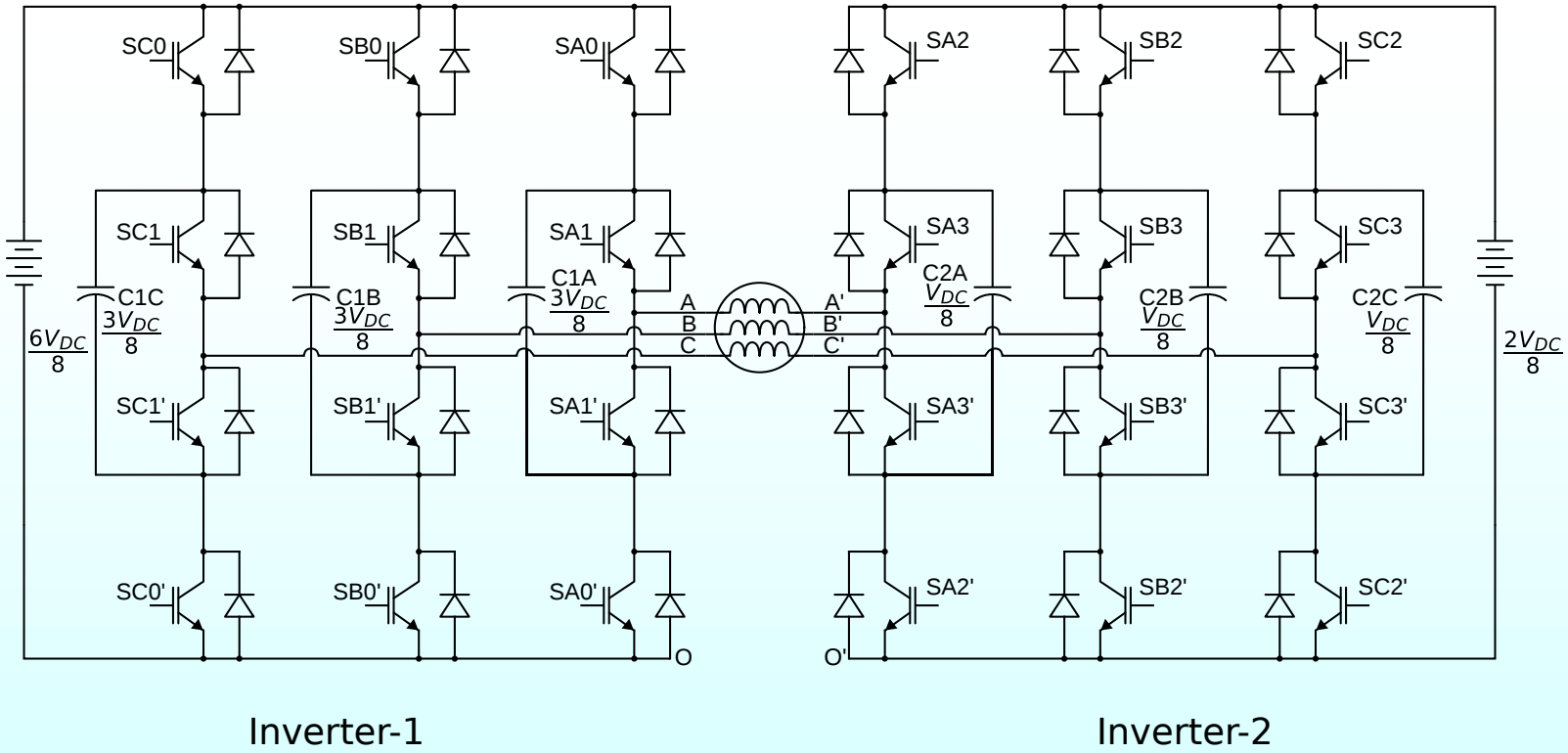
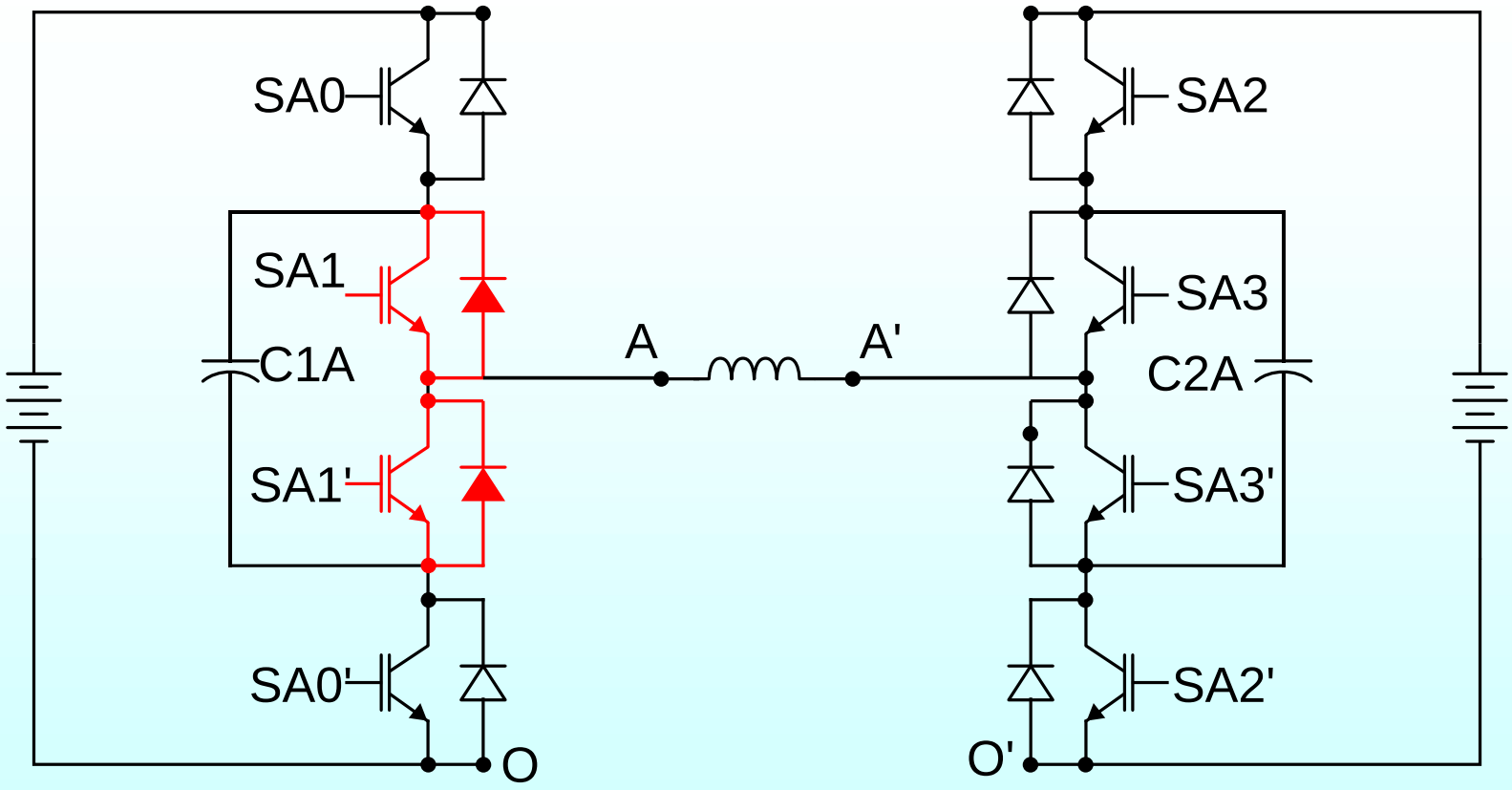


- Two 3-level inverters
- DC Supplies of $6V_{DC}/8$ and $2V_{DC}/8$
- 8 switches, 2 capacitors per phase

Complementary Switch Pairs

Each arm consists of two complementary switch pairs.



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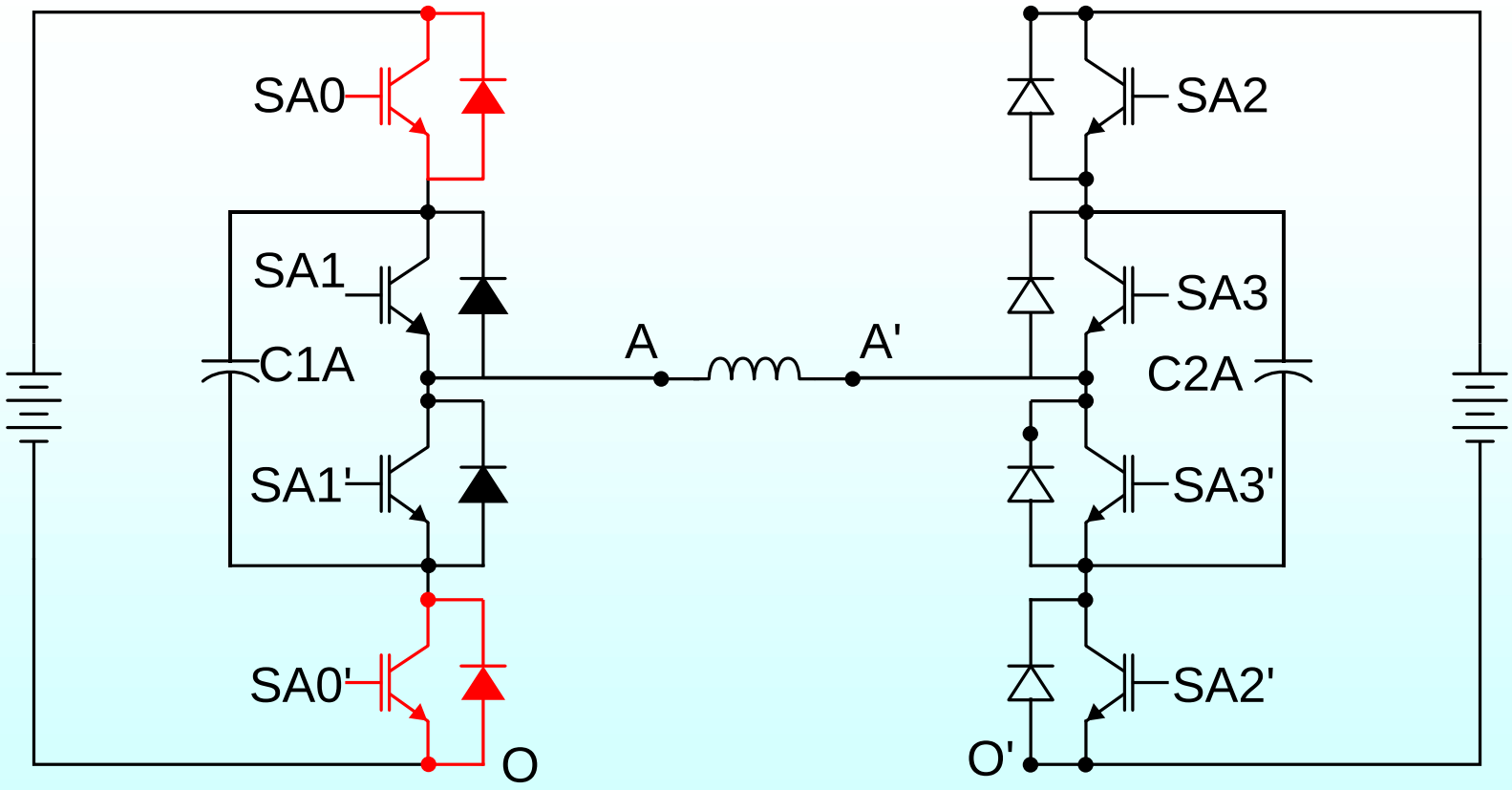
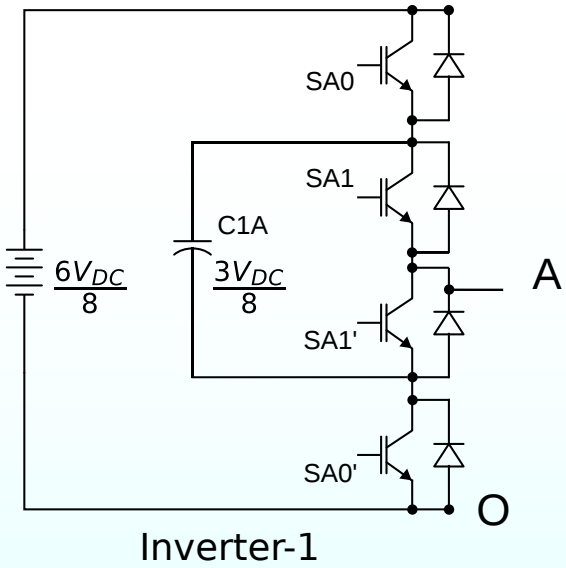
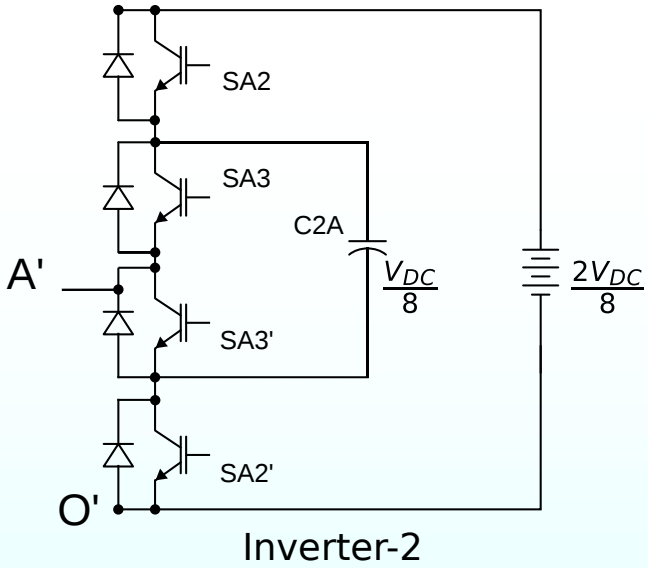


Voltage Levels

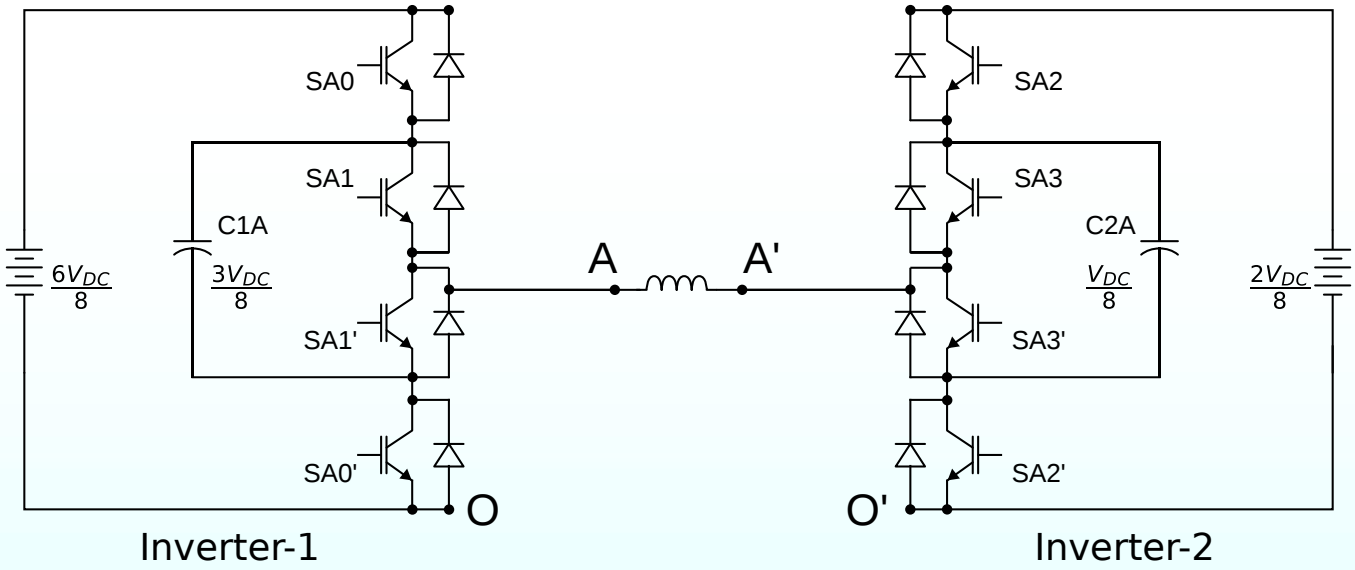




- Inverter-1 output (V_{AO}) can be:
  - $6V_{DC}/8$
  - $3V_{DC}/8$
  - 0

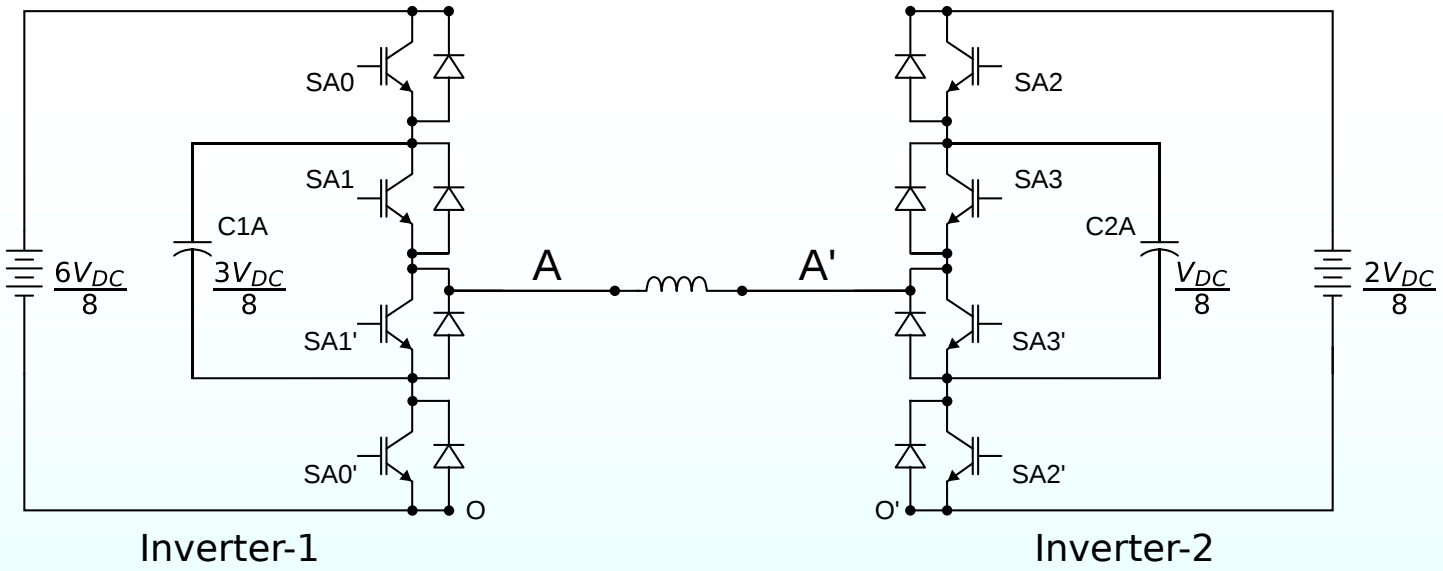
- Inverter-2 output ($V_{A'O'}$) can be:
  - $2V_{DC}/8$
  - $V_{DC}/8$
  - 0

Voltage Levels



- Motor phase voltage $V_{AA'} = V_{AO} - V_{A'O'}$

Voltage Levels

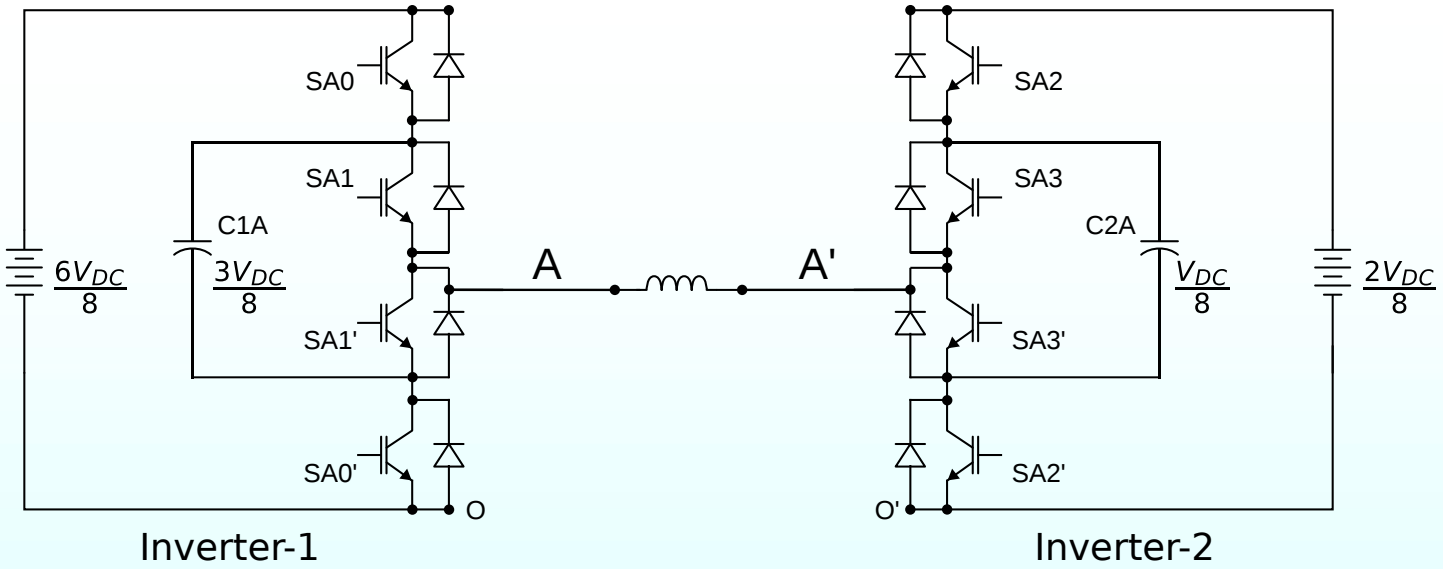


- $\mathbf{V_{AA'}}$ can have **nine** values:

$-2V_{DC}/8$ $(0 - 2V_{DC}/8)$	$+V_{DC}/8$ $(3V_{DC}/8 - 2V_{DC}/8)$	$+4V_{DC}/8$ $(6V_{DC}/8 - 2V_{DC}/8)$
$-V_{DC}/8$ $(0 - V_{DC}/8)$	$+2V_{DC}/8$ $(3V_{DC}/8 - V_{DC}/8)$	$+5V_{DC}/8$ $(6V_{DC}/8 - V_{DC}/8)$
-0 $(0 - 0)$	$+3V_{DC}/8$ $(3V_{DC}/8 - 0)$	$+6V_{DC}/8$ $(6V_{DC}/8 - 0)$

Phase Voltage Levels

A **unique pole voltage combination** for each phase voltage level



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- 0	(0 - 0)	$+3V_{DC}/8$	$(3V_{DC}/8 - 0)$	$+6V_{DC}/8$	$(6V_{DC}/8 - 0)$

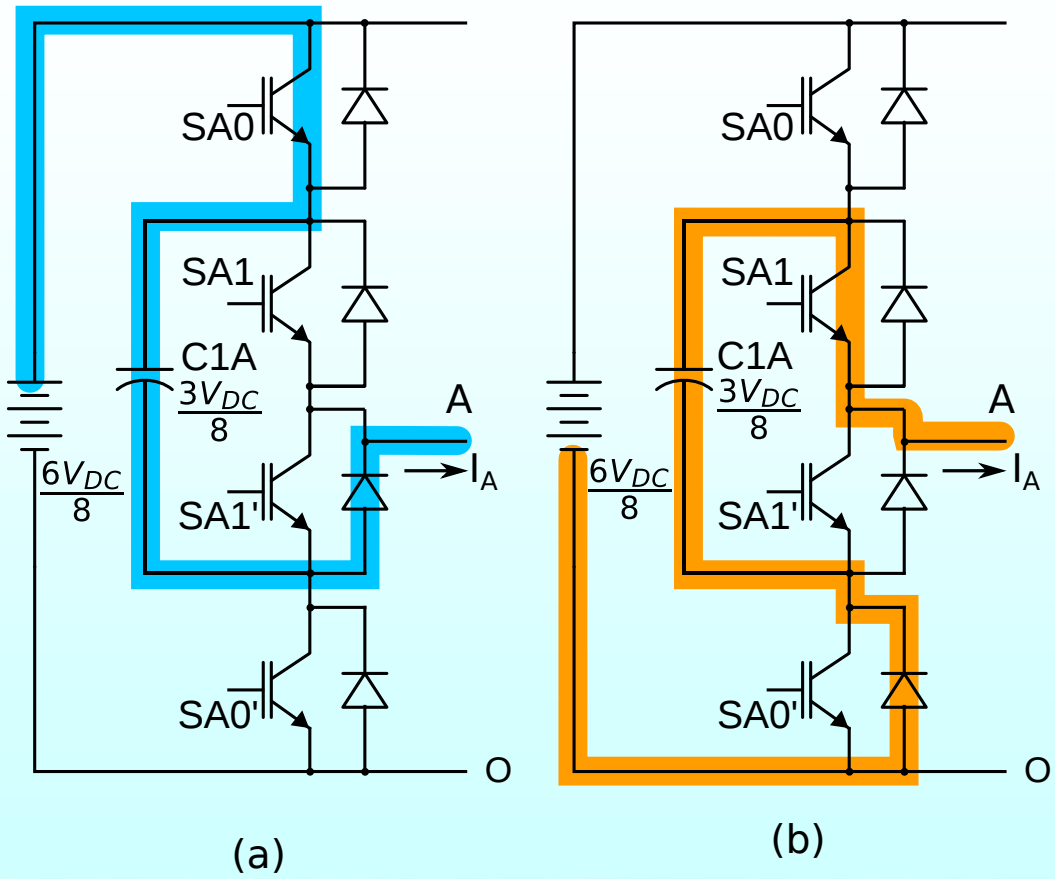
Phase voltage levels

Level	$\mathbf{V_{AA'}}$	$\mathbf{V_{AO}}$	$\mathbf{V_{A'O'}}$
0	$-2V_{DC}/8$	0	$2V_{DC}/8$
1	$-V_{DC}/8$	0	$V_{DC}/8$
2	0	0	0
3	$V_{DC}/8$	$3V_{DC}/8$	$2V_{DC}/8$
4	$2V_{DC}/8$	$3V_{DC}/8$	$V_{DC}/8$
5	$3V_{DC}/8$	$3V_{DC}/8$	0
6	$4V_{DC}/8$	$6V_{DC}/8$	$2V_{DC}/8$
7	$5V_{DC}/8$	$6V_{DC}/8$	$V_{DC}/8$
8	$6V_{DC}/8$	$6V_{DC}/8$	0

Table 1 : $V_{AA'}$ values for all possible combinations of V_{AO} and $V_{A'O'}$

Switching Redundancies for Capacitor Balancing

Switching states for Pole voltage $3V_{DC}$:
(a) C1A charging
(b) C1A discharging



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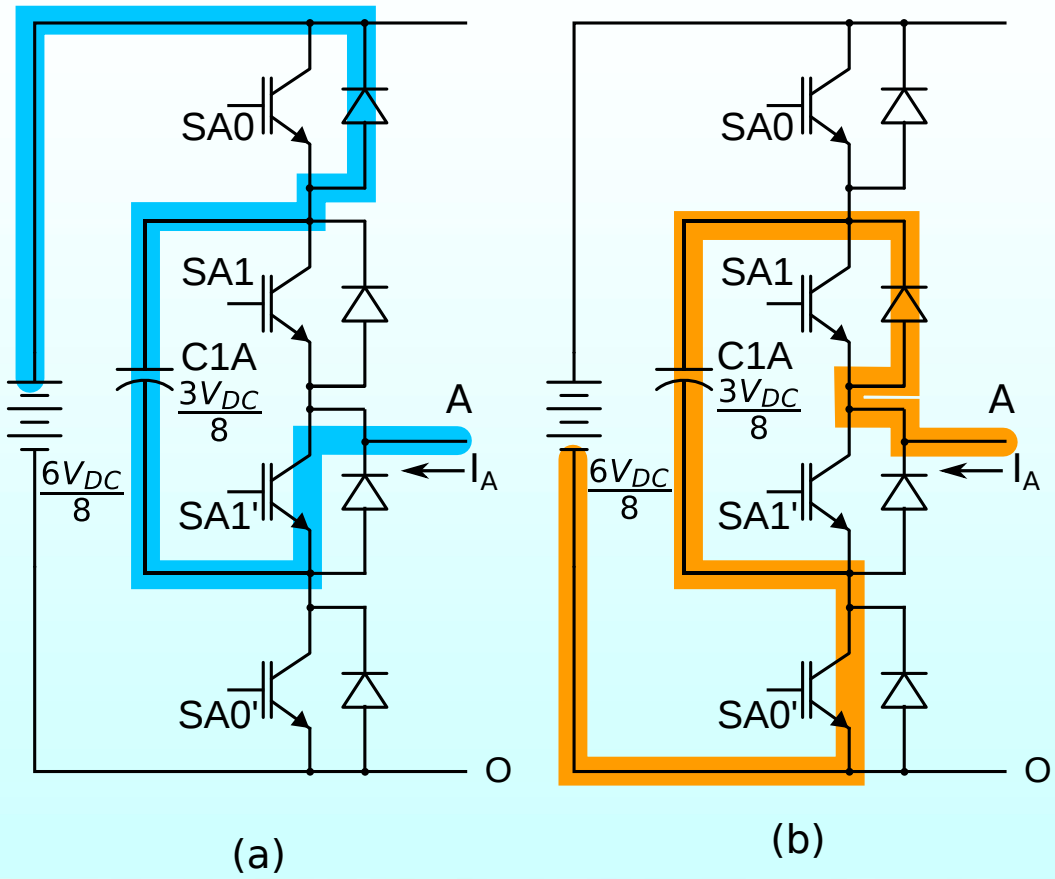

Capacitor Balancing

All floating caps can be balanced by selecting **appropriate switching state**:

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- Capacitors see **switching freq.** currents (not fundamental current)

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- Independent of **current direction**
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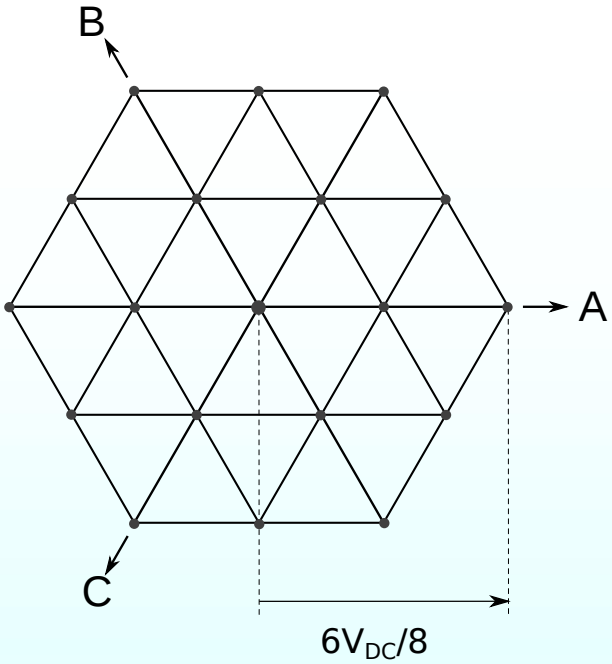
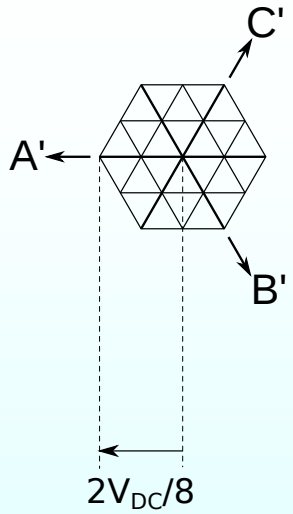
- No Precharging required at **startup**
- Switching state choice updated in **every switching period**
- Capacitors see **switching freq.** currents (not fundamental current)
- Leads to **low capacitance** requirement

Space-vector diagrams

Space-Vector Diagrams for individual inverters



Inverter-1
3L-space vector structure

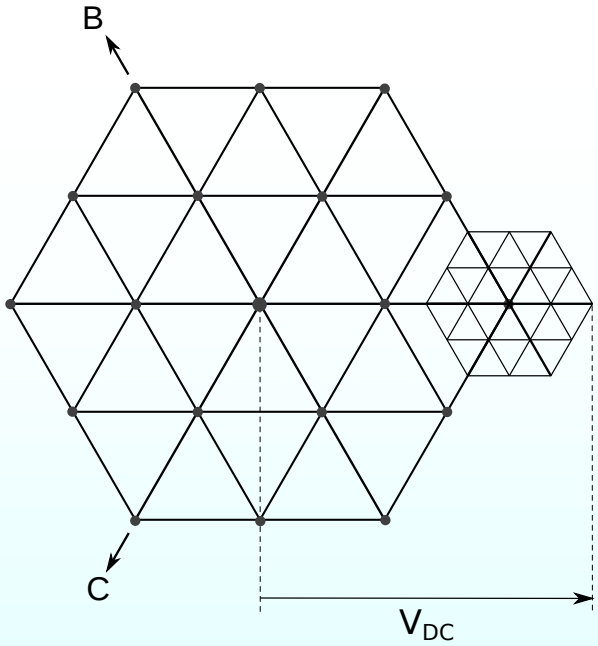


Inverter-2
3L-space vector structure

- Radii of hexagons in 3:1 ratio
- Inverter-2 axes (A'B'C') opposing inverter-1 (A,B,C)

Superposition of Space-vector diagrams

generating effective space vector structure



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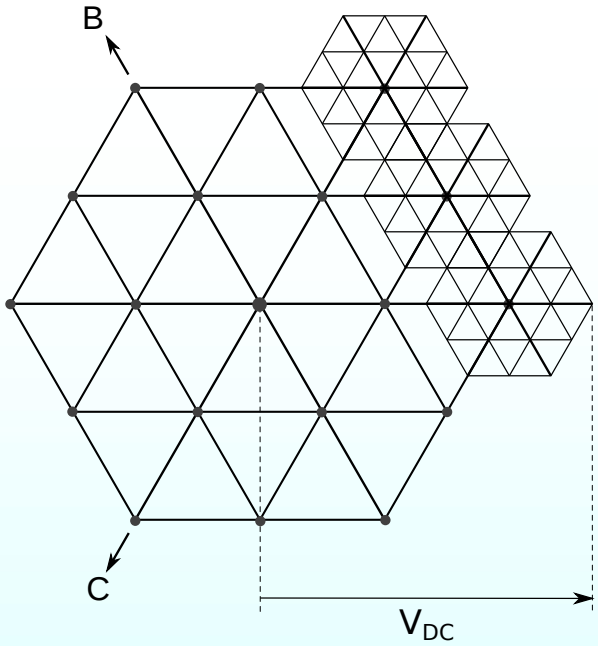

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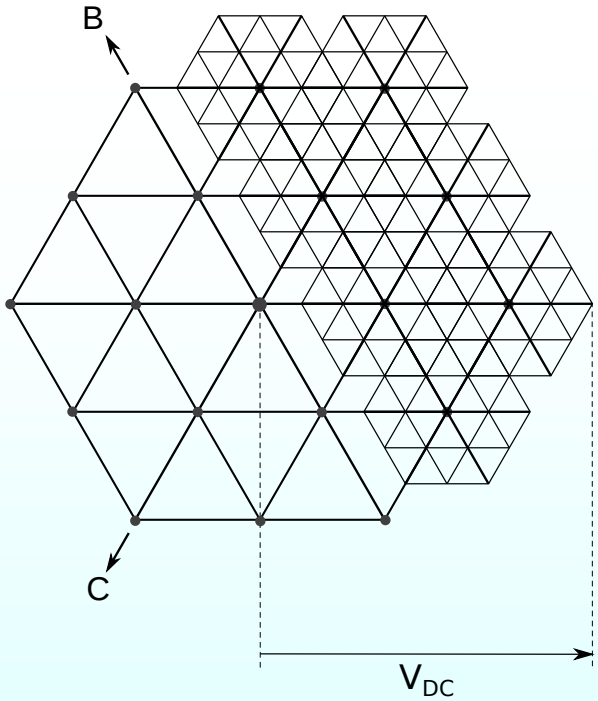

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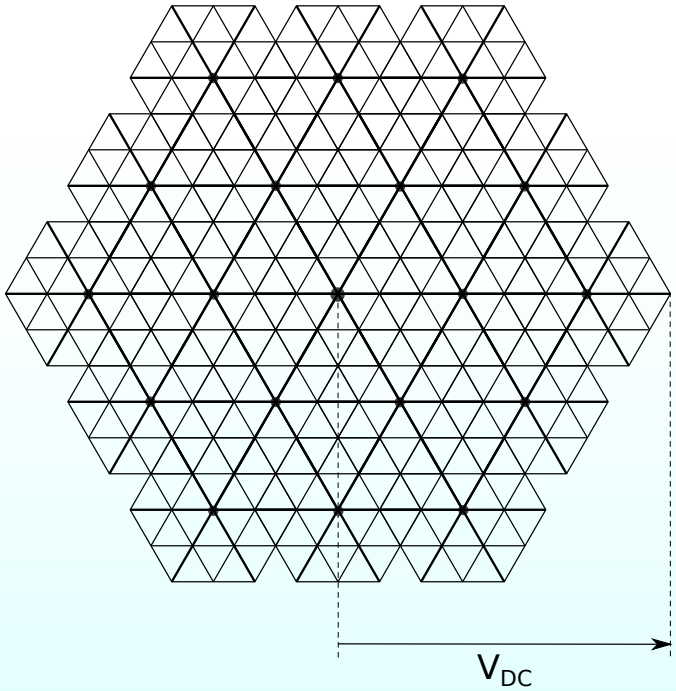

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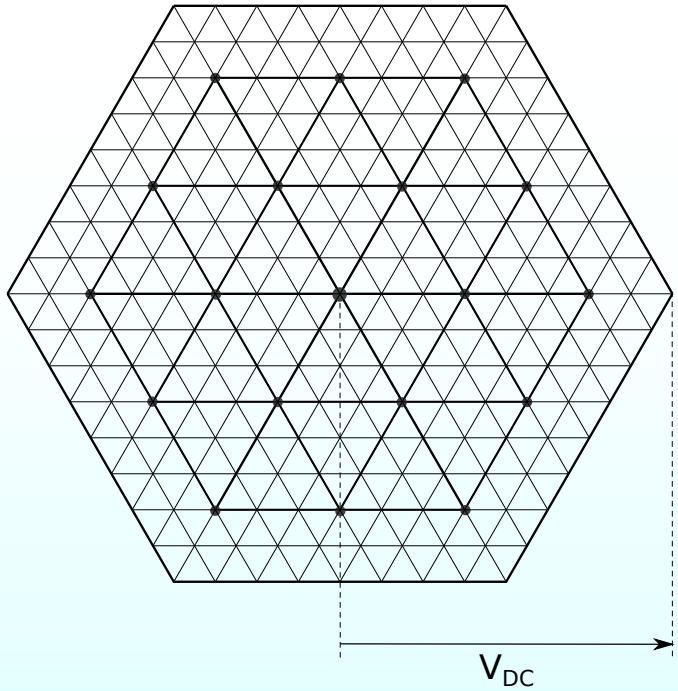

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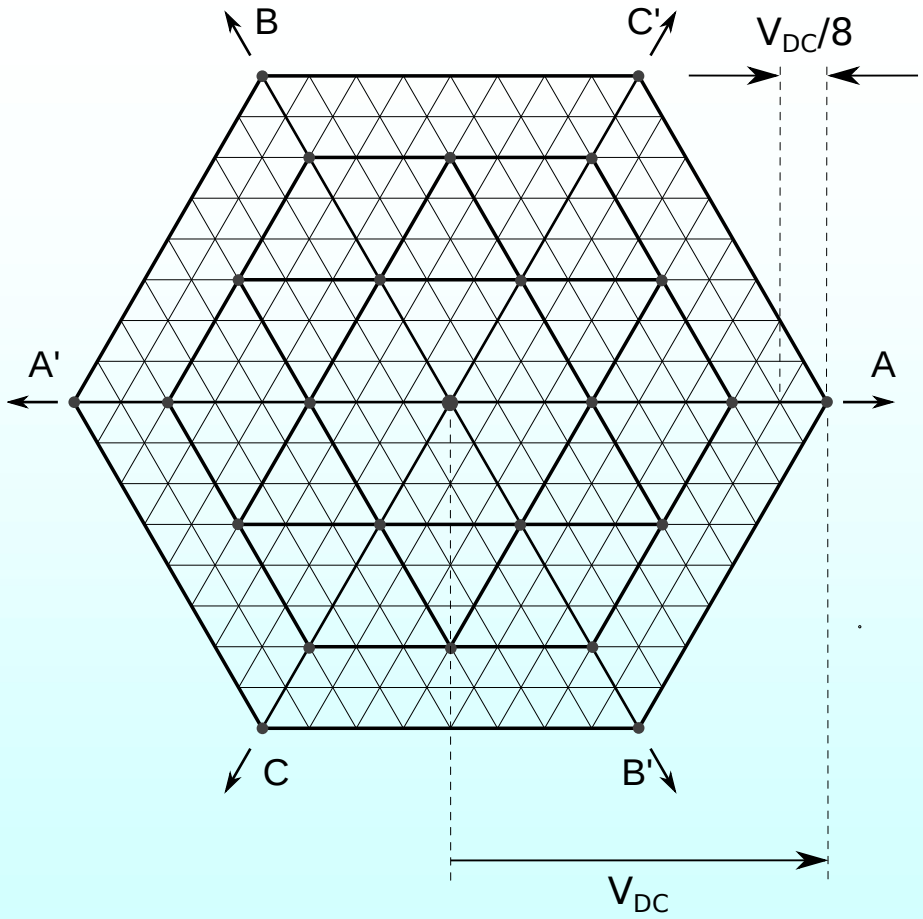
Effective space-vector structure

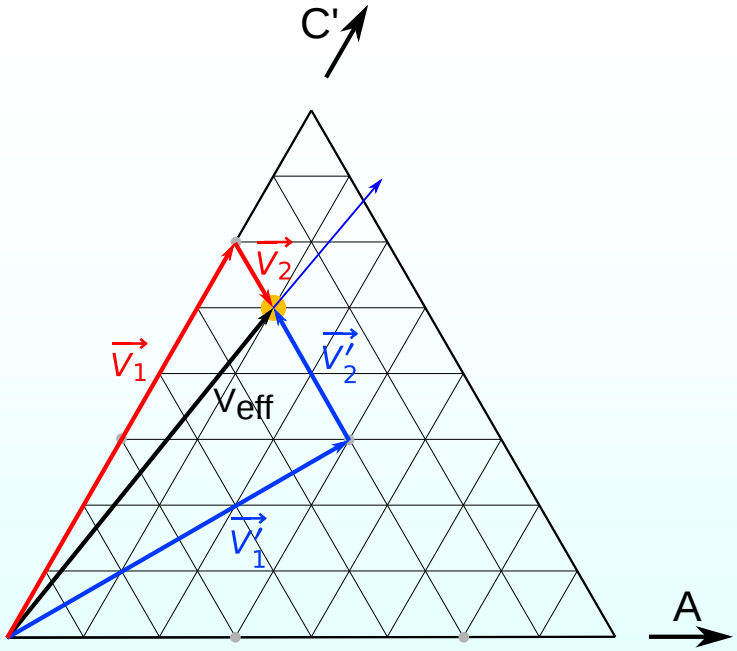
of proposed 9L inverter



- 3^6=729 pole voltage combinations
- 217 space vector locations
- Radius of outer hexagon = V_{DC}
- Smallest triangles of side $V_{DC}/8$

Space vector combinations

Determining individual inverter outputs



Different combination of vectors from Inverter-1 and Inverter-2 generate the same net space vector

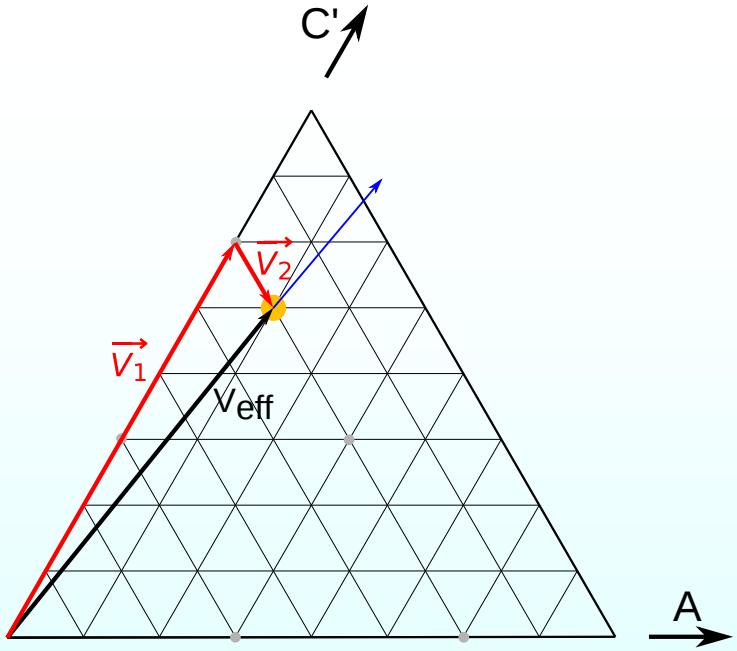
E.g. desired space vector = V_{eff}

Case 1: $\vec{V_{eff}} = \vec{V_1} + \vec{V_2}$

Case 2: $\vec{V_{eff}} = \vec{V'_1} + \vec{V'_2}$

Space vector combinations

Determining individual inverter outputs



Different combination of vectors from Inverter-1 and Inverter-2 generate the same net space vector

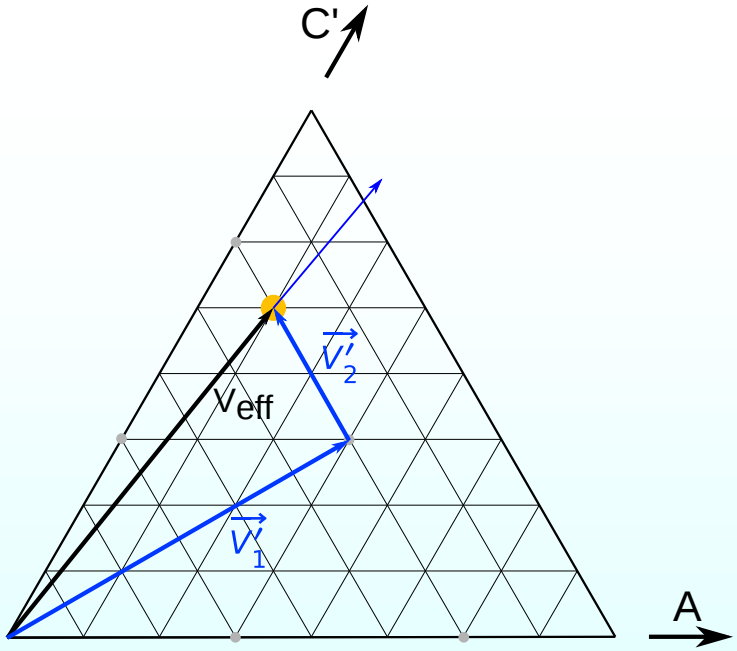
E.g. desired space vector = V_{eff}

Component of V_1 along V_{eff} is positive => Inverter1 supplies power
Component of V_2 along V_{eff} is negative => Inverter2 receives power

Results in circulating currents, overcharging of DC bus
MUST BE AVOIDED!

Space vector combinations

Determining individual inverter outputs



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E.g. desired space vector = V_{eff}

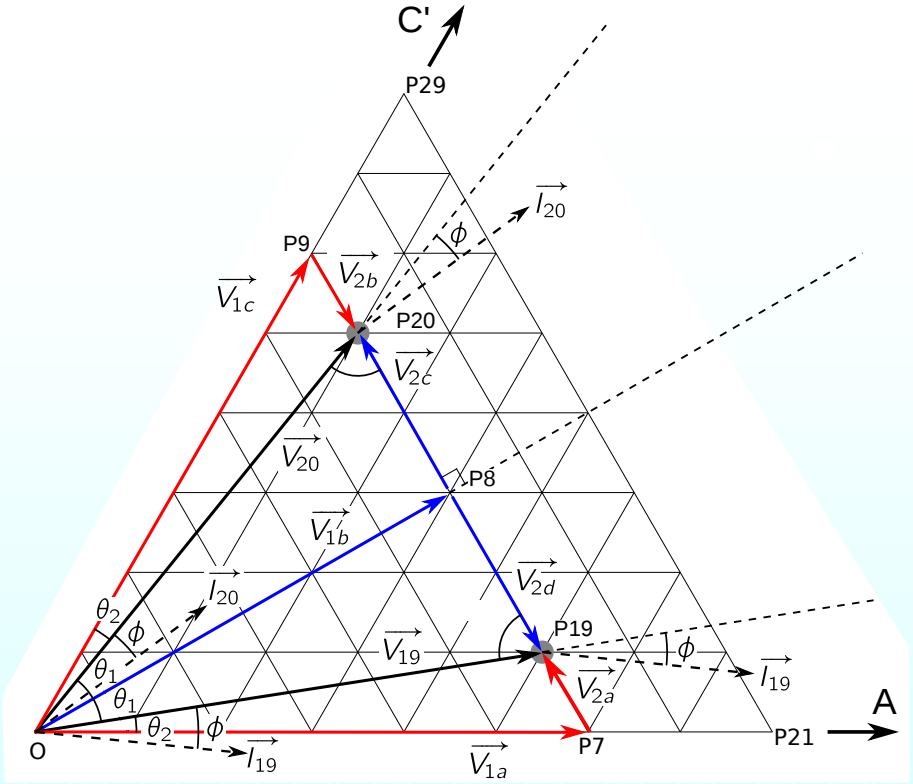
Case 2: $\overrightarrow{V_{eff}} = \overrightarrow{V_1'} + \overrightarrow{V_2'}$

Component of V1 along Veff is positive => Inverter1 supplies power
Component of V2 along Veff is positive => Inverter2 supplies power

No circulating currents, both inverters supply power
Only such states are used

Space vector combinations

Proof for steady state case



Assume:

Steady state constant frequency operation

Identical dwell times at P19 and P20

Steady lagging PF, angle ϕ

Power delivered by inverter 2 is:

$$P_a = \vec{V}_{2a} \cdot \vec{I}_{19} + \vec{V}_{2b} \cdot \vec{I}_{20}$$

OR

$$P_b = \vec{V}_{2d} \cdot \vec{I}_{19} + \vec{V}_{2c} \cdot \vec{I}_{20}$$

From geometry: $\theta_1 = 21.05°$, $\theta_2 = 8.95°$

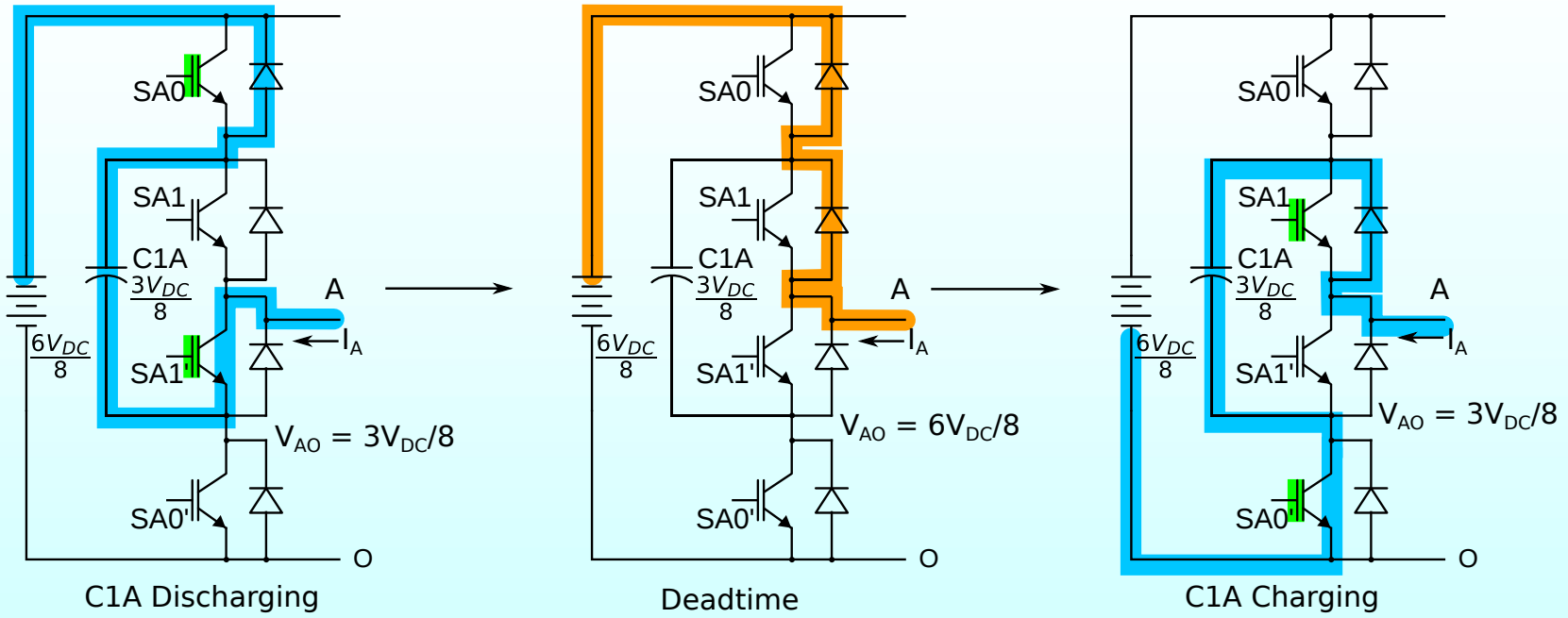
$P_a < 0$ for any power factor angle $-\pi < \phi < \pi$;

whereas

$P_b > 0$ for any power factor angle $-\pi < \phi < \pi$;

Dead-time-induced transients

During a transitions from C1 **Discharging** to C1 **Charging**, the pole voltage V_{AO} has an undesirable transient.



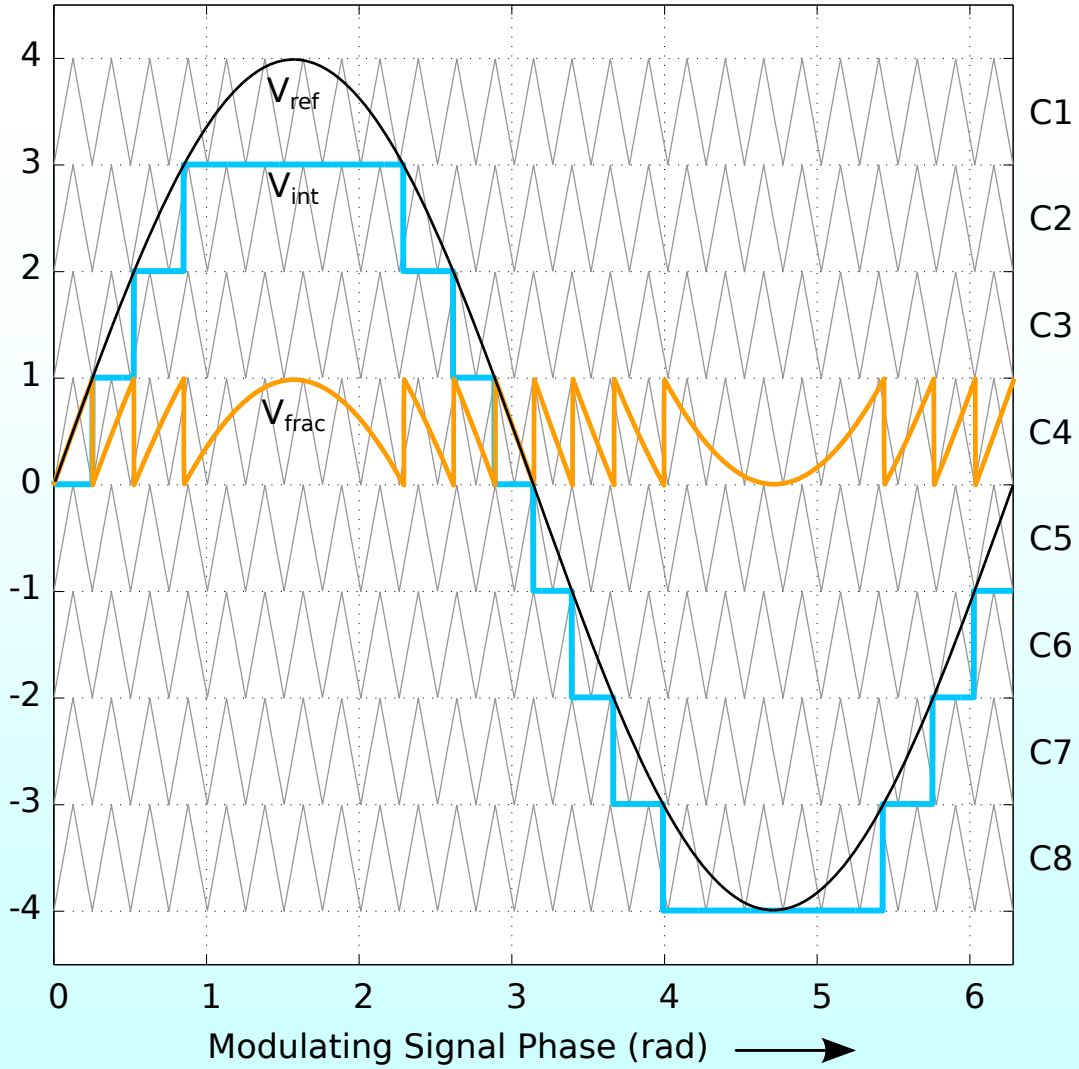
Dead-time-induced transients

- Error voltage has a magnitude of $\mathbf{3V_{DC}/8}$
- Sign depends on phase current
- Results in **distortion** in phase current
- Also causes radiated and conducted **noise**
- Can be prevented by disallowing direct transition between charging and discharging states

Modulation Scheme

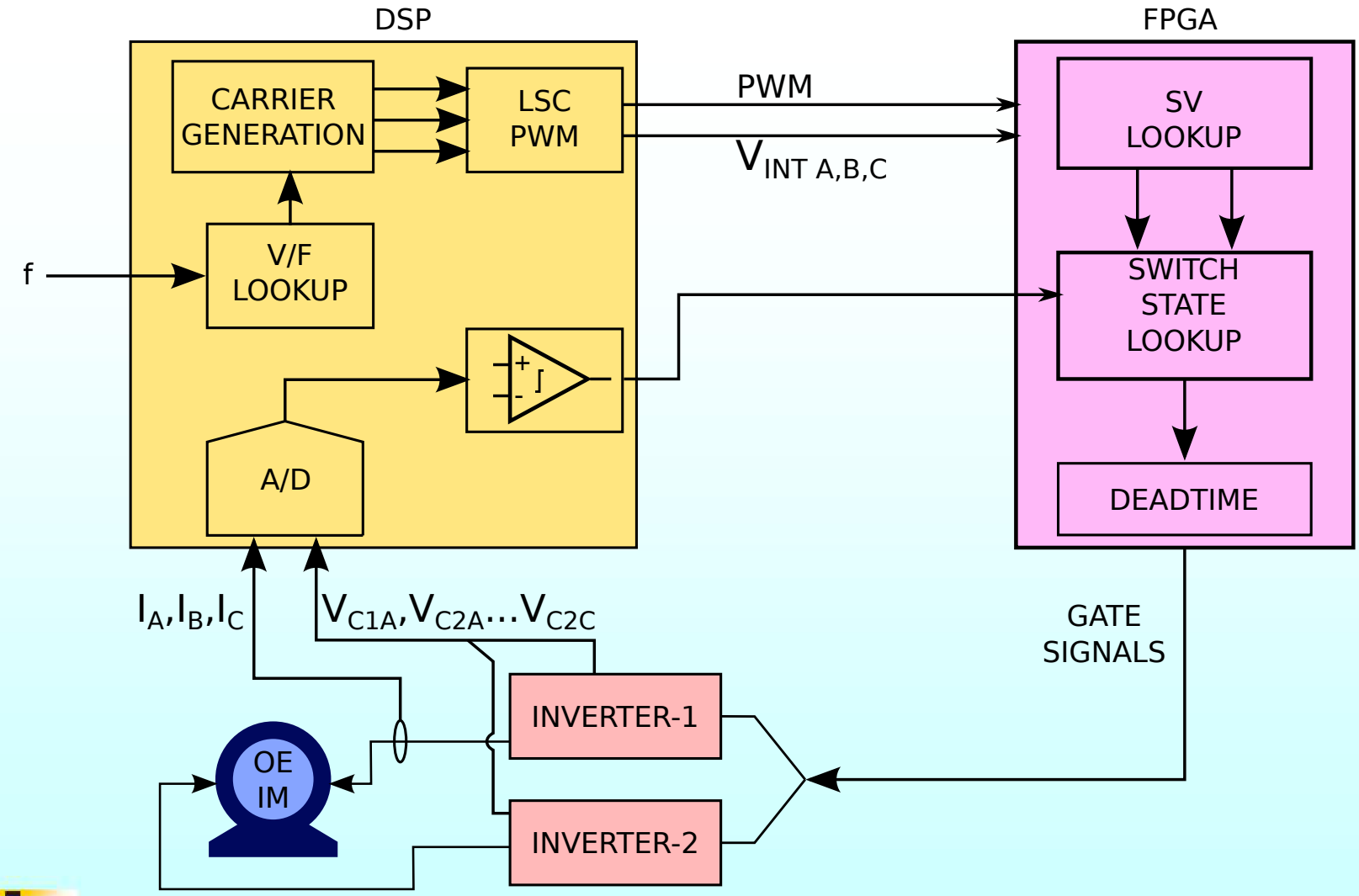
- Level-Shifted Carrier PWM based scheme
- Only instantaneous phase voltage references required
- Usable with closed loop scalar/vector control schemes
- No recursive timing calculations required
- Current direction and cap. voltages sensed once every switching period

Level-shifted carrier PWM signals



Control Scheme

System Block Diagram



Experimental Results

- Steady State operation at constant frequency (8Hz - 45Hz)
- System startup and motor acceleration
- Demonstration of capacitor re-balancing after intentional unbalancing
- Prevention of DC bus overcharging

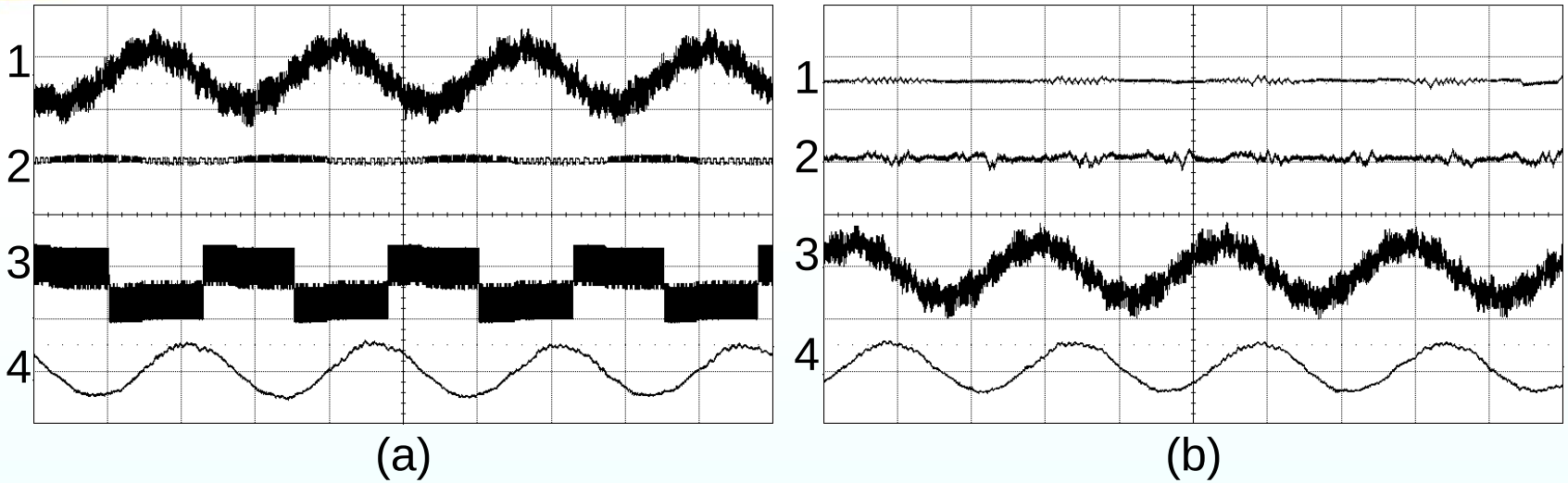


Figure 1 : Experimental results for 8Hz operation (a) Voltage and current waveforms. X-Axis: 50ms/div. (1) A-phase voltage (Y -axis: 50 V/div). (2) Inverter-1 pole voltage V_{AO} (Y -axis: 100V/div). (3) Inverter-2 pole voltage $V_{A'O'}$ (Y -axis: 50V/div). (4) A Phase current (Y -axis: 1A/div) (b) Capacitor voltage waveforms. X-Axis: 20ms/div. (1) Ripple in flying capacitor C1A, (AC coupled) (Y -axis: 5 V/div). (2) Ripple in flying capacitor C2A, (AC coupled) (Y -axis: 200mV/div). (3) A-phase voltage (Y -axis: 50 V/div). (4) A Phase current (Y -axis: 1A/div).

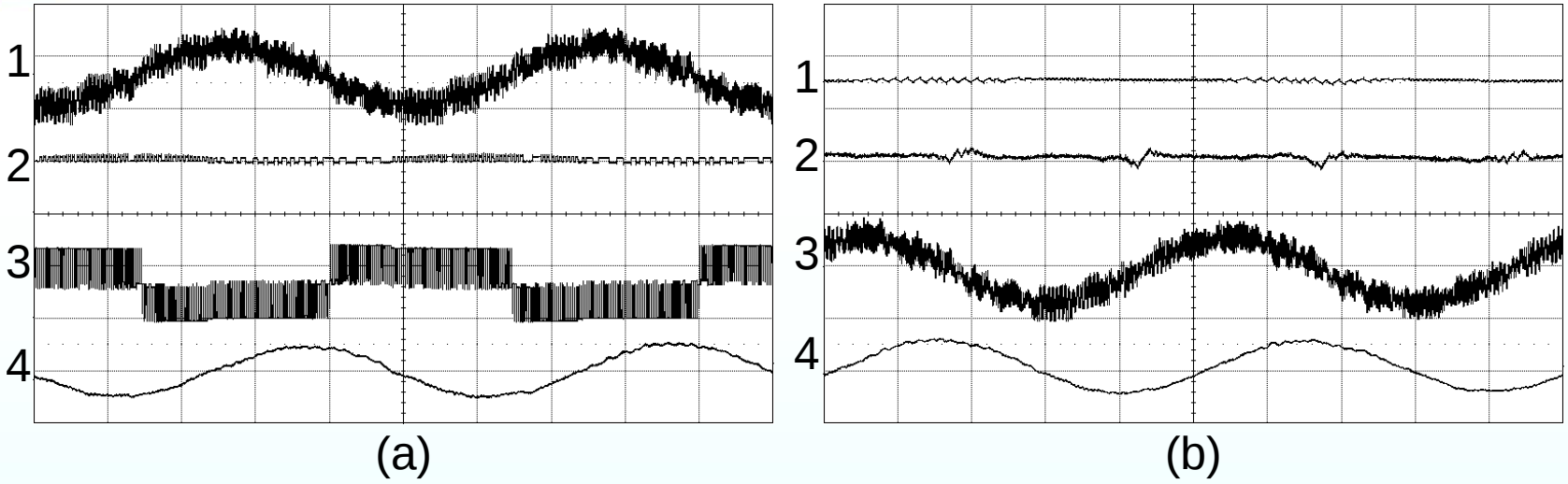


Figure 2 : Experimental results for 10Hz operation (a) Voltage and current waveforms. X-Axis: 20ms/div. (1) A-phase voltage (Y -axis: 50 V/div). (2) Inverter-1 pole voltage V_{AO} (Y -axis: 100V/div). (3) Inverter-2 pole voltage $V_{A'O'}$ (Y -axis: 50V/div). (4) A Phase current (Y -axis: 1A/div) (b) Capacitor voltage waveforms. X-Axis: 20ms/div. (1) Ripple in flying capacitor C1A, (AC coupled) (Y -axis: 5 V/div). (2) Ripple in flying capacitor C2A, (AC coupled) (Y -axis: 200mV/div). (3) A-phase voltage (Y -axis: 50 V/div). (4) A Phase current (Y -axis: 1A/div).

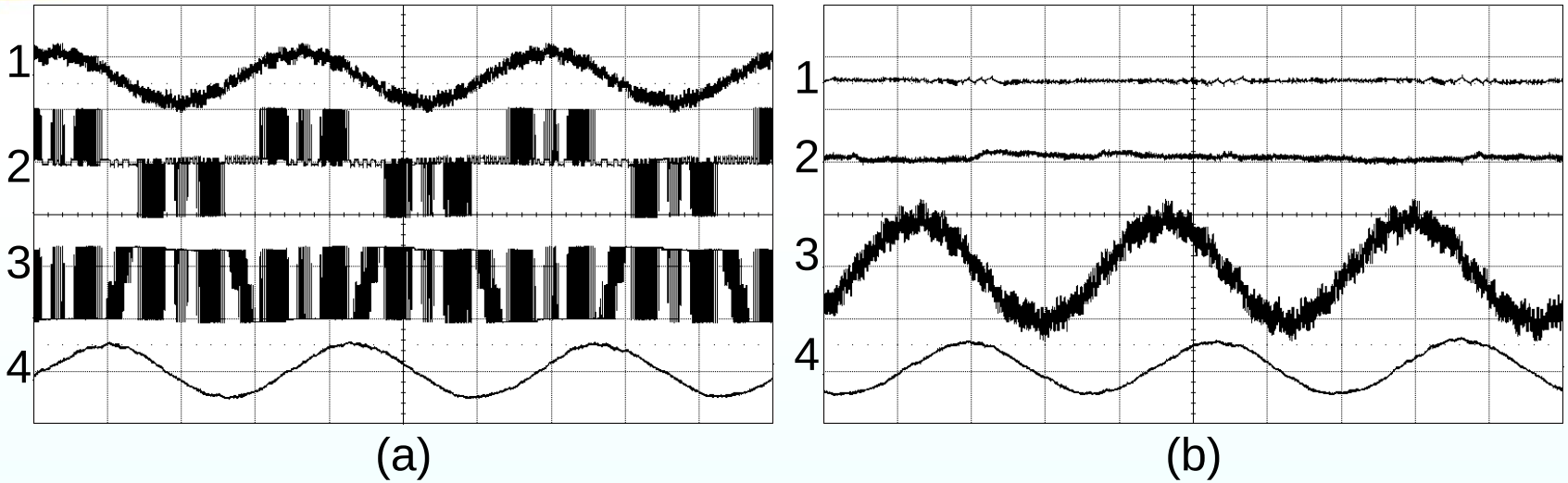


Figure 3 : Experimental results for 15Hz operation (a) Voltage and current waveforms. X-Axis: 20ms/div. (1) A-phase voltage (Y -axis: 100 V/div). (2) Inverter-1 pole voltage V_{AO} (Y -axis: 100V/div). (3) Inverter-2 pole voltage $V_{A'O'}$ (Y -axis: 50V/div). (4) A Phase current (Y -axis: 1A/div) (b) Capacitor voltage waveforms. X-Axis: 20ms/div. (1) Ripple in flying capacitor C1A, (AC coupled) (Y -axis: 5 V/div). (2) Ripple in flying capacitor C2A, (AC coupled) (Y -axis: 200mV/div). (3) A-phase voltage (Y -axis: 50 V/div). (4) A Phase current (Y -axis: 1A/div).

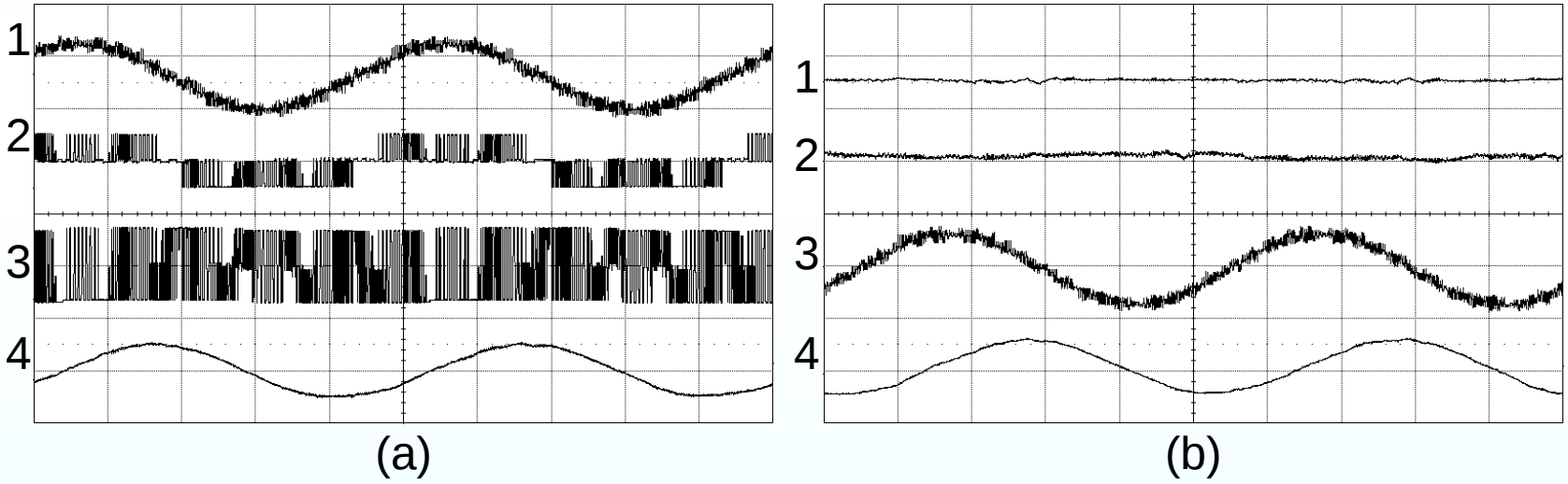


Figure 4 : Experimental results for 20Hz operation (a) Voltage and current waveforms. X-Axis: 10ms/div. (1) A-phase voltage (Y -axis: 100 V/div). (2) Inverter-1 pole voltage V_{AO} (Y -axis: 200V/div). (3) Inverter-2 pole voltage $V_{A'O'}$ (Y -axis: 50V/div). (4) A Phase current (Y -axis: 1A/div) (b) Capacitor voltage waveforms. X-Axis: 10ms/div. (1) Ripple in flying capacitor C1A, (AC coupled) (Y -axis: 5 V/div). (2) Ripple in flying capacitor C2A, (AC coupled) (Y -axis: 200mV/div). (3) A-phase voltage (Y -axis: 100 V/div). (4) A Phase current (Y -axis: 1A/div).

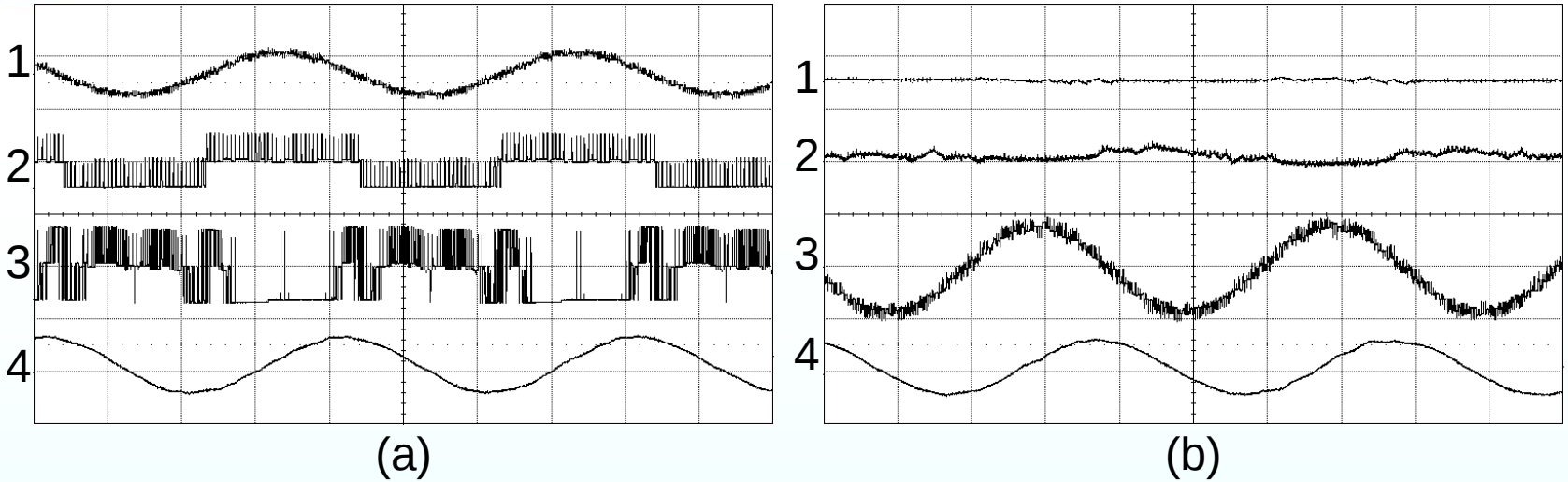


Figure 5 : Experimental results for 25Hz operation (a) Voltage and current waveforms. X-Axis: 10ms/div. (1) A-phase voltage (Y -axis: 200 V/div). (2) Inverter-1 pole voltage V_{AO} (Y -axis: 200V/div). (3) Inverter-2 pole voltage $V_{A'O'}$ (Y -axis: 50V/div). (4) A Phase current (Y -axis: 1A/div) (b) Capacitor voltage waveforms. X-Axis: 10ms/div. (1) Ripple in flying capacitor C1A, (AC coupled) (Y -axis: 5 V/div). (2) Ripple in flying capacitor C2A, (AC coupled) (Y -axis: 200mV/div). (3) A-phase voltage (Y -axis: 100 V/div). (4) A Phase current (Y -axis: 1A/div).

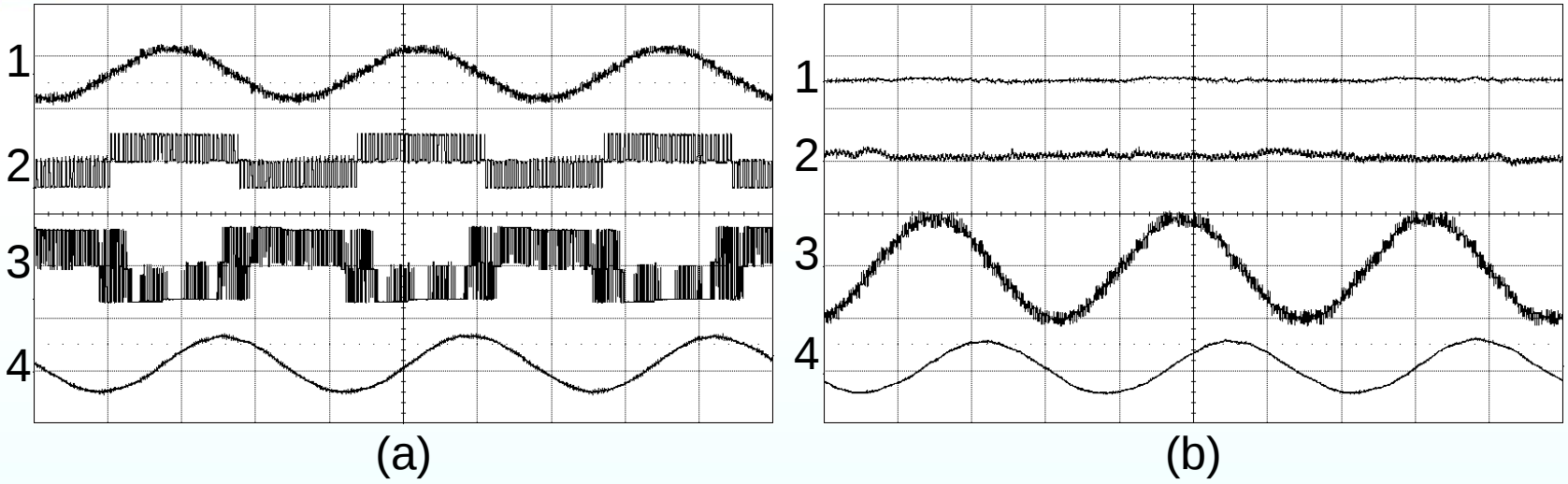


Figure 6 : Experimental results for 30Hz operation (a) Voltage and current waveforms. X-Axis: 10ms/div. (1) A-phase voltage (Y -axis: 200 V/div). (2) Inverter-1 pole voltage V_{AO} (Y -axis: 200V/div). (3) Inverter-2 pole voltage $V_{A'O'}$ (Y -axis: 50V/div). (4) A Phase current (Y -axis: 1A/div) (b) Capacitor voltage waveforms. X-Axis: 10ms/div. (1) Ripple in flying capacitor C1A, (AC coupled) (Y -axis: 5 V/div). (2) Ripple in flying capacitor C2A, (AC coupled) (Y -axis: 200mV/div). (3) A-phase voltage (Y -axis: 100 V/div). (4) A Phase current (Y -axis: 1A/div).

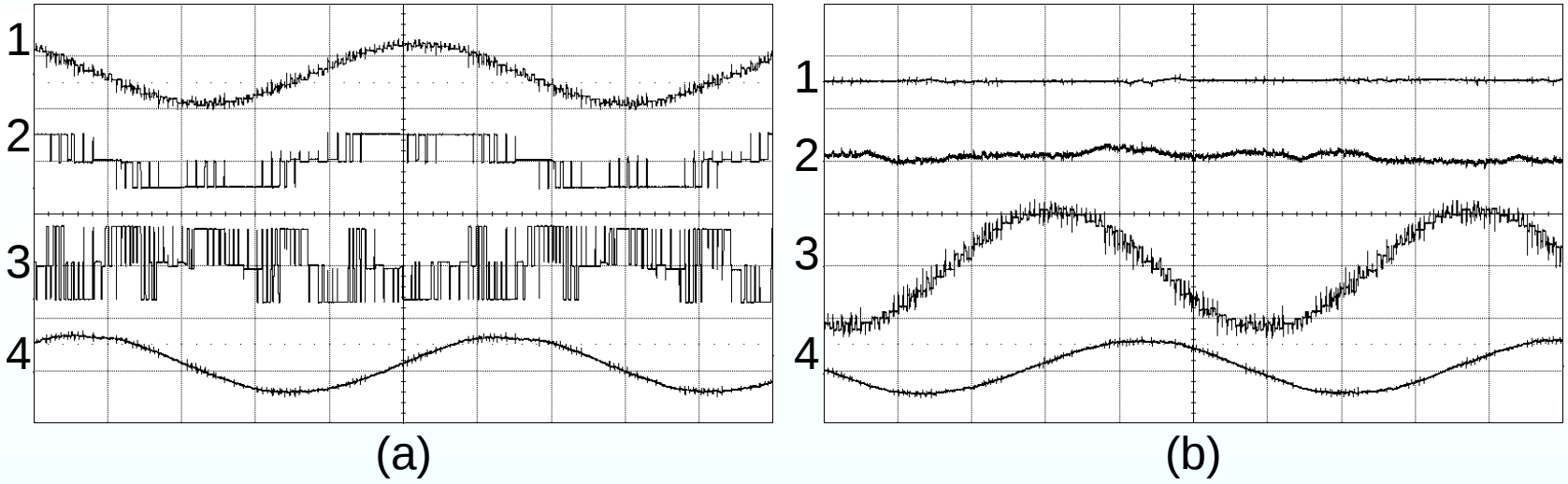


Figure 7 : Experimental results for 35Hz operation (a) Voltage and current waveforms. X-Axis: 5ms/div. (1) A-phase voltage (Y -axis: 200 V/div). (2) Inverter-1 pole voltage V_{AO} (Y -axis: 200V/div). (3) Inverter-2 pole voltage $V_{A'O'}$ (Y -axis: 50V/div). (4) A Phase current (Y -axis: 1A/div) (b) Capacitor voltage waveforms. X-Axis: 5ms/div. (1) Ripple in flying capacitor C1A, (AC coupled) (Y -axis: 5 V/div). (2) Ripple in flying capacitor C2A, (AC coupled) (Y -axis: 200mV/div). (3) A-phase voltage (Y -axis: 100 V/div). (4) A Phase current (Y -axis: 1A/div).

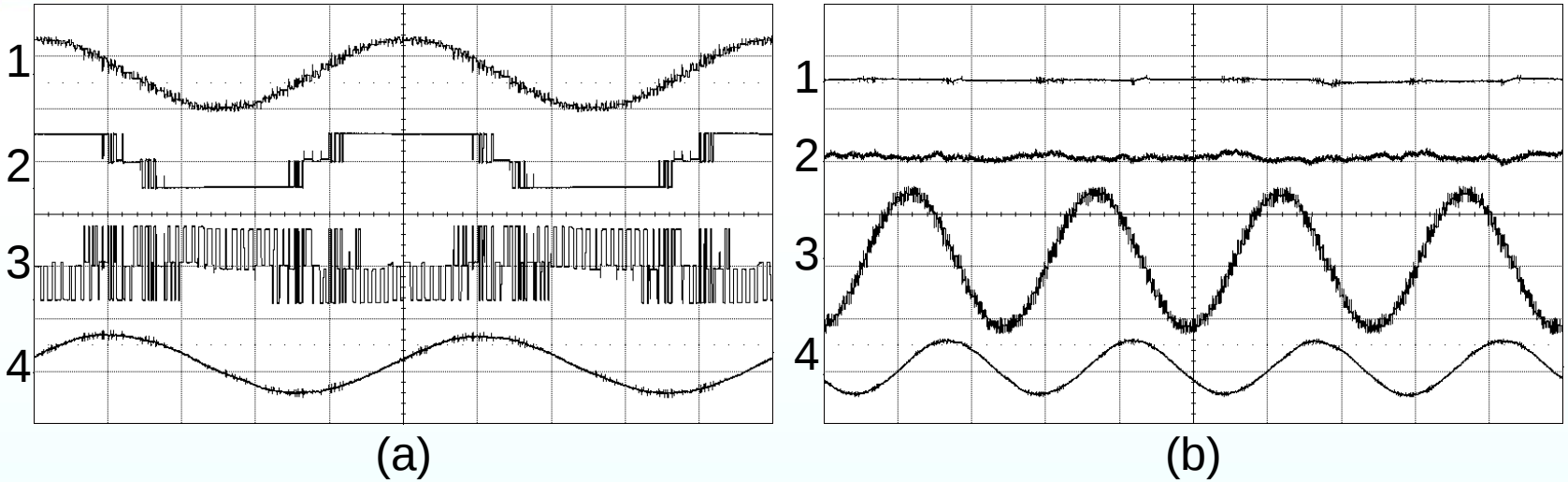


Figure 8 : Experimental results for 40Hz operation (a) Voltage and current waveforms. X-Axis: 5ms/div. (1) A-phase voltage (Y -axis: 200 V/div). (2) Inverter-1 pole voltage V_{AO} (Y -axis: 200V/div). (3) Inverter-2 pole voltage $V_{A'O'}$ (Y -axis: 50V/div). (4) A Phase current (Y -axis: 1A/div) (b) Capacitor voltage waveforms. X-Axis: 10ms/div. (1) Ripple in flying capacitor C1A, (AC coupled) (Y -axis: 5 V/div). (2) Ripple in flying capacitor C2A, (AC coupled) (Y -axis: 200mV/div). (3) A-phase voltage (Y -axis: 100 V/div). (4) A Phase current (Y -axis: 1A/div).

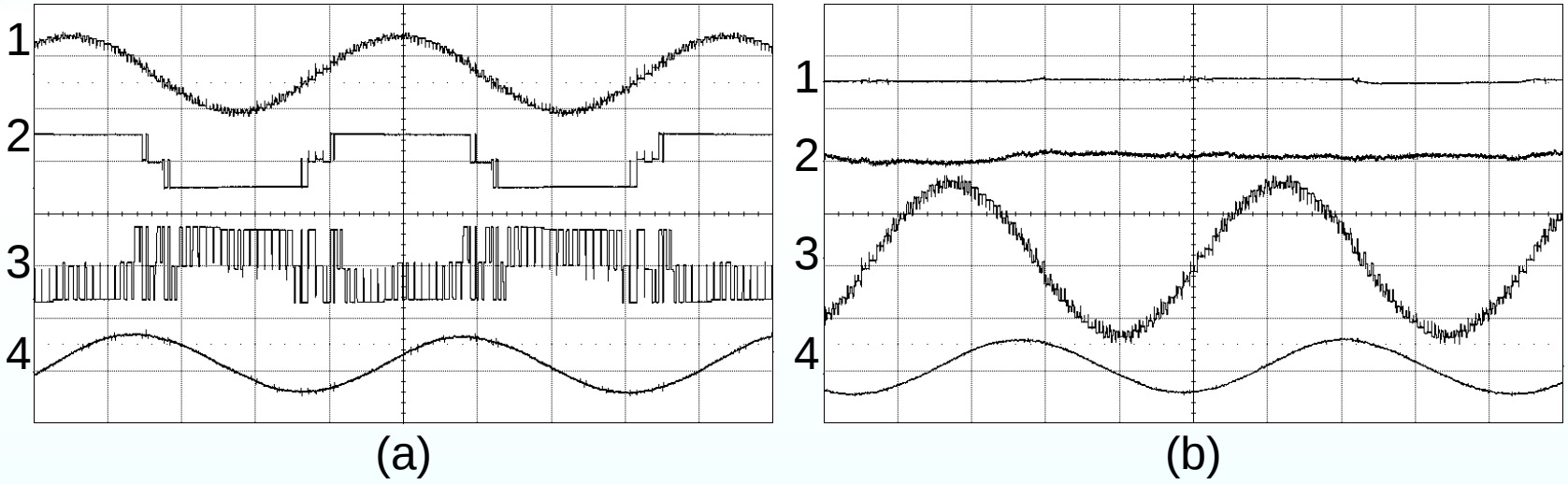


Figure 9 : Experimental results for 45Hz operation (a) Voltage and current waveforms. X-Axis: 5ms/div. (1) A-phase voltage (Y -axis: 200 V/div). (2) Inverter-1 pole voltage V_{AO} (Y -axis: 200V/div). (3) Inverter-2 pole voltage $V_{A'O'}$ (Y -axis: 50V/div). (4) A Phase current (Y -axis: 1A/div) (b) Capacitor voltage waveforms. X-Axis: 5ms/div. (1) Ripple in flying capacitor C1A, (AC coupled) (Y -axis: 5 V/div). (2) Ripple in flying capacitor C2A, (AC coupled) (Y -axis: 200mV/div). (3) A-phase voltage (Y -axis: 100 V/div). (4) A Phase current (Y -axis: 1A/div).

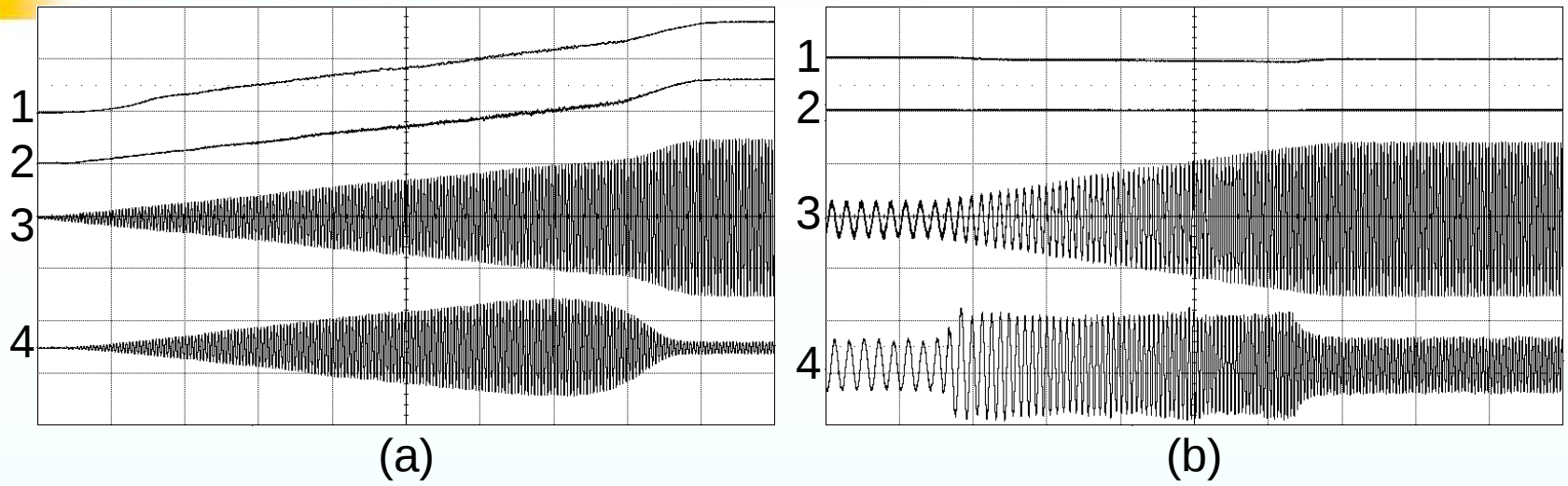


Figure 10 : Performance during startup and acceleration: (a) System startup, fundamental frequency of 45Hz; X-Axis: 500ms/div. (1) Flying Capacitor Voltage C2A, (Y -axis: 50 V/div). (2) Flying Capacitor Voltage C1A, (Y -axis: 100 V/div). (3) A-phase voltage (Y -axis: 100 V/div). (4) A Phase current (Y -axis: 5A/div). (b) Motor acceleration from 10Hz to 45Hz in approx 2.5s; X-Axis: 500ms/div. (1) Flying Capacitor Voltage C2A, (Y -axis: 100 V/div). (2) Flying Capacitor Voltage C1A, (Y -axis: 1000 V/div). (3) A-phase voltage (Y -axis: 100 V/div). (4) A Phase current (Y -axis: 1A/div).

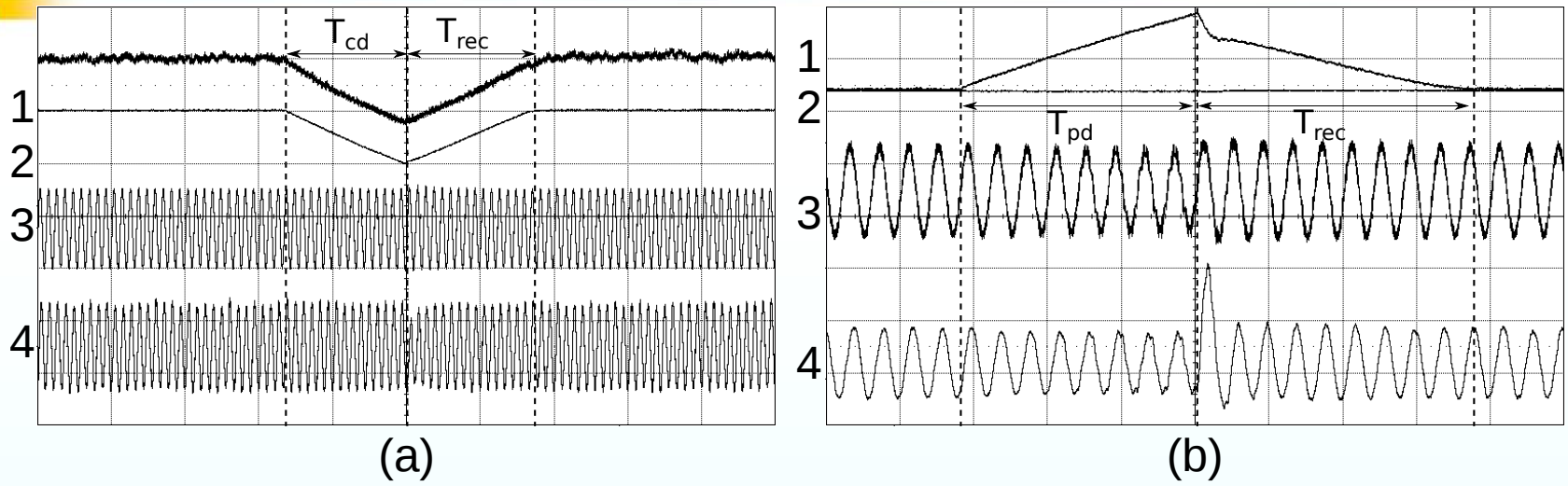


Figure 11 : (a) Control of flying capacitor voltages, fundamental frequency of 45Hz; X-Axis: 200ms/div. (1) Flying Capacitor Voltage C1A, (Y -axis: 5 V/div). (2) Flying Capacitor Voltage C2A, (Y -axis: 10 V/div). (3) A-phase voltage (Y -axis: 100 V/div). (4) A Phase current (Y -axis: 0.5A/div). (b) Control of inverter-2 DC bus, fundamental frequency 25Hz; X-Axis: 100ms/div. (1) Inverter-1 DC bus voltage,(35V nom.), (Y -axis: 10 V/div). (2) Inverter-2 DC bus voltage (100V nom.), (Y -axis: 100 V/div). (3) A-phase voltage (Y -axis: 50 V/div). (4) A Phase current (Y -axis: 0.5A/div).

Summary

A novel 9-level inverter topology proposed with

- **Reduced component count**: Only eight switches and two capacitors per phase, and two DC links
- **Capacitor voltage balancing** at switching frequency
  - Over entire linear modulation range
  - Any load power factor
- Iteration-less modulation and switching control scheme
- No circulating power or DC bus overcharging

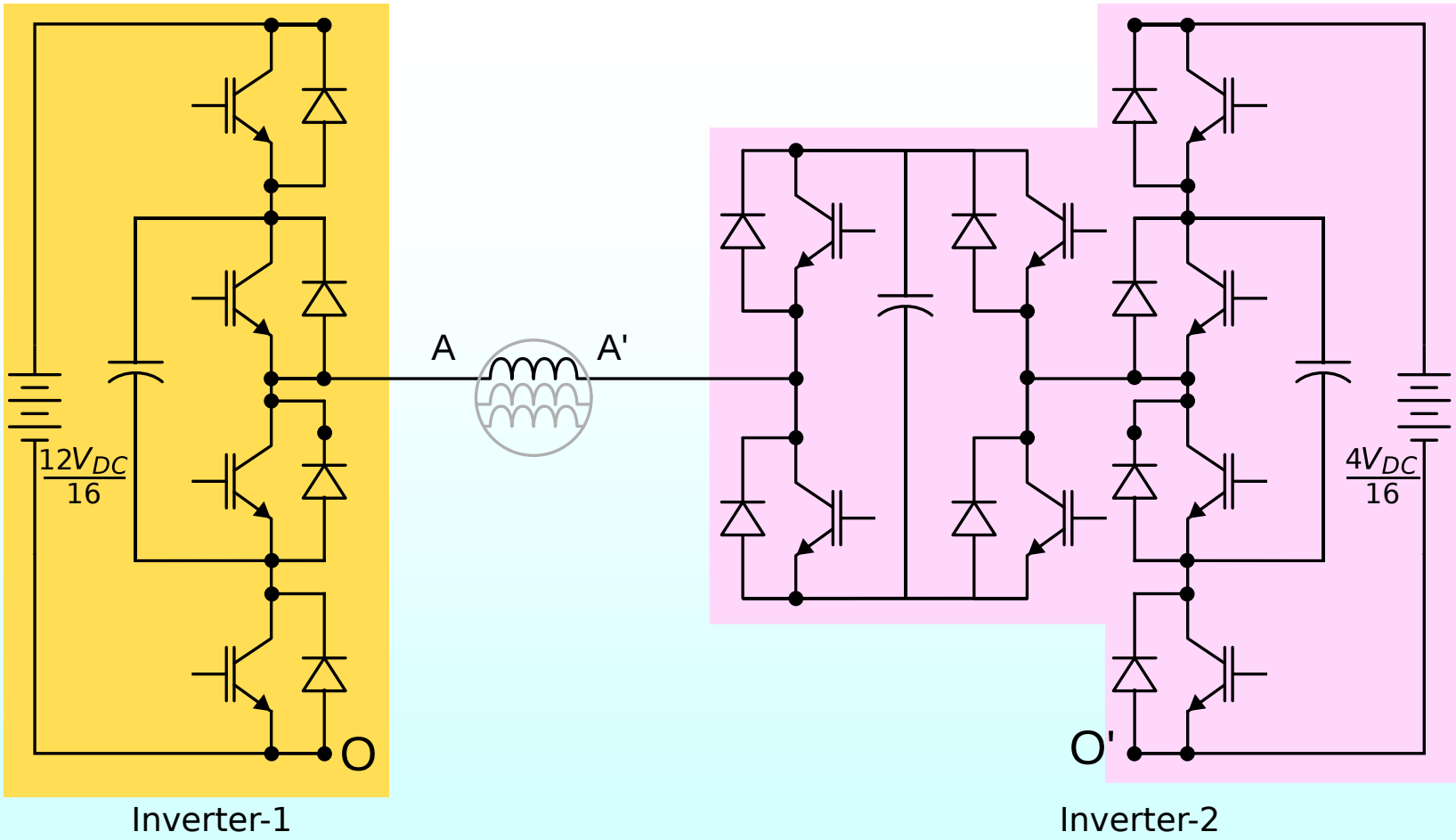
Seventeen Level Inverter Topology for Open End Induction Motor Drive

Overview

- A 17-level inverter topology for open-end induction motor drives
- Low component count: 12 switches and 2 capacitors per phase
- Instantaneous capacitor balancing over full modulation range, for any load power factor.
- No pre-charging required for capacitors

Power Circuit Topology

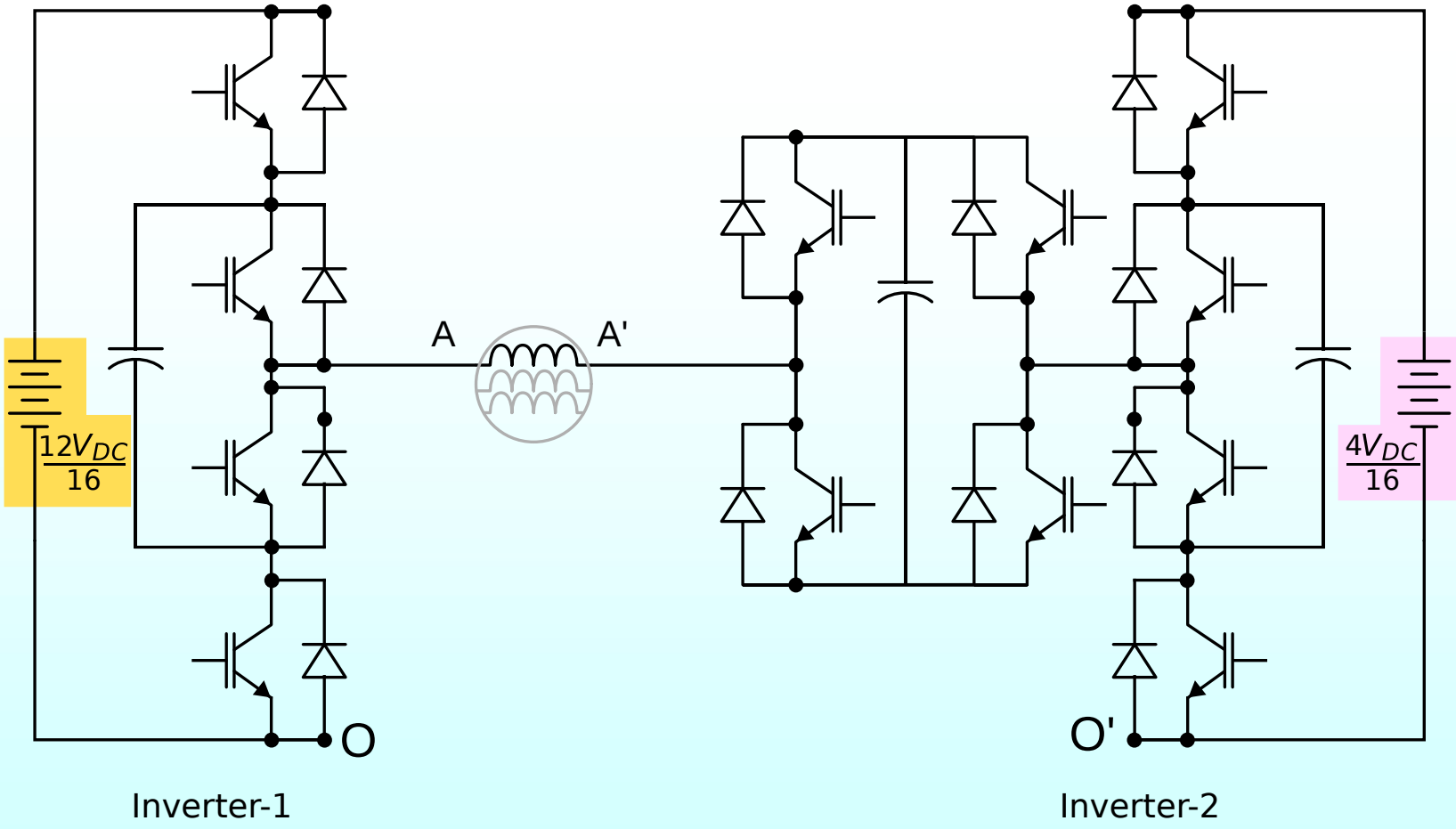
Per-phase circuit, for A-phase



- Two inverters, powered by isolated DC supplies

Power Circuit Topology

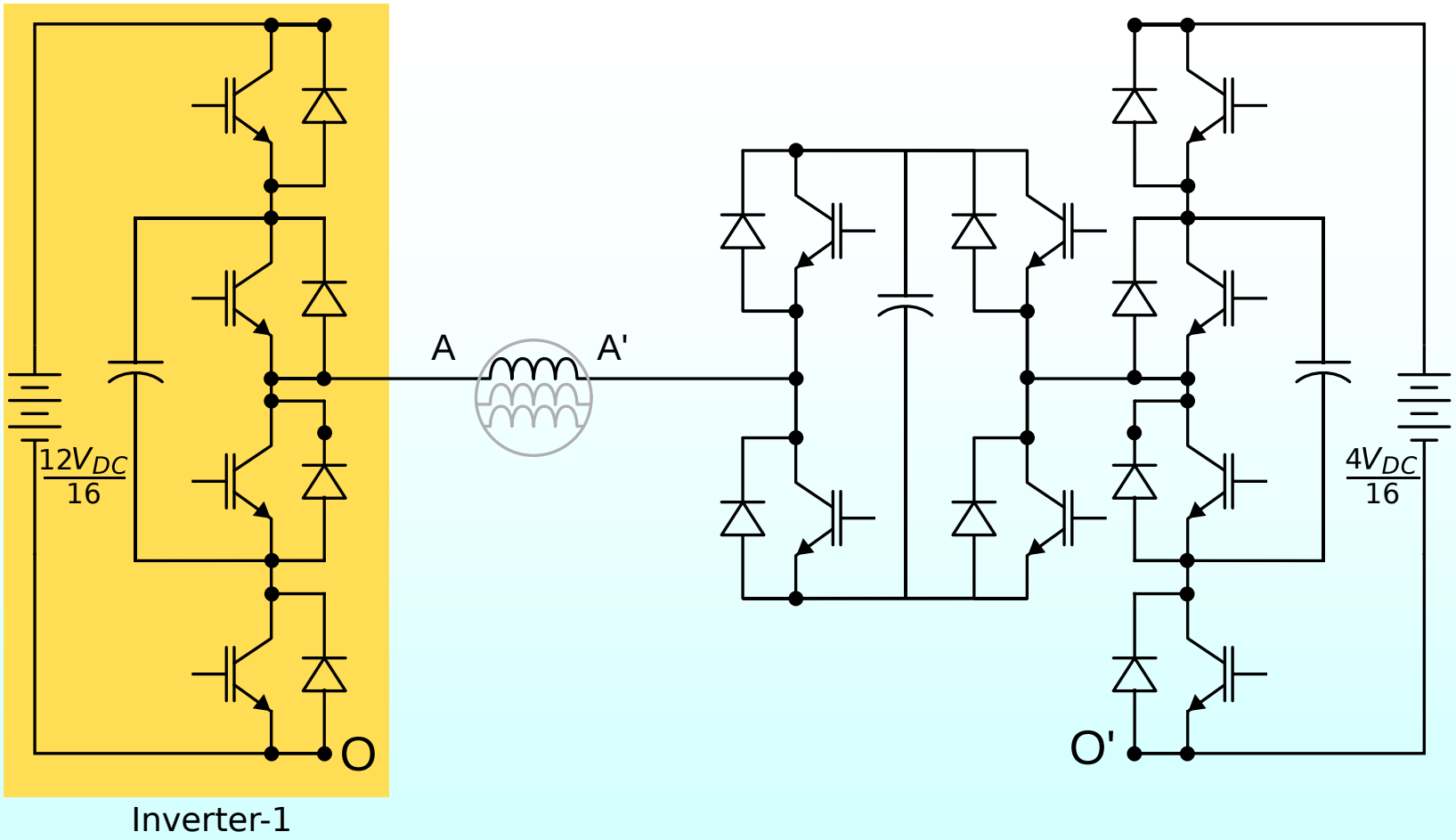
Per-phase circuit, for A-phase



- DC supply voltages in 3:1 ratio

Power Circuit Topology

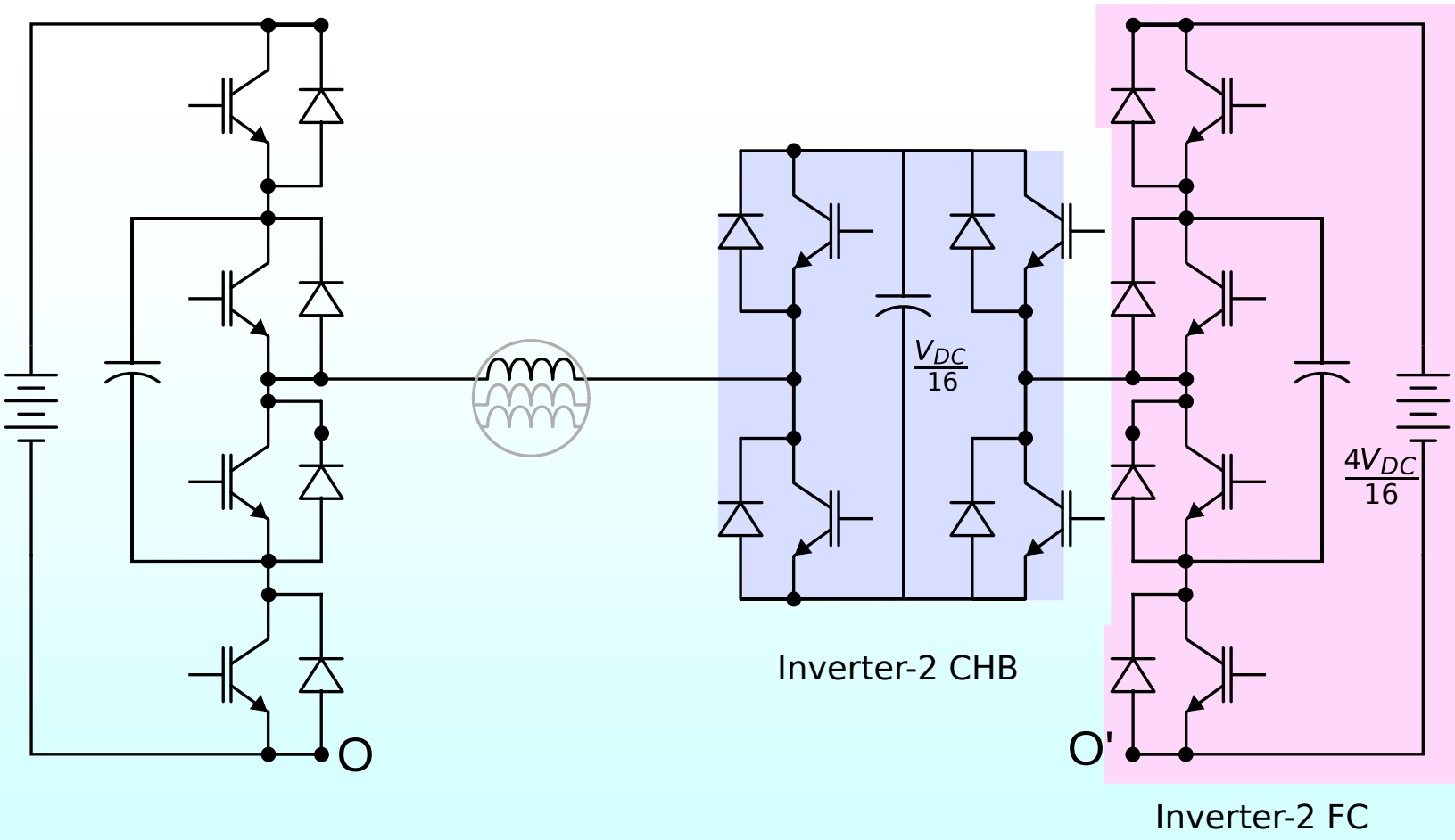
Per-phase circuit, for A-phase



- Inverter1: 3-Level Flying Capacitor Inverter

Power Circuit Topology

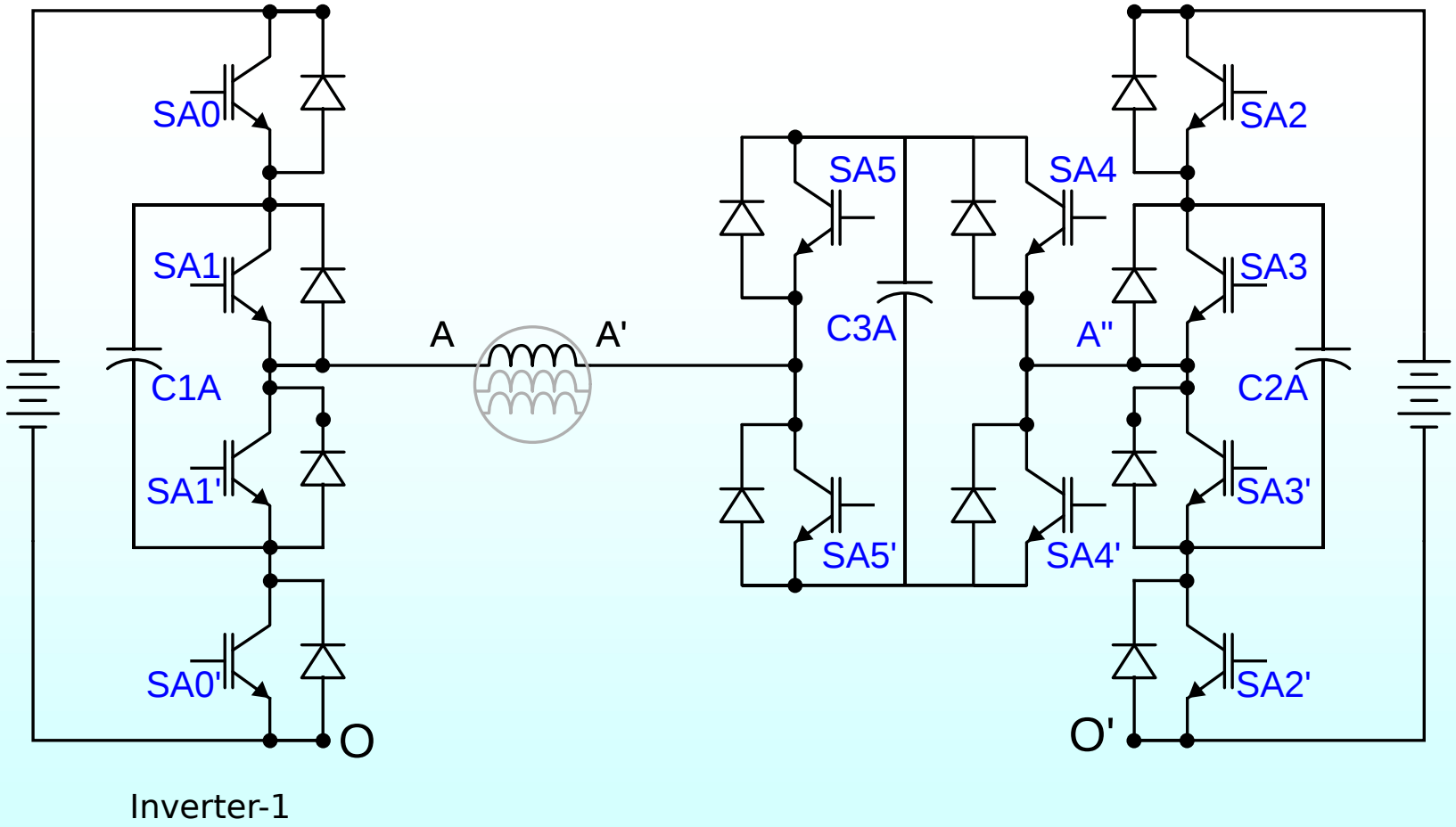
Per-phase circuit, for A-phase



- Inverter2: Cascade connection of 3L Flying capacitor inverter and floating cascaded H-Bridge

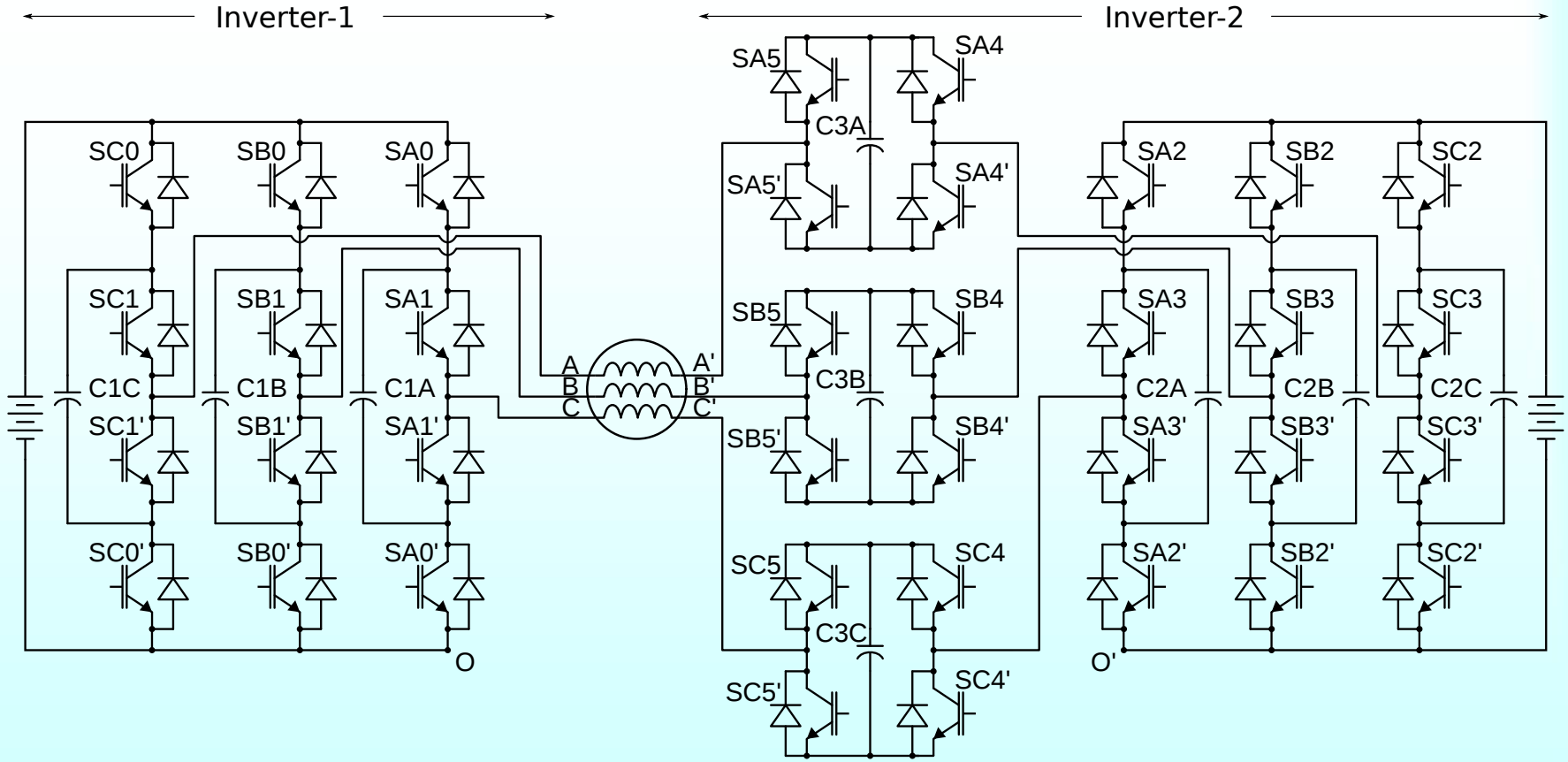
Power Circuit Topology

Per-phase circuit, for A-phase

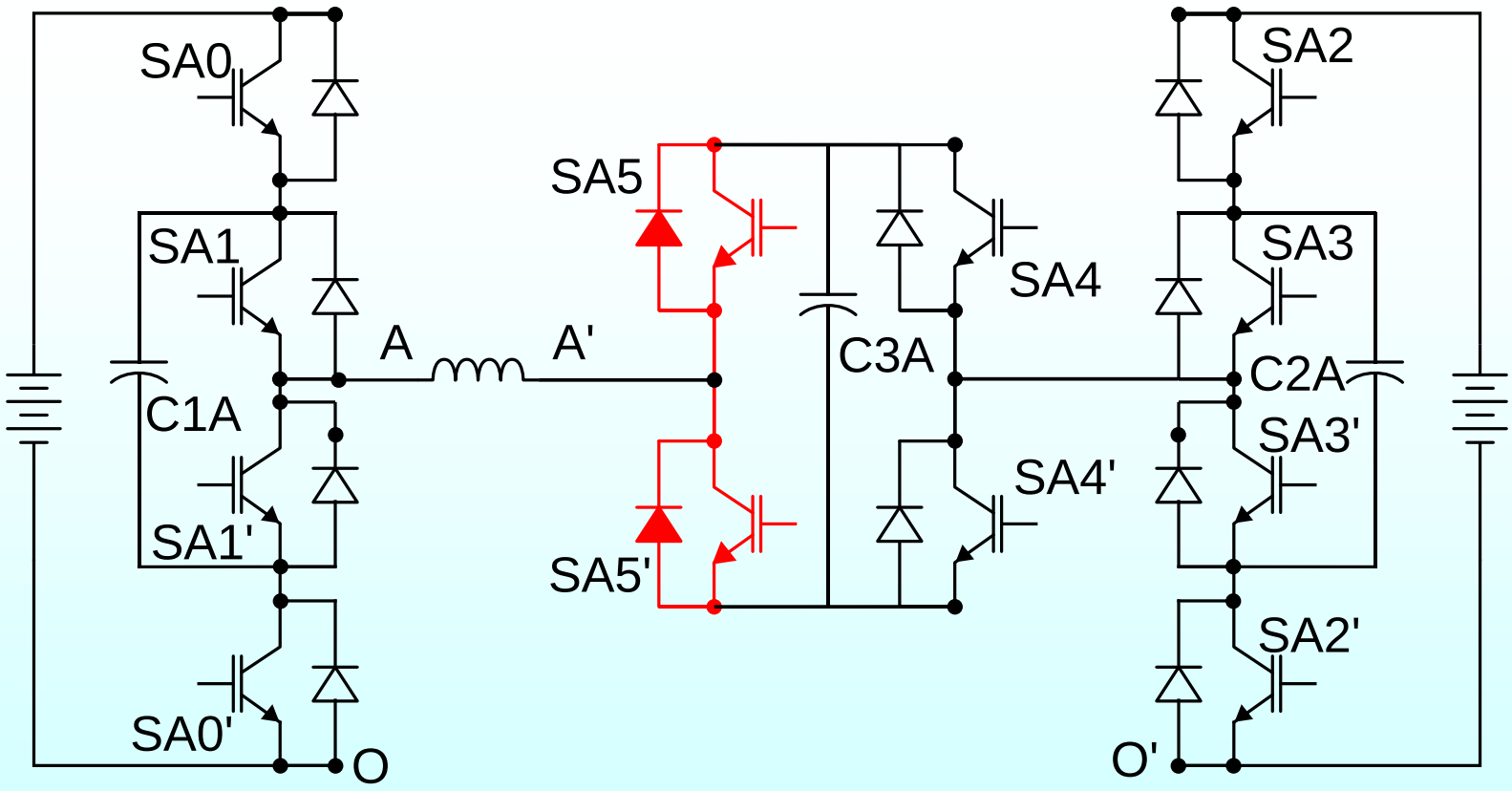


- 12 switches and 3 floating capacitors per phase

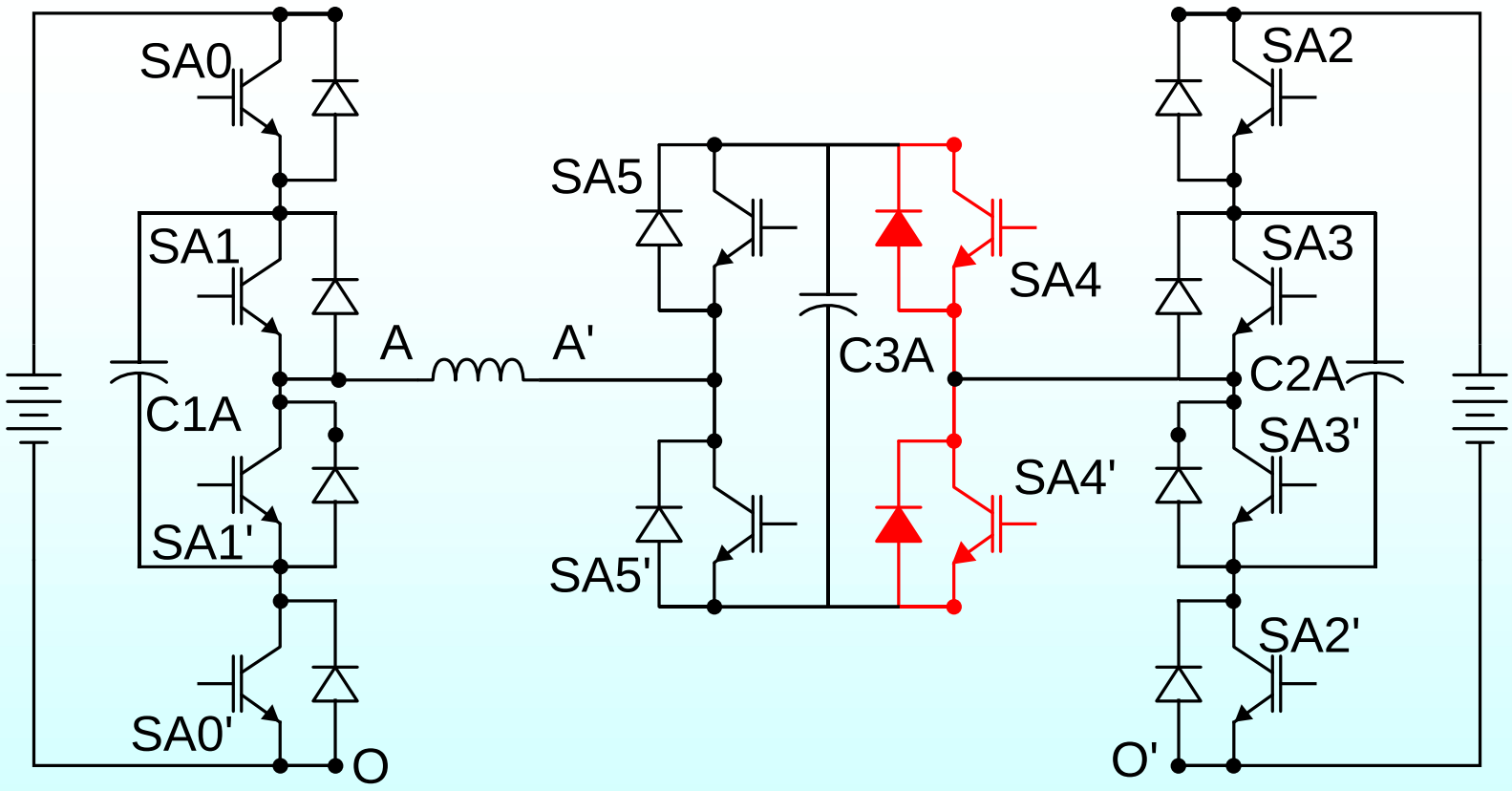
Circuit Topology



Complementary Switch Pairs

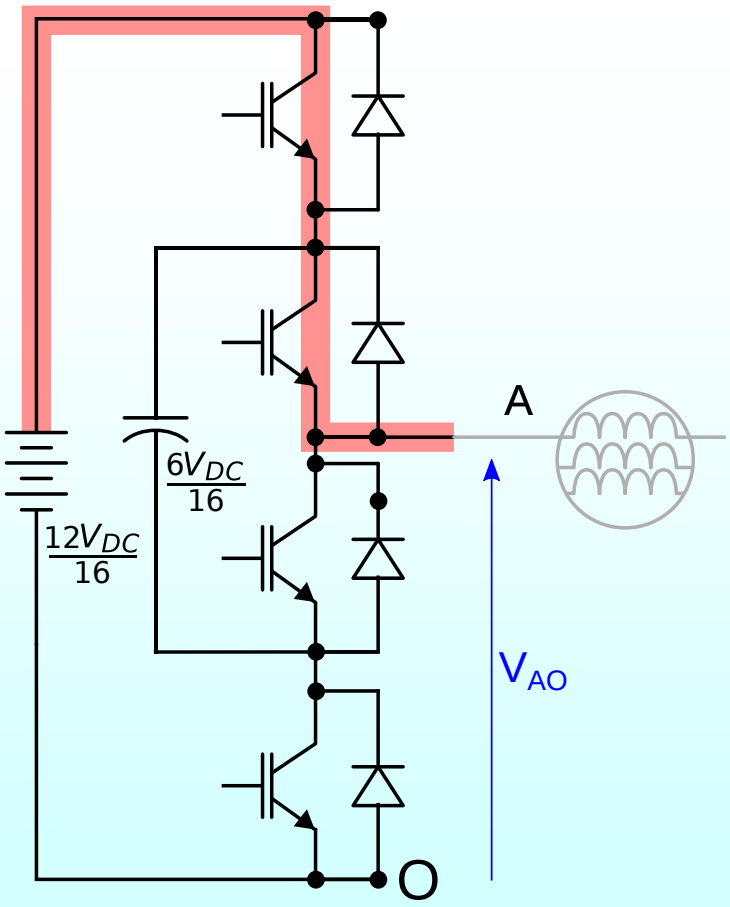


Complementary Switch Pairs



Pole Voltage Levels

Inverter-1

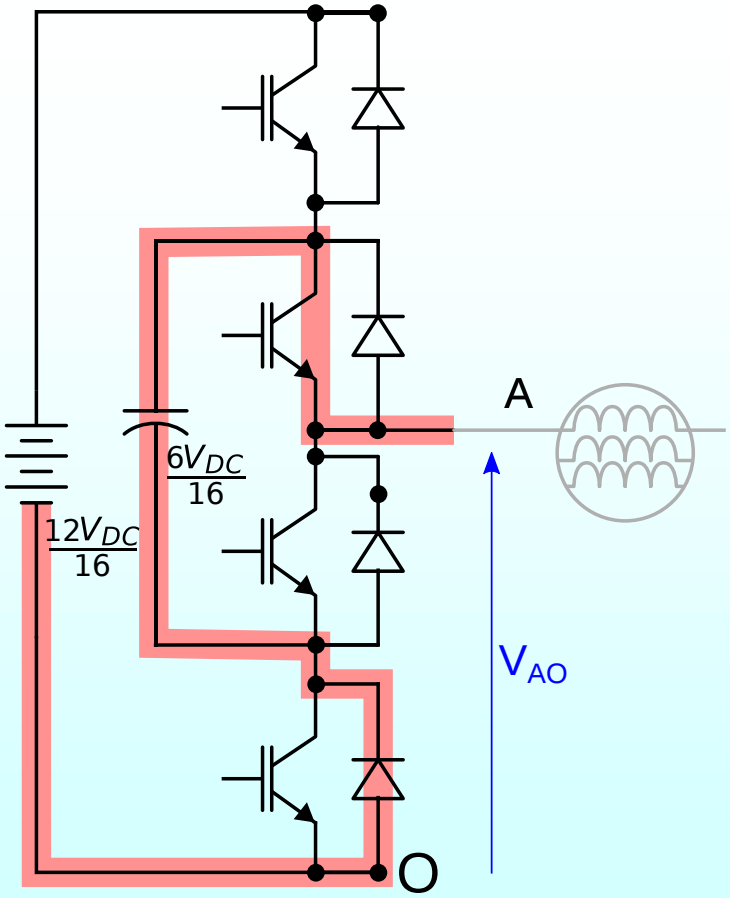


Inverter-1 pole voltage ($\mathbf{V_{AO}}$) can have **three levels**:

- $12V_{DC}/16$,
- $6V_{DC}/16$
- or 0

Pole Voltage Levels

Inverter-1

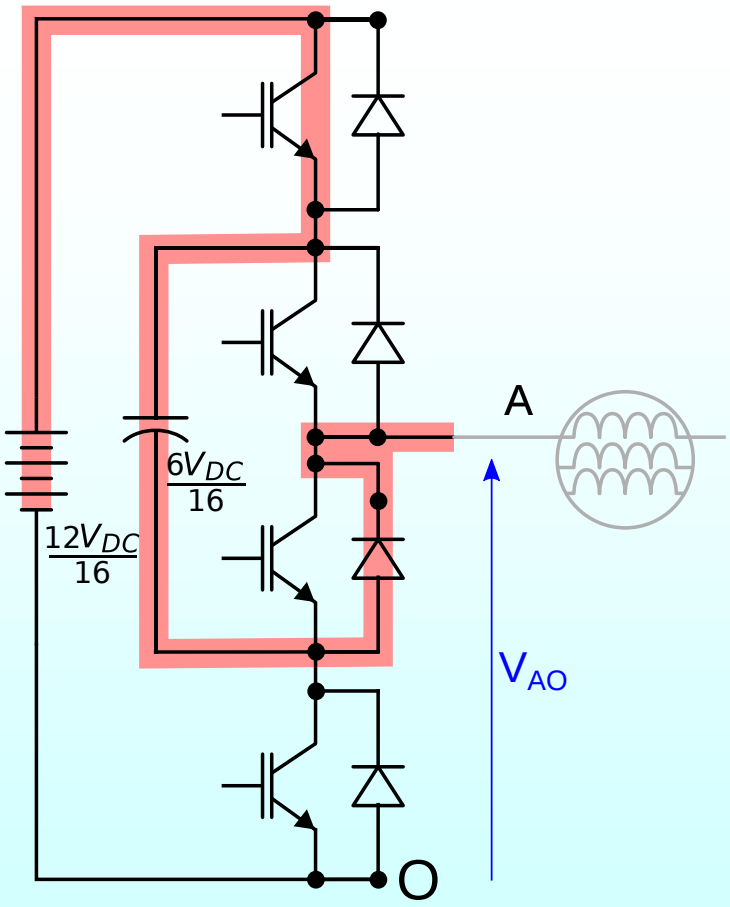


Inverter-1 pole voltage ($\mathbf{V_{AO}}$) can have **three levels**:

- $12V_{DC}/16$,
- $6V_{DC}/16$ (C1 connected to DC-)
- or 0

Pole Voltage Levels

Inverter-1

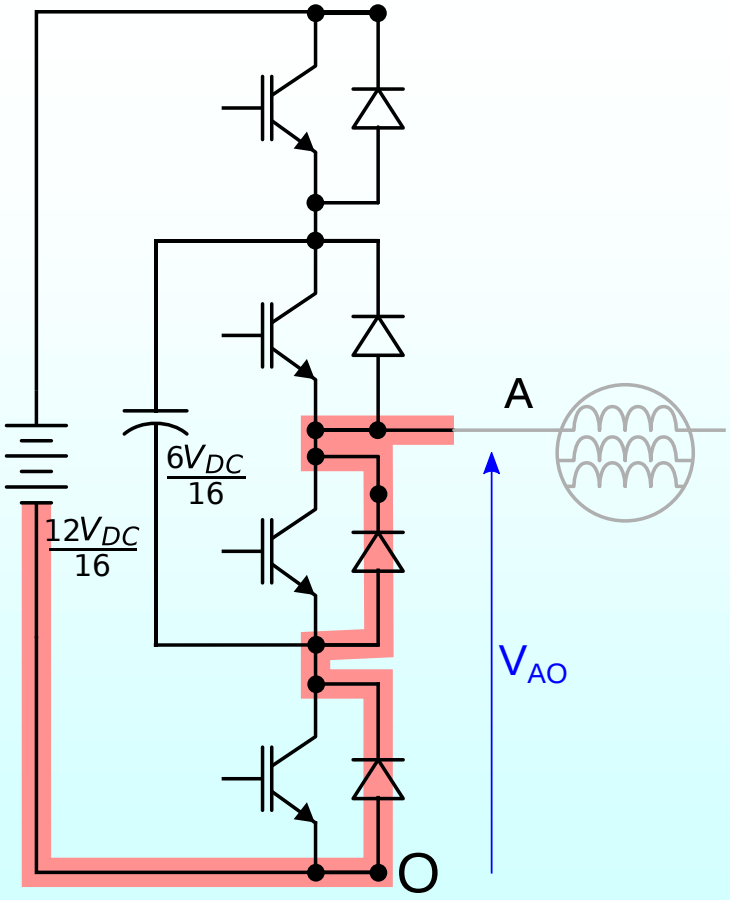


Inverter-1 pole voltage ($\mathbf{V_{AO}}$) can have **three levels**:

- $12V_{DC}/16$,
- $6V_{DC}/16$ (C1 connected to DC+)
- or 0

Pole Voltage Levels

Inverter-1



Inverter-1 pole voltage ($\mathbf{V_{AO}}$) can have **three levels**:

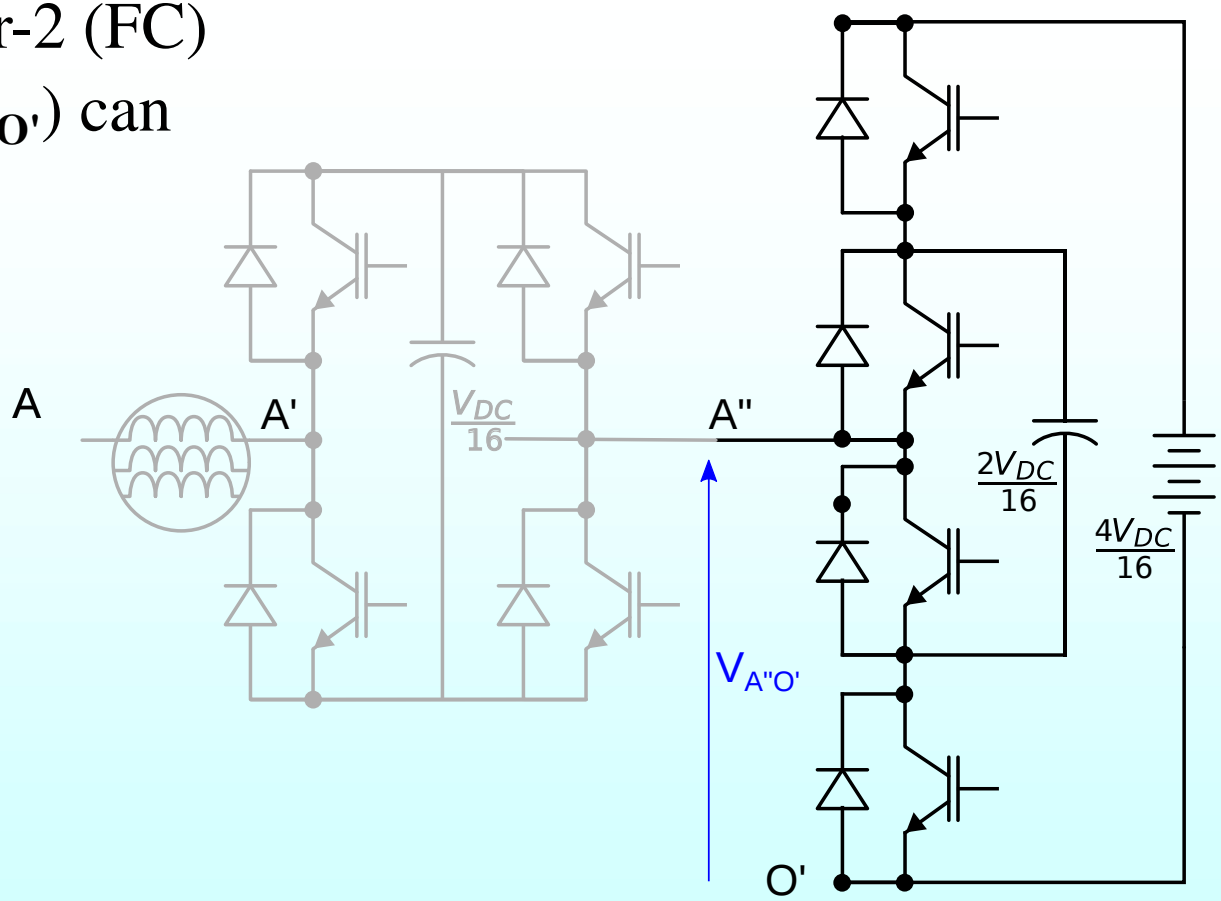
- $12V_{DC}/16$,
- $6V_{DC}/16$
- or 0

Pole Voltage Levels

Inverter-2

Similarly, Inverter-2 (FC) pole voltage ($\mathbf{V_{A"O'}}$) can have **three levels**:

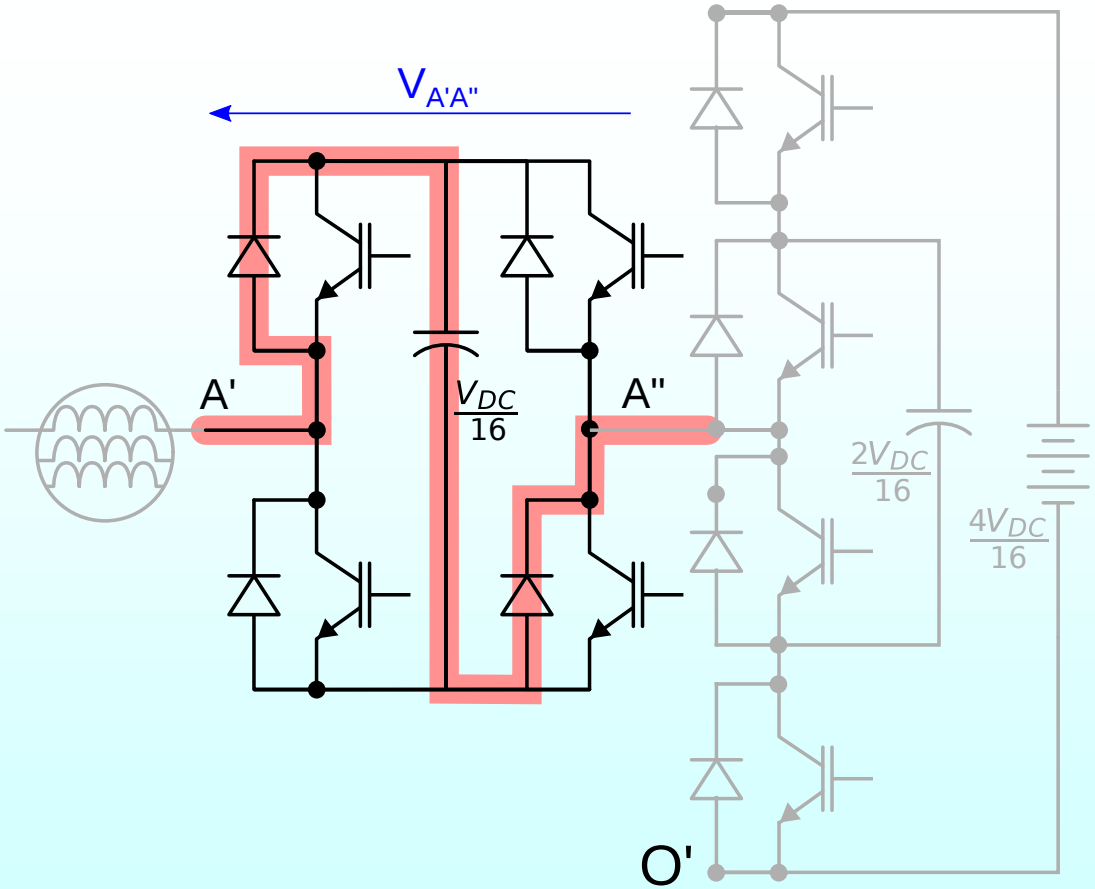
- $4V_{DC}/16$,
- $2V_{DC}/16$
- or 0



Pole Voltage Levels

Inverter-2

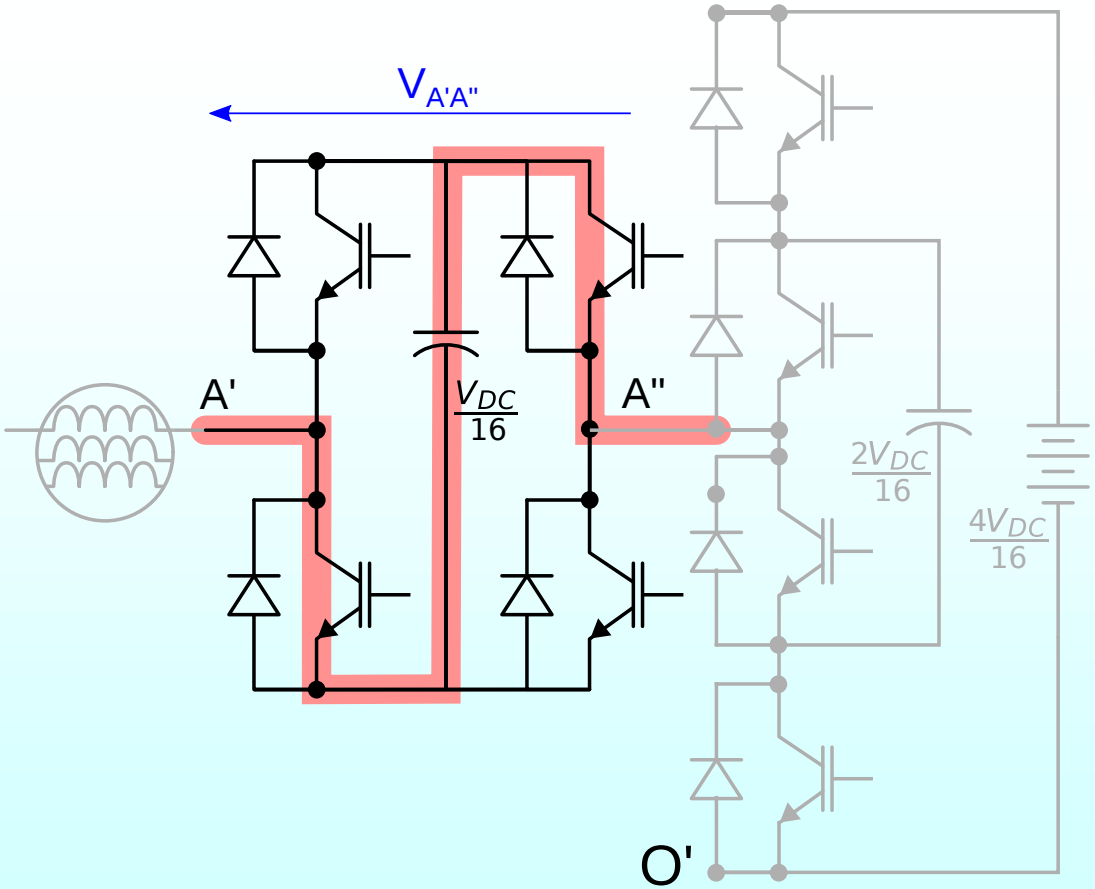
H-bridge can add
$(+V_{DC}/16)$,
$(-V_{DC}/16)$,
or (0).



Pole Voltage Levels

Inverter-2

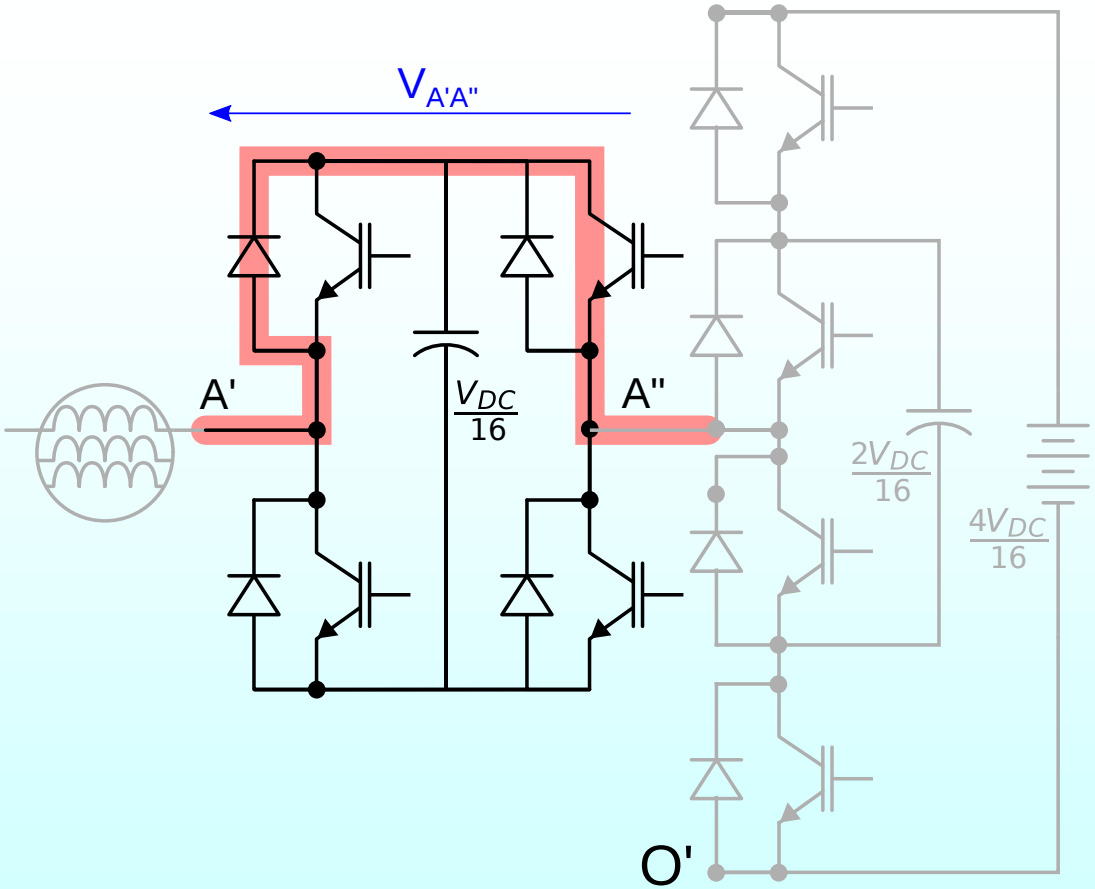
H-bridge can add
$(+V_{DC}/16)$,
$(-V_{DC}/16)$,
or (0).



Pole Voltage Levels

Inverter-2

H-bridge can add
$(+V_{DC}/16)$,
$(-V_{DC}/16)$,
or (0).

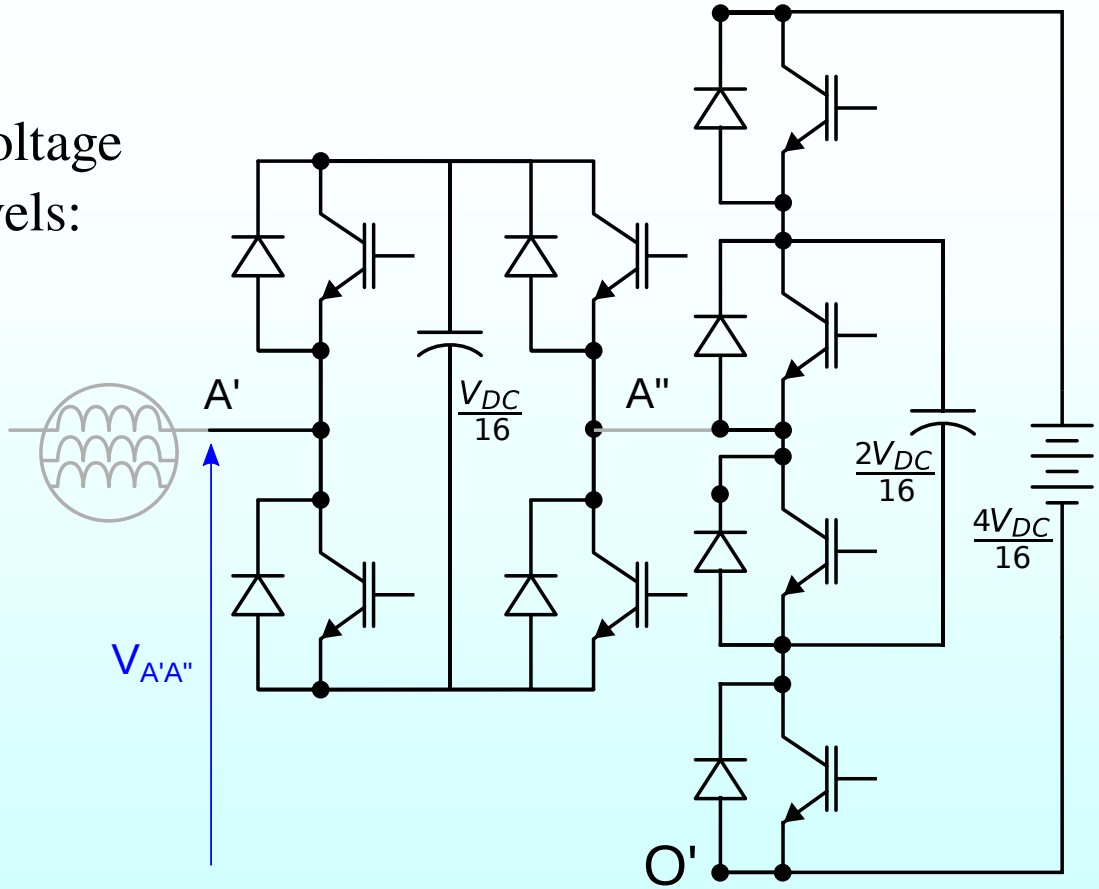


Pole Voltage Levels

Inverter-2

Hence, Inverter-2 pole voltage ($V_{A'O'}$) can take seven levels:

- $0 \pm V_{DC}/16$
- $2V_{DC}/16 \pm V_{DC}/16$
- $4V_{DC}/16 \pm V_{DC}/16$

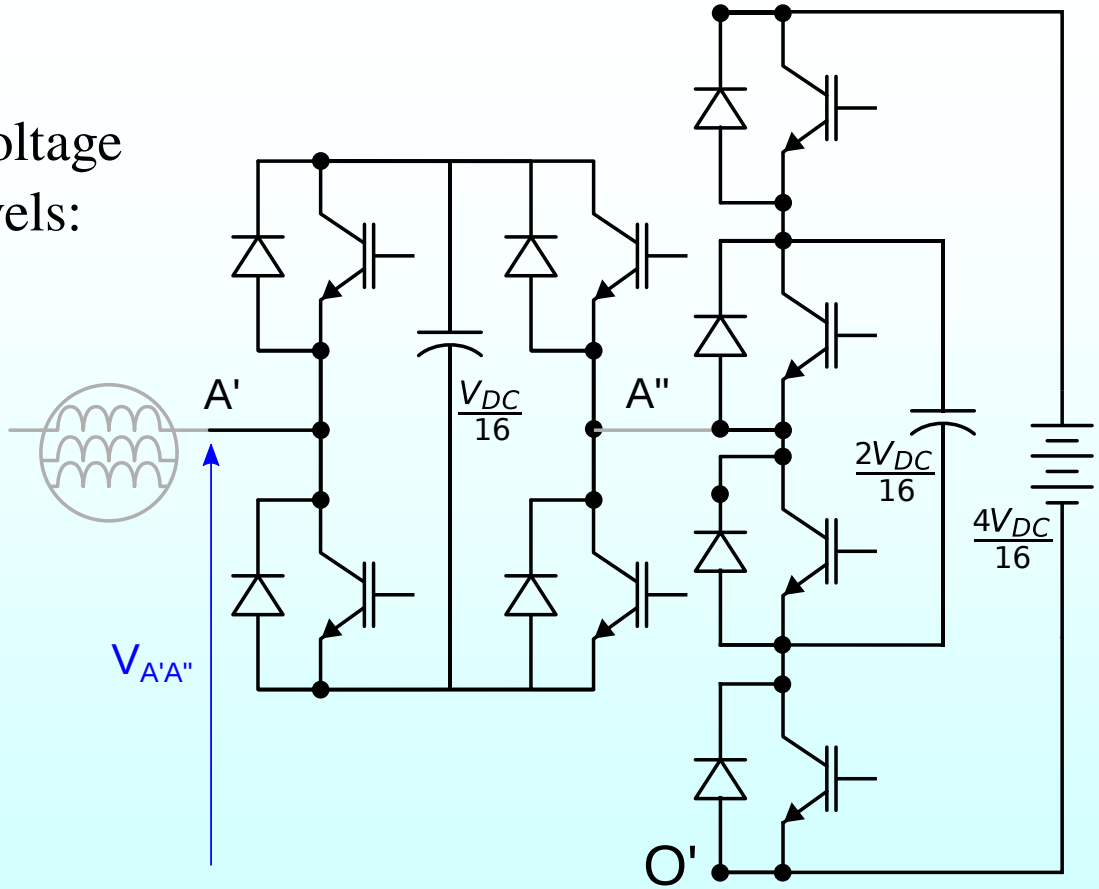


Pole Voltage Levels

Inverter-2

Hence, Inverter-2 pole voltage ($V_{A'O'}$) can take seven levels:

- $-V_{DC}/16$
- 0
- $V_{DC}/16$
- $2V_{DC}/16$
- $3V_{DC}/16$
- $4V_{DC}/16$
- $5V_{DC}/16$



Effective Pole Voltages

- Inverter-1 is a three level inverter (0, $3V_{DC}/8$, $6V_{DC}/8$)
- Inverter-2 is a seven level inverter (-$0.5V_{DC}/8$, 0, $0.5V_{DC}/8$, $1V_{DC}/8$, ..., $2.5V_{DC}/8$)
- Total of 3x7=21 combinations

Phase Voltage Levels

Level	$V_{AA'}$	V_{AO}	$V_{A'O'}$
-1	$-2.5V_{DC}/8$	0	$2.5V_{DC}/8$
0	$-2V_{DC}/8$	0	$2V_{DC}/8$
1	$-1.5V_{DC}/8$	0	$1.5V_{DC}/8$
2	$-1V_{DC}/8$	0	$1V_{DC}/8$
3	$-0.5V_{DC}/8$	0	$0.5V_{DC}/8$
4	0	0	0
5	$0.5V_{DC}/8$	0	$-0.5V_{DC}/8$
5	$0.5V_{DC}/8$	$3V_{DC}/8$	$2.5V_{DC}/8$
6	$V_{DC}/8$	$3V_{DC}/8$	$2V_{DC}/8$
7	$1.5V_{DC}/8$	$3V_{DC}/8$	$1.5V_{DC}/8$
8	$2V_{DC}/8$	$3V_{DC}/8$	$1V_{DC}/8$
9	$2.5V_{DC}/8$	$3V_{DC}/8$	$0.5V_{DC}/8$
10	3	$3V_{DC}/8$	0

Phase Voltage Levels

Level	$\mathbf{V_{AA'}}$	$\mathbf{V_{AO}}$	$\mathbf{V_{A'O'}}$
11	$3.5V_{DC}/8$	$3V_{DC}/8$	$-0.5V_{DC}/8$
11	$3.5V_{DC}/8$	$6V_{DC}/8$	$2.5V_{DC}/8$
12	$4V_{DC}/8$	$6V_{DC}/8$	$2V_{DC}/8$
13	$4.5V_{DC}/8$	$6V_{DC}/8$	$1.5V_{DC}/8$
14	$5V_{DC}/8$	$6V_{DC}/8$	$1V_{DC}/8$
15	$5.5V_{DC}/8$	$6V_{DC}/8$	$0.5V_{DC}/8$
16	6	$6V_{DC}/8$	0
17	$6.5V_{DC}/8$	$6V_{DC}/8$	$-0.5V_{DC}/8$

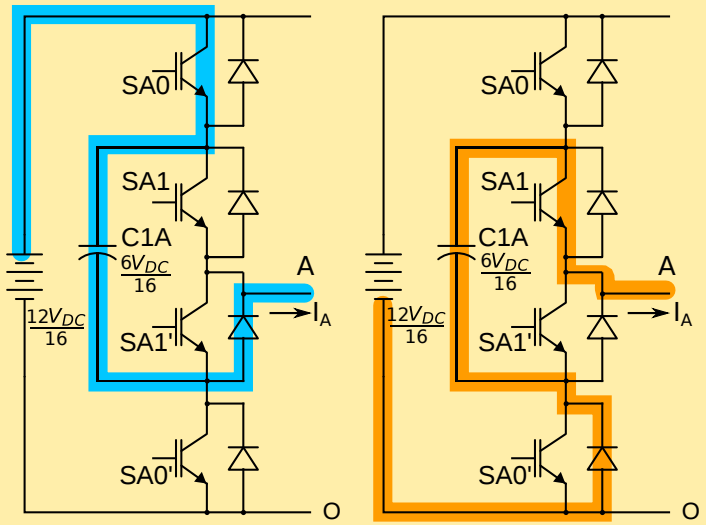
Some phase voltage levels have multiple pole voltage combinations (e.g. level 5, 11)

Flying Capacitor Voltage Balancing

using switching state redundancy

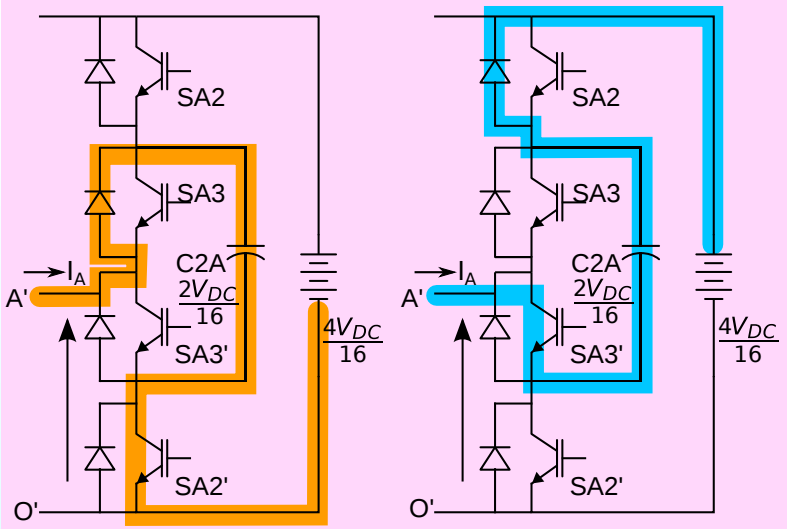
Inverter-1

Pole voltage redundancy for $V_{AO} = 6V_{DC}/16$



Inverter-2

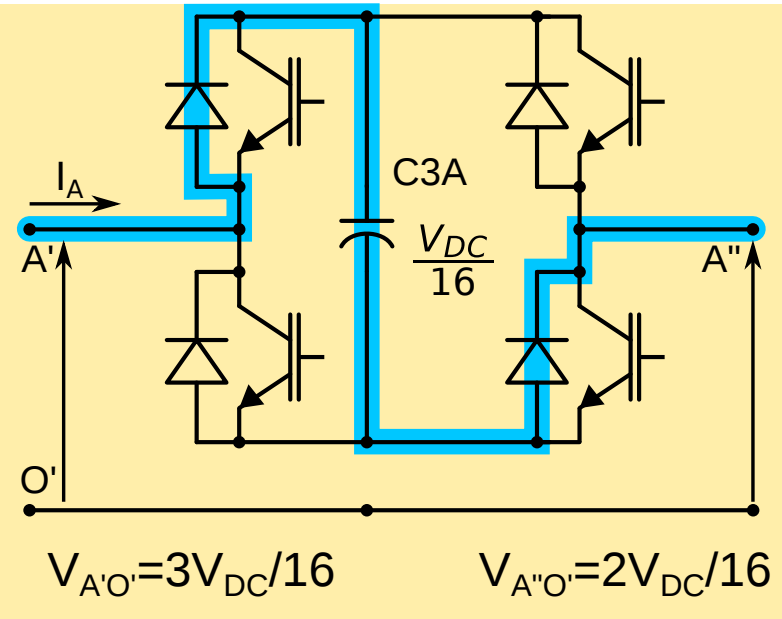
Pole voltage redundancy for $V_{A'O'} = 2V_{DC}/16$

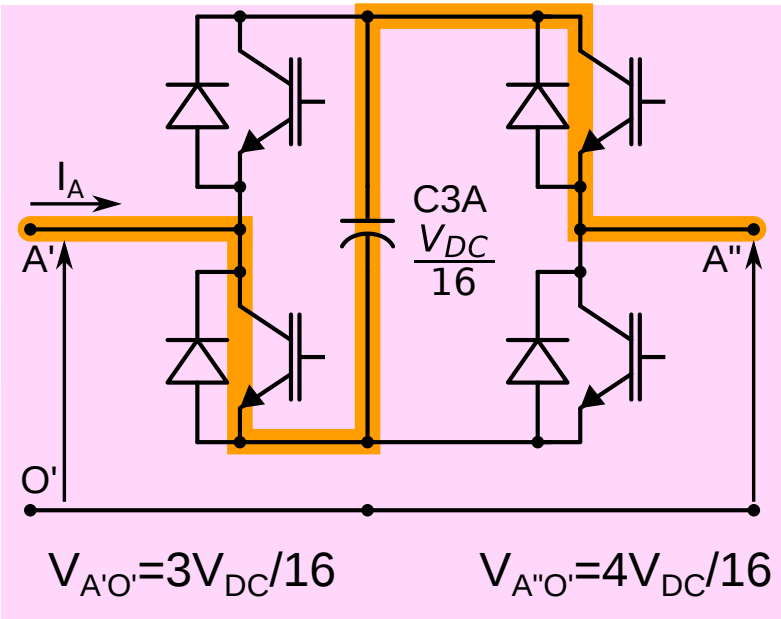


- Instantaneous balancing of all floating capacitors for any load current
- Balancing at switching frequency: low capacitance required
  - CA1 unaffected for [$V_{AO} = 12V_{DC}/16$ or 0]
  - CA2 unaffected for [$V_{A'O'} = 4V_{DC}/16$ or 0]

H-Bridge Capacitor Voltage Balancing

using inverter pole voltage selection





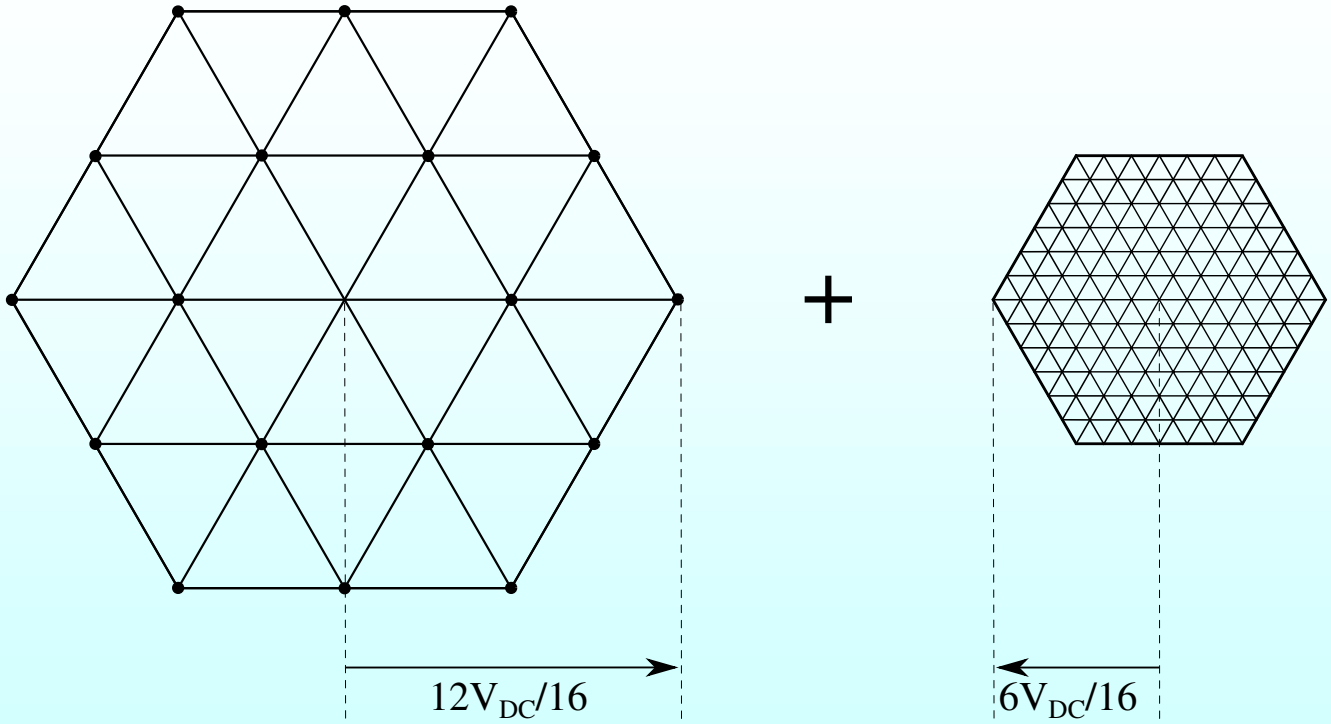
- No switching state redundancy for CHB
- H-bridge capacitors balanced by pole voltage selection.
- E.g. for $V_{A'O'} = 3V_{DC}/16$:
  - C3A Charges when $V_{AA'} = V_{DC}/16$ and $V_{A"O'} = 2V_{DC}/16$
  - C3A Discharges when $V_{AA'} = -V_{DC}/16$ and $V_{A"O'} = 4V_{DC}/16$

Superposition of Space-Vector Dagrams

generating effective space vector structure

Inverter-1 forms a 3-L space vector structure

Inverter-2 forms a 7-L space vector structure

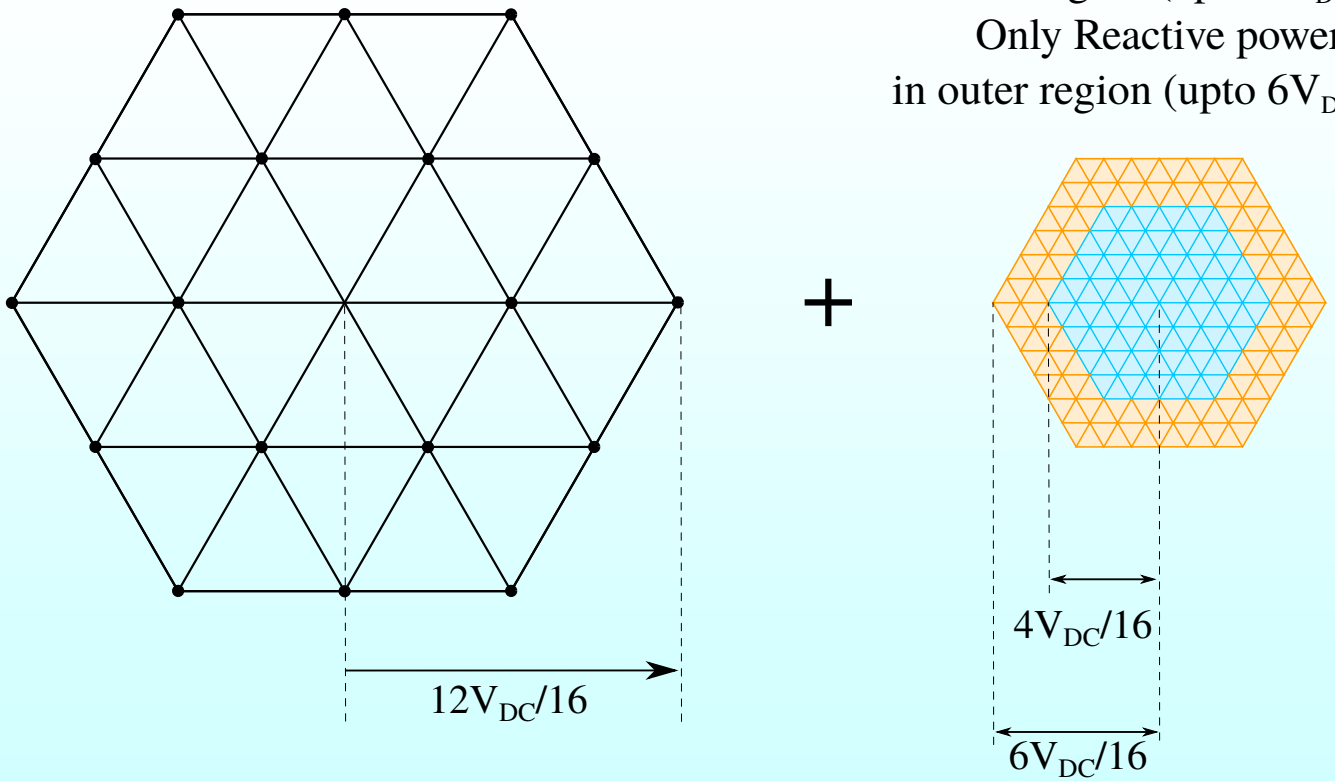


Superposition of Space-Vector Dagrams

generating effective space vector structure

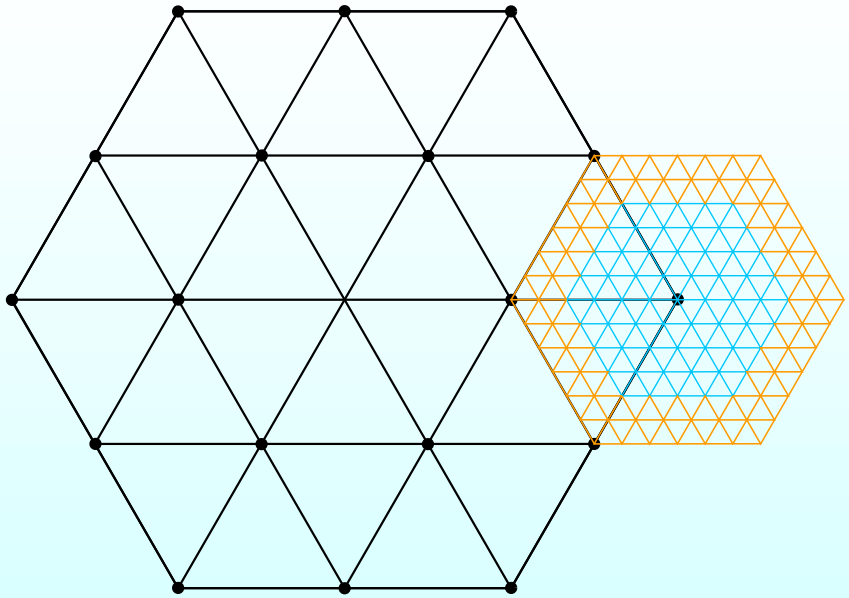
Inverter-2 DC link is $4V_{DC}/16$!

Can deliver real power
in inner region (upto $4V_{DC}/16$),
Only Reactive power
in outer region (upto $6V_{DC}/16$)



Superposition of Space-Vector Dagrams

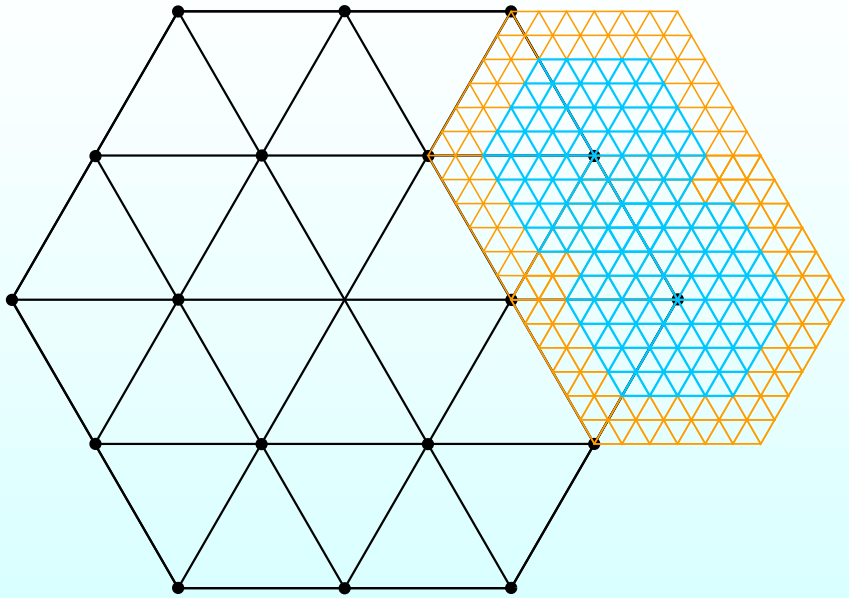
generating effective space vector structure



To get **resulting** space-vector structure, **superpose** inverter-2 space vector structure at each location of inverter-1

Superposition of Space-Vector Dagrams

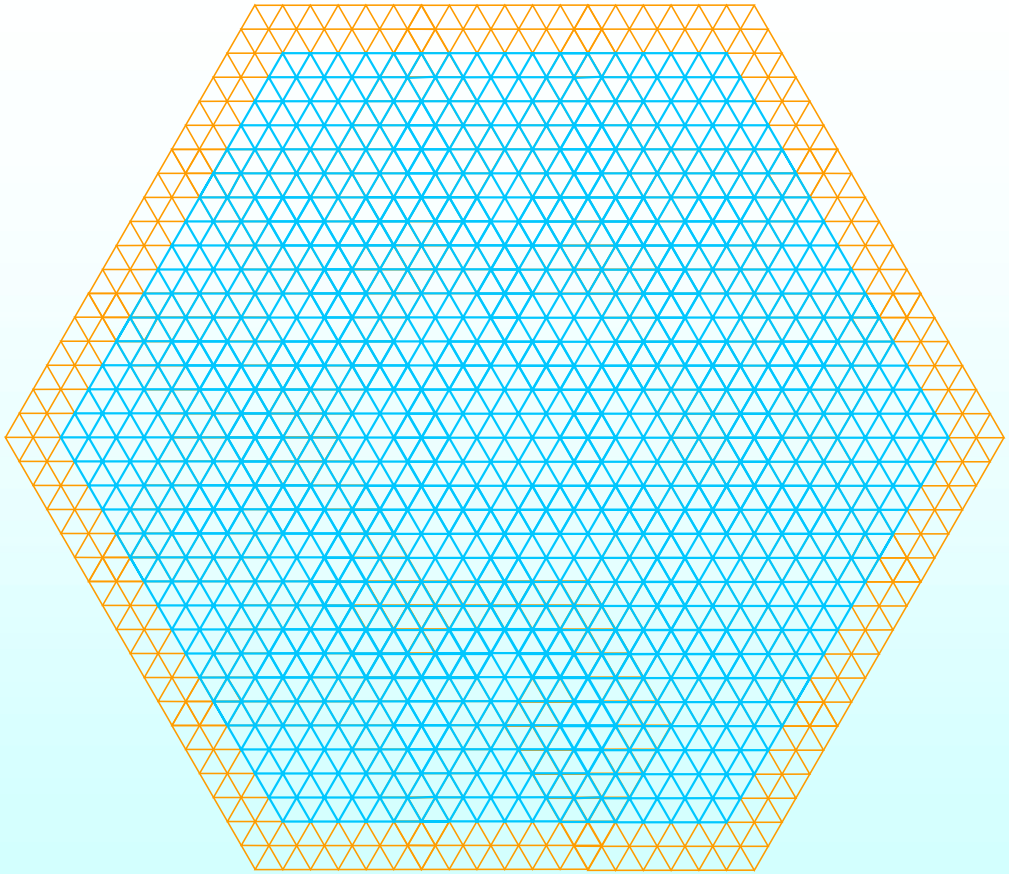
generating effective space vector structure



To get **resulting** space-vector structure, **superpose** inverter-2 space vector structure at each location of inverter-1

Superposition of Space-Vector Dagrams

generating effective space vector structure

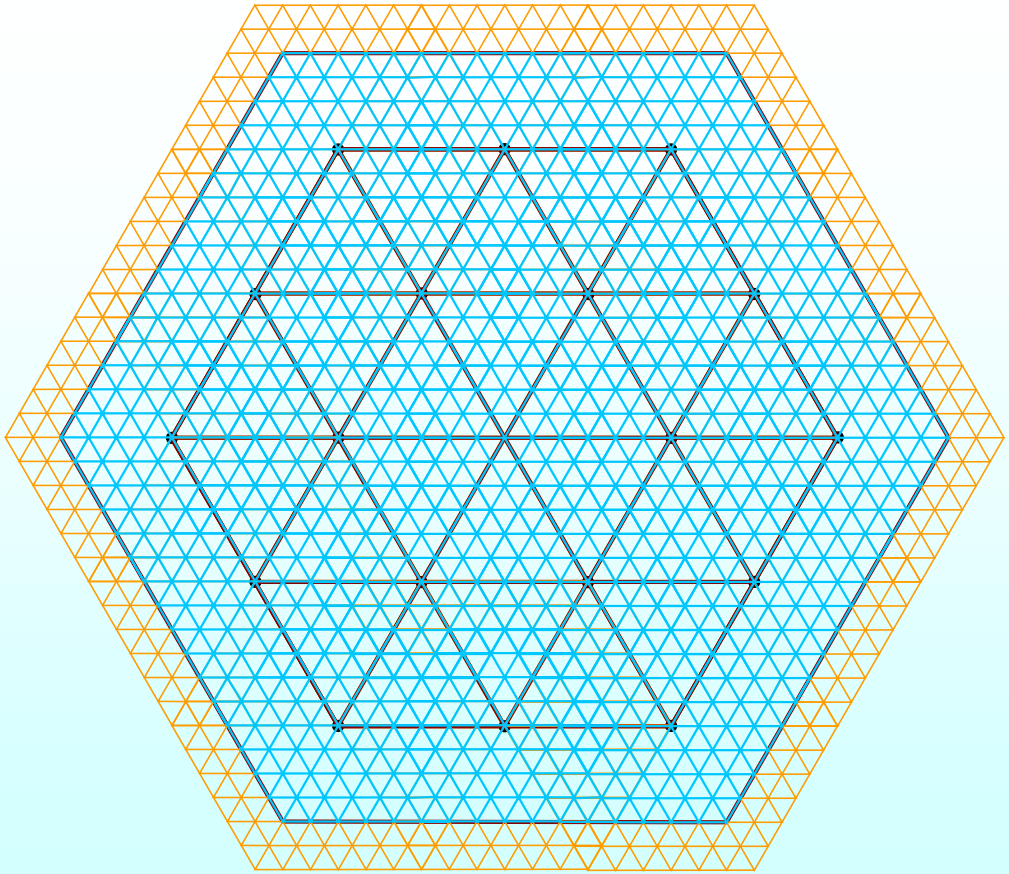


Inner region (blue)
forms a 17-Level
Space-vector Structure

Outer region (orange)
forms a 19-Level
Space-vector Structure

Superposition of Space-Vector Dagrams

generating effective space vector structure



Resulting space-vector structure is **19-level**.

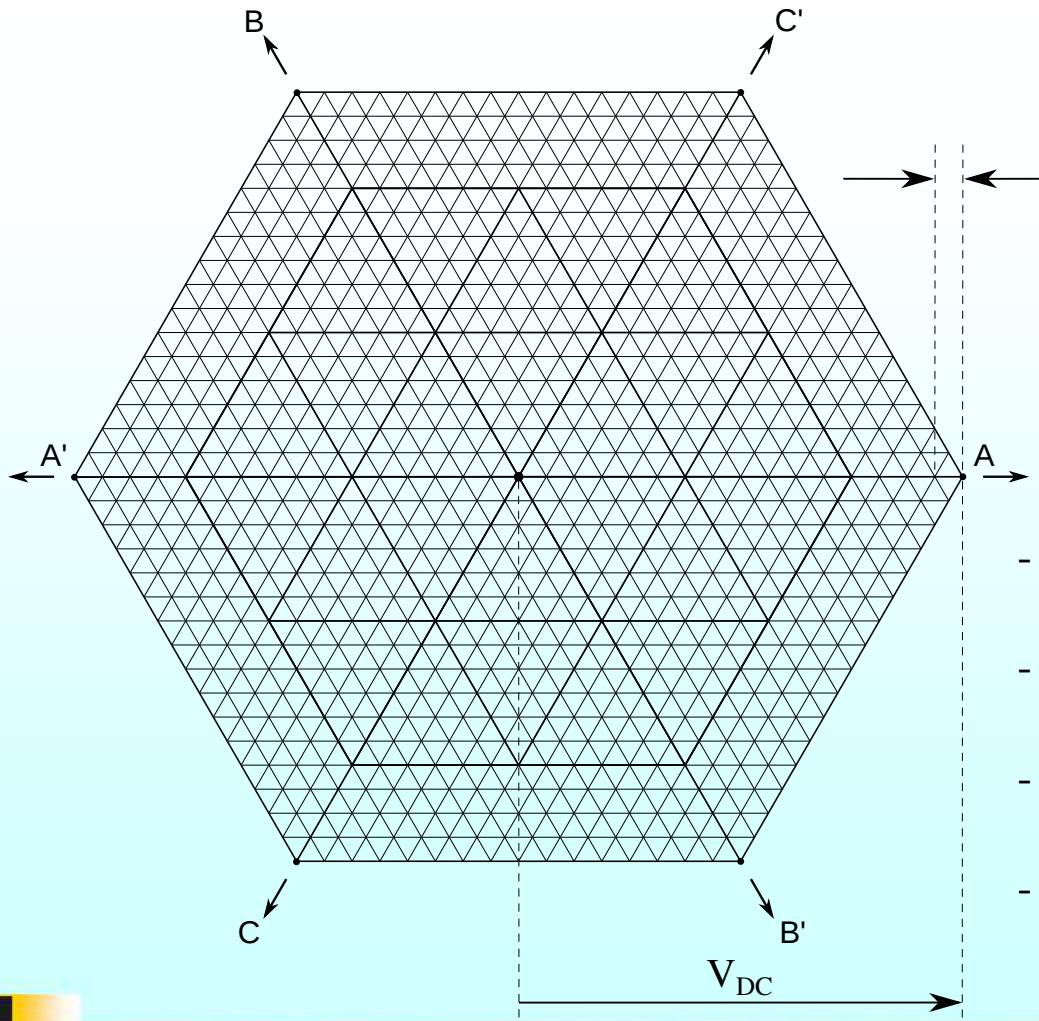
BUT, inverter cannot deliver real power in outer (orange) region

Operation limited to inner (blue) region only,

Forming a **17-level Space Vector Structure**

Superposition of Space-Vector Dagrams

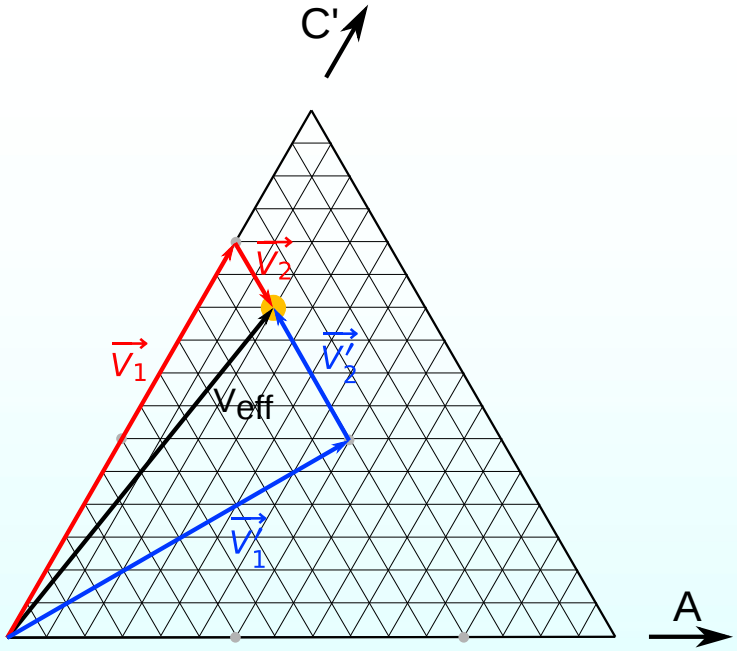
generating effective space vector structure



- 2^18≈262k switching states
- 817 space vector locations
- Radius of outermost hex = V_{DC}
- Smallest triangles of side $V_{DC}/16$

Space vector combinations

Determining individual inverter outputs



Different combination of vectors from Inverter-1 and Inverter-2 generate the same net space vector

E.g. desired space vector = V_{eff}

Case 1: $\vec{V_{eff}} = \vec{V_1} + \vec{V_2}$

Case 2: $\vec{V_{eff}} = \vec{V_1'} + \vec{V_2'}$

For each location, **vector combination**† must be chosen such that:

- Both inverters supply power
- No circulating power
- No overcharging of smaller DC supply

†A. Kshirsagar, R. S. Kaarthik, L. Umanand, K. Gopakumar, and K. Rajashekara, ***"Nine level inverter for open end induction motor with eight switches per phase,"*** in IECON 2015, DOI 10.1109/IECON.2015.7392246, Nov. 2015

Switching State Selection

- Inverter voltages vectors selected to prevent DC bus overcharging
- Inverter pole voltages and switching states selected to keep all caps balanced
- For most locations (Type-1 SVLs), these two constraints can be satisfied independently.
- For the rest (Type-2 SVLs)
  - Determine all floating cap voltages
  - Determine inveter vectors AND switching states based on cap voltages [1]

Modulation Scheme

- Level-Shifted Carrier PWM based scheme
- Only instantaneous phase voltage references required
- Usable with closed loop scalar/vector control schemes
- No recursive timing calculations required
- Current direction and cap. voltages sensed once every switching period

Experimental Results

- Steady State operation at constant frequency (10Hz - 45Hz)
- System startup and motor acceleration
- Demonstration of capacitor re-balancing after intentional unbalancing
- Prevention of DC bus overcharging

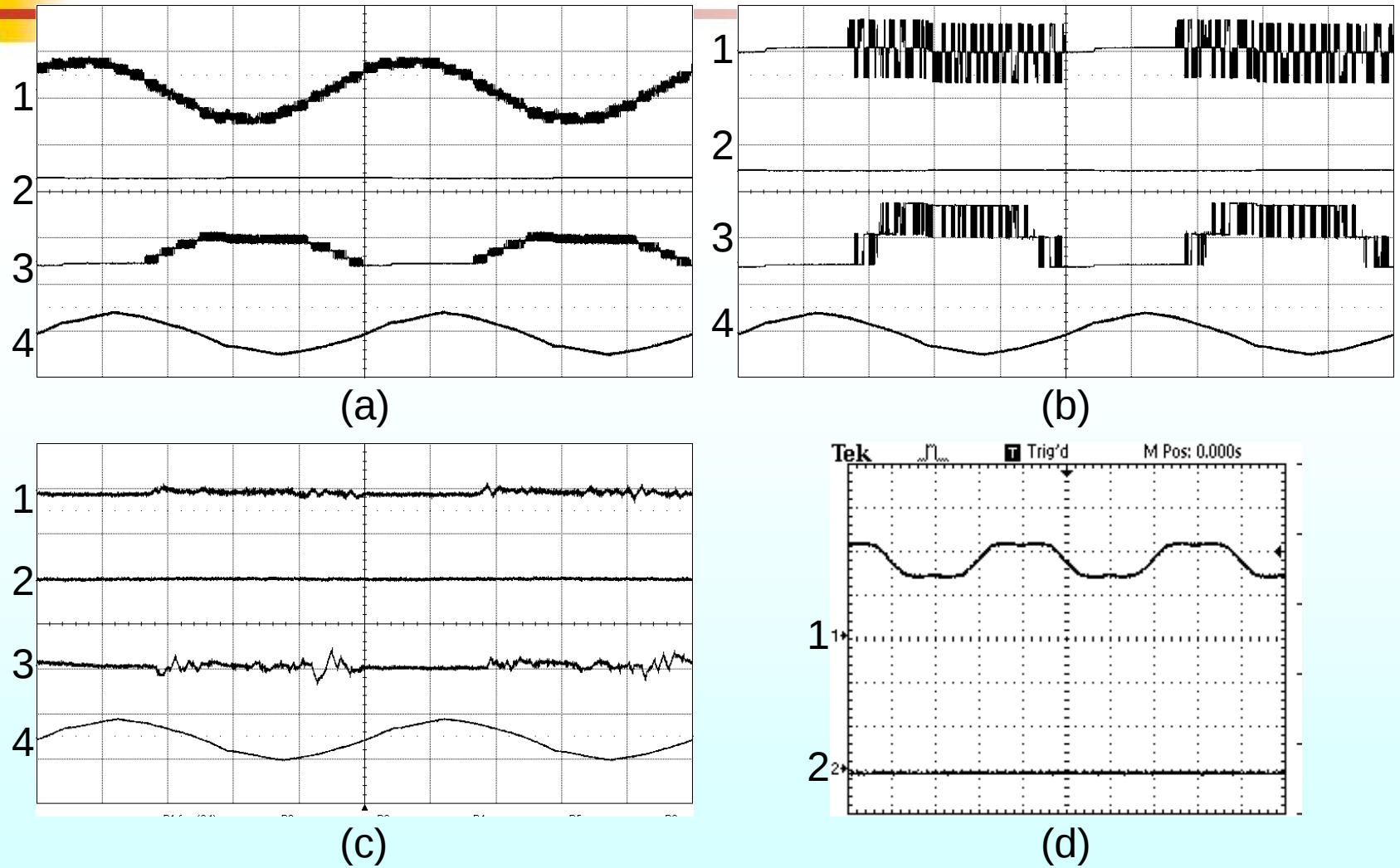


Figure 12 : 10Hz Operation: (a) VAO, VA'O', VAA', IA (b) VA'A",VAO,VA"O', IA (c) VC3A, VC1A VC1A, IA (d) VA_{ref}, Spl. Loc.

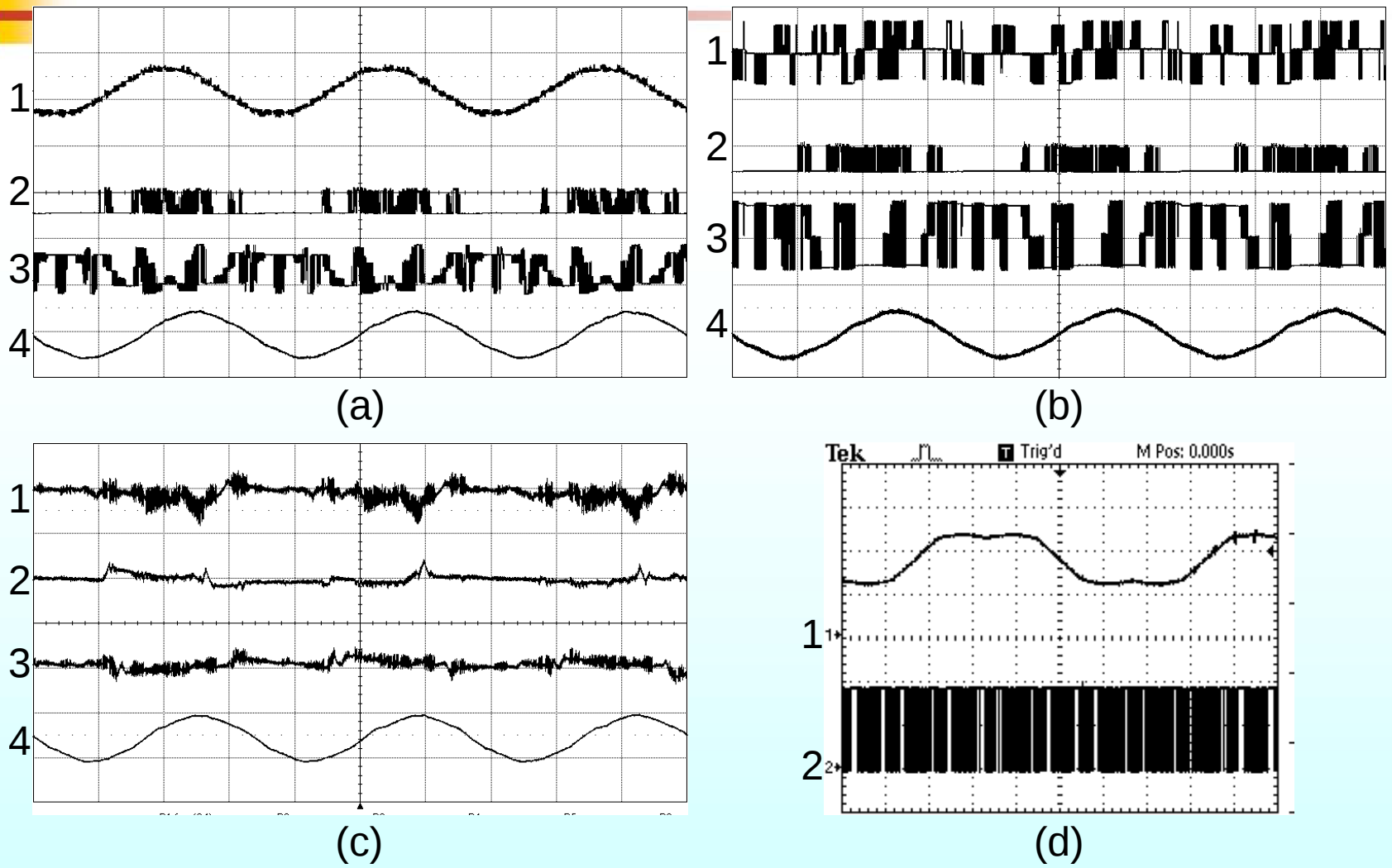


Figure 13 : 15Hz Operation: (a) VAO, VA'O', VAA', IA (b) VA'A",VAO,VA"O', IA (c) VC3A, VC1A VC1A, IA (d) VA_{ref}, Spl. Loc.

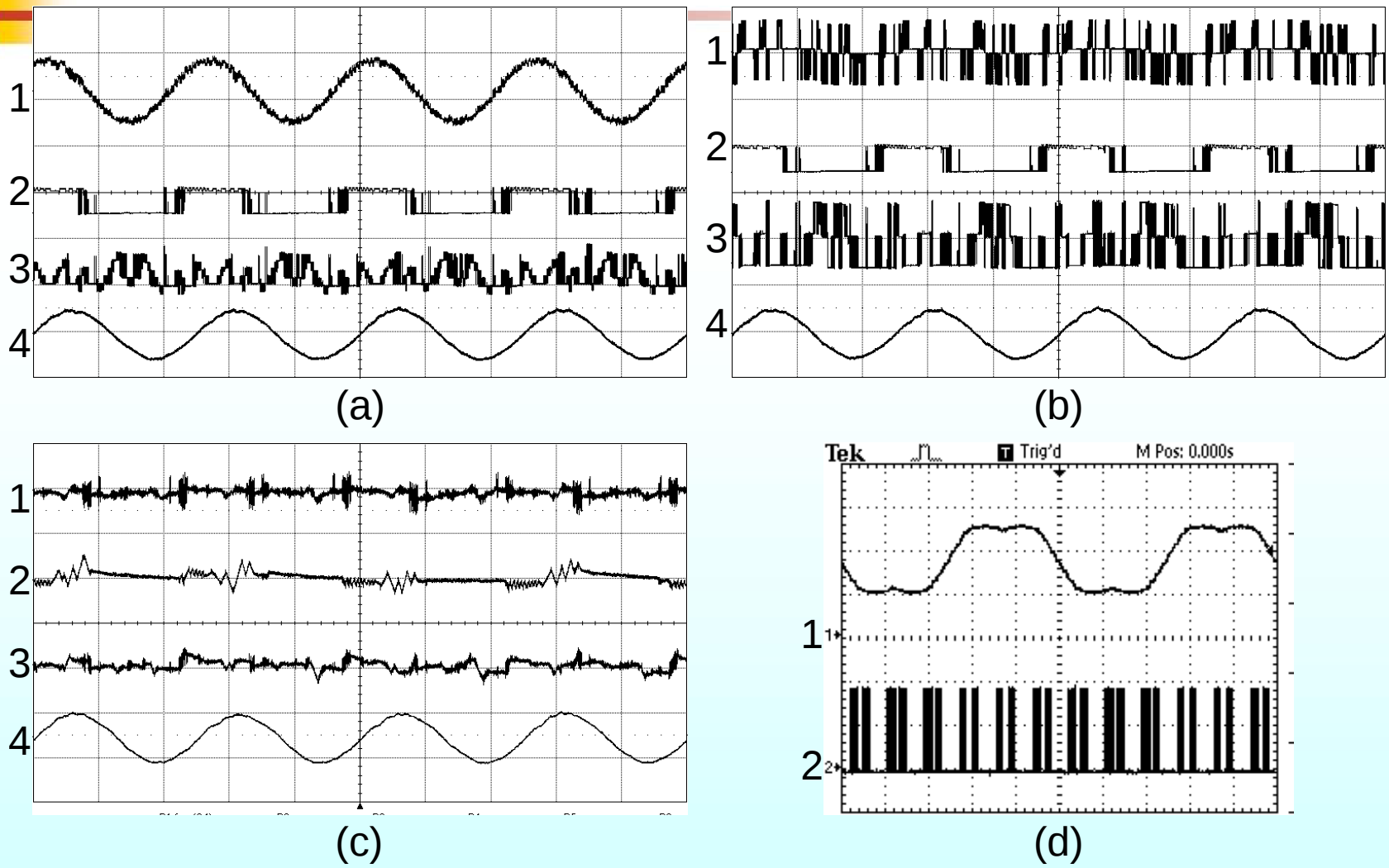


Figure 14 : 20Hz Operation: (a) VAO, VA'O', VAA', IA (b) VA'A",VAO,VA"O', IA (c) VC3A, VC1A VC1A, IA (d) VA_{ref}, Spl. Loc.

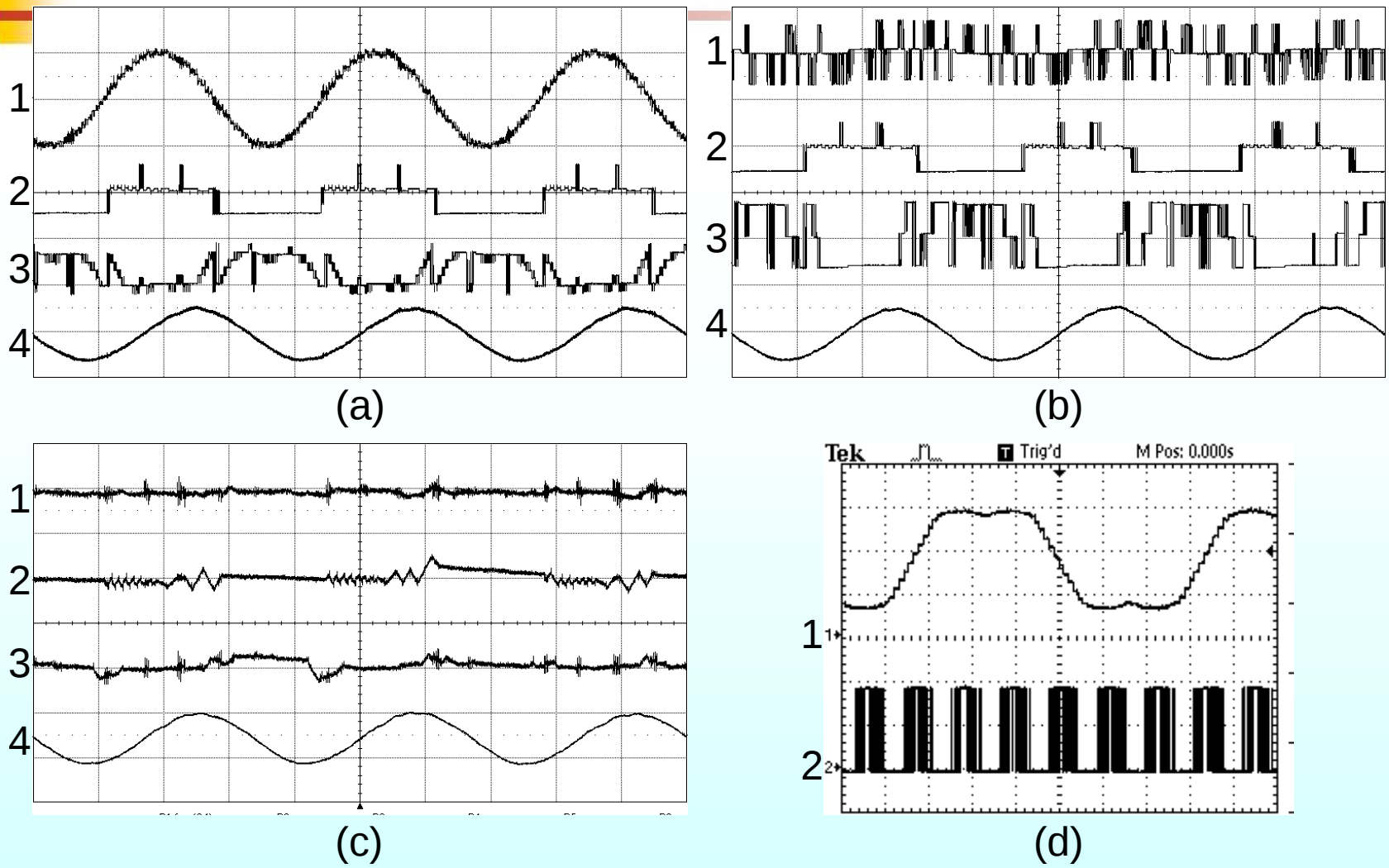


Figure 15 : 30Hz Operation: (a) VAO, VA'O', VAA', IA (b) VA'A",VAO,VA"O', IA (c) VC3A, VC1A VC1A, IA (d) VA_{ref}, Spl. Loc.

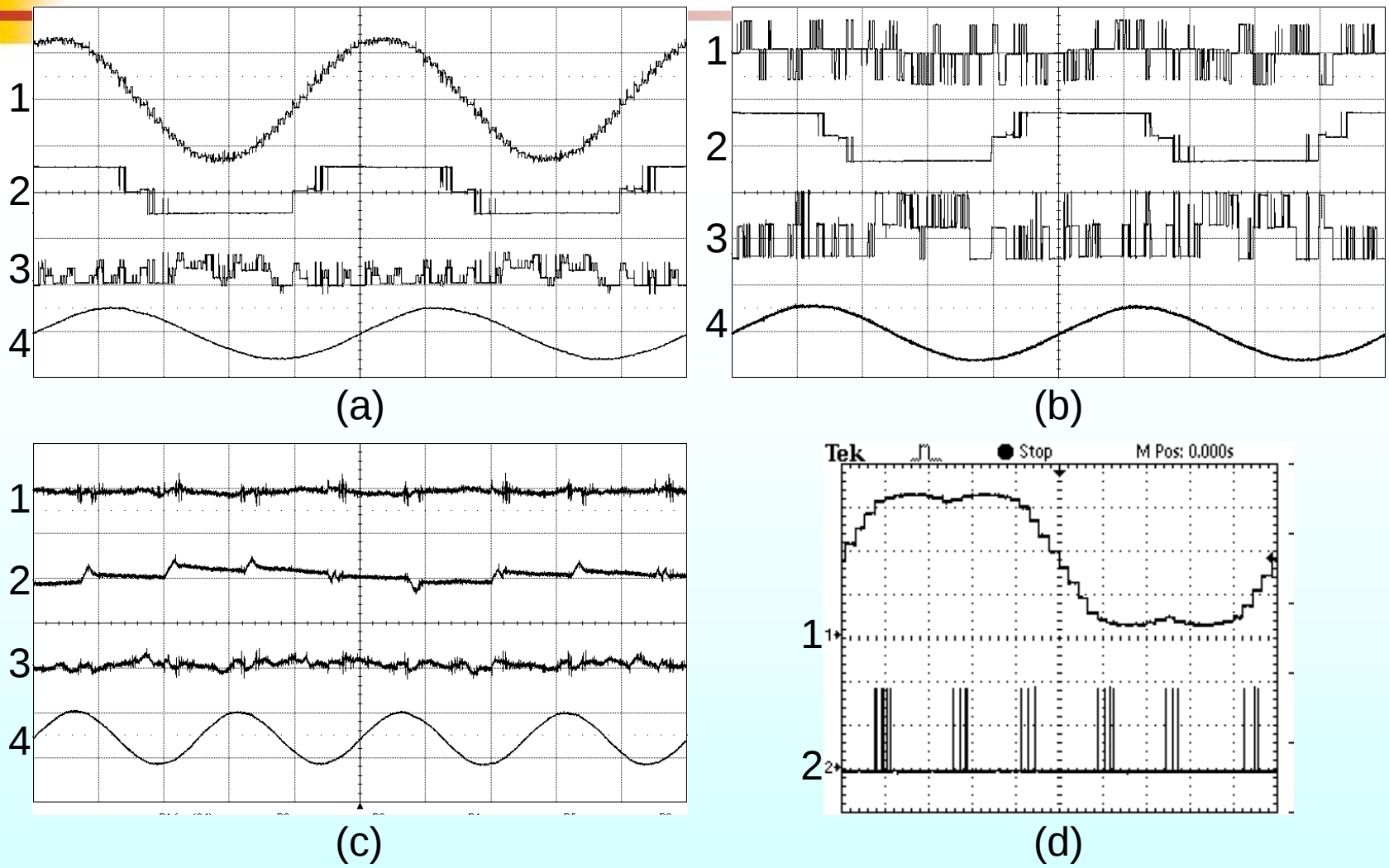


Figure 16 : 40Hz Operation: (a) VAO, VA'O', VAA', IA (b) VA'A",VAO,VA"O', IA (c) VC3A, VC1A VC1A, IA (d) VA_{ref}, Spl. Loc.

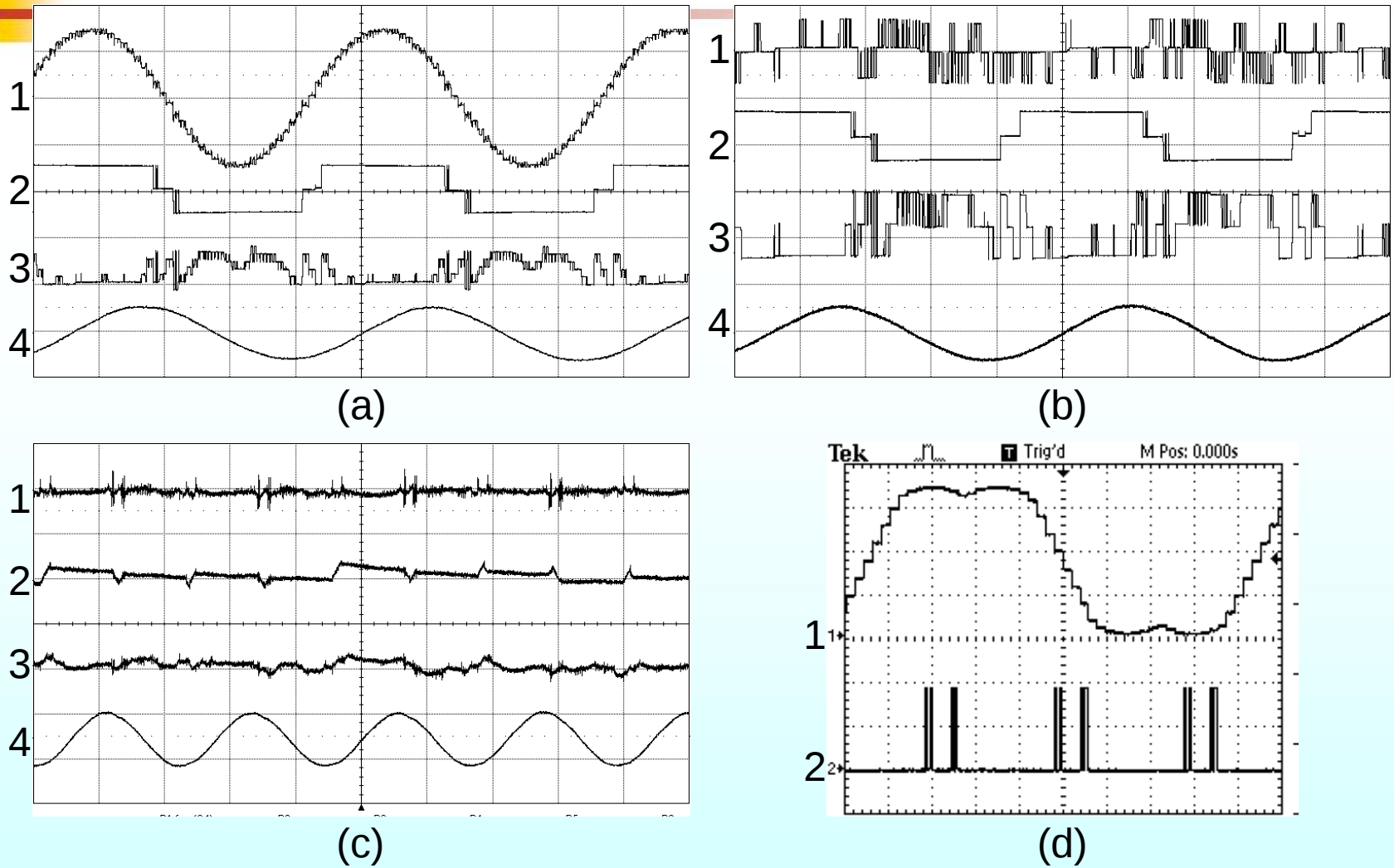


Figure 17 : 45Hz Operation: (a) VAO, VA'O', VAA', IA (b) VA'A",VAO,VA"O', IA (c) VC3A, VC1A VC1A, IA (d) VA_{ref}, Spl. Loc.

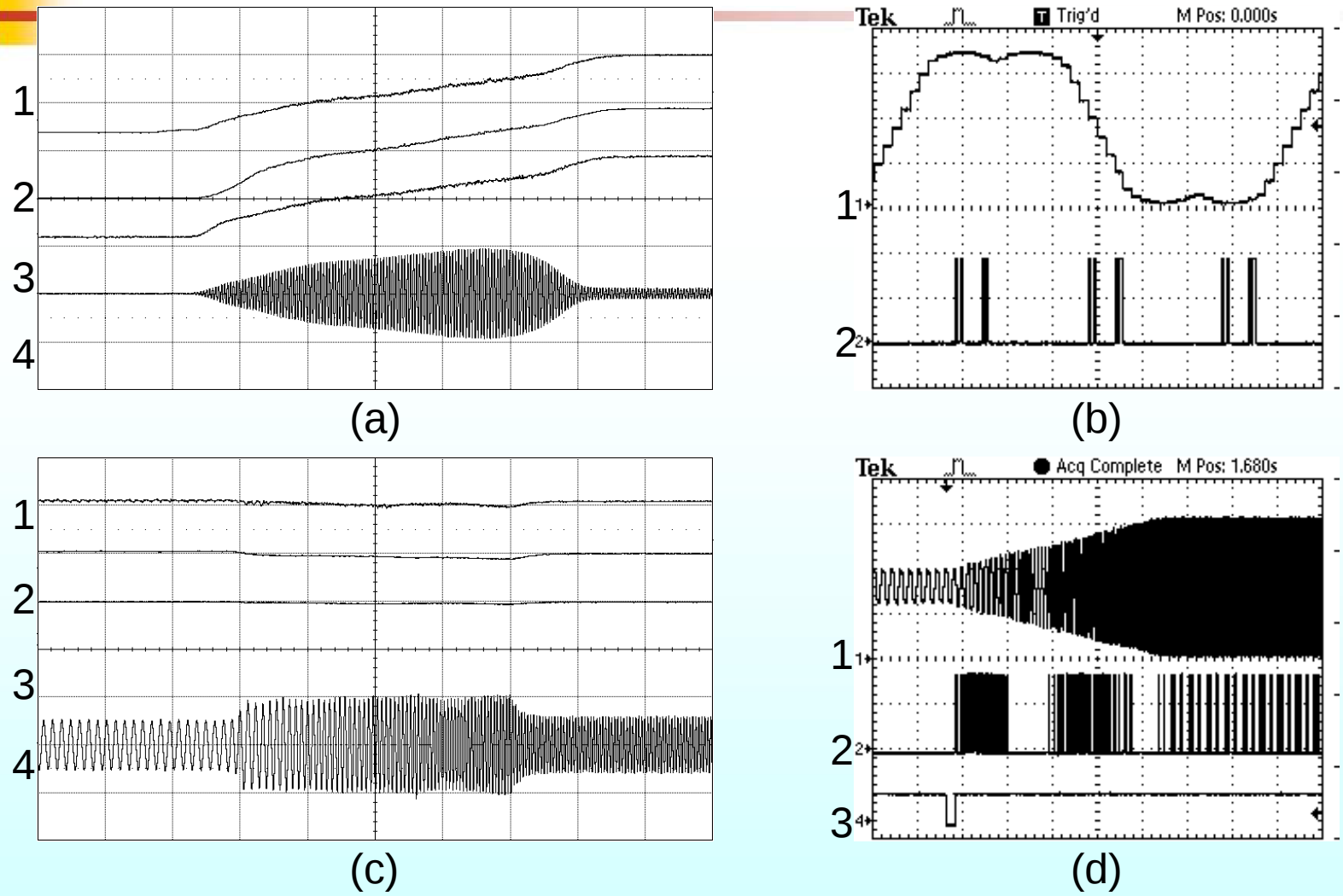


Figure 18 : (a) (Startup) VC3A, VC1A VC1A, IA (b) VA_{ref}, Spl. Loc. (c) (Acceleration, 15-45Hz in 2sec) VC3A, VC1A VC1A, IA (d) VA_{ref}, Spl. Loc.

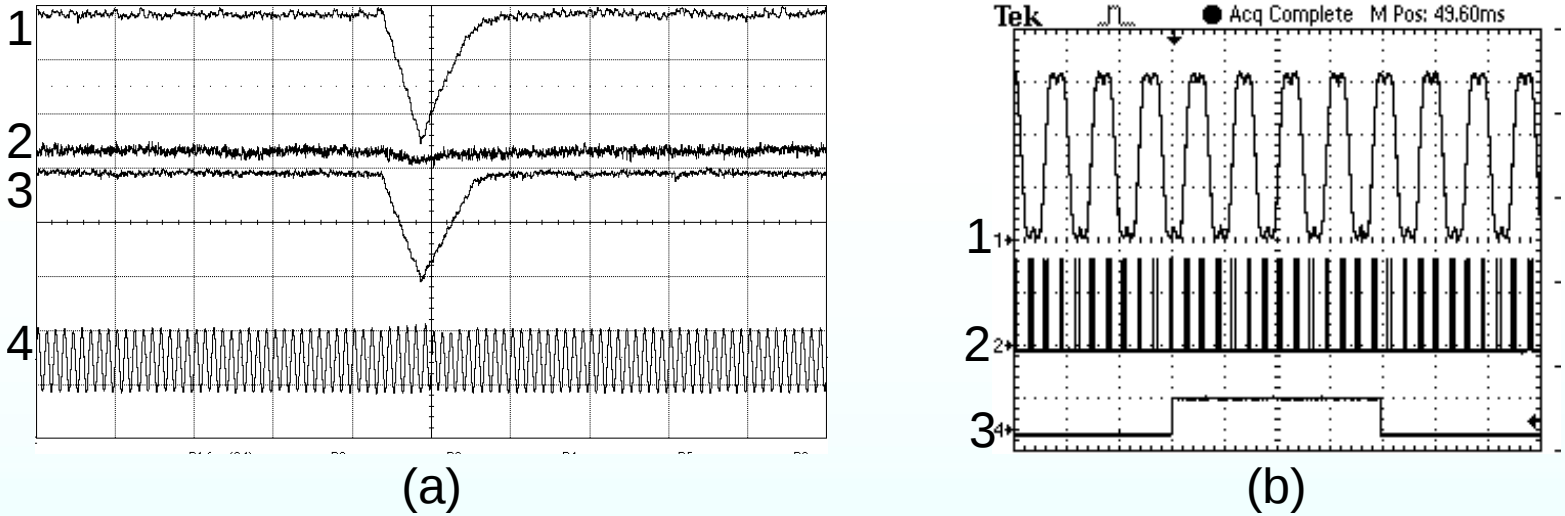


Figure 19 : (a) Capacitor voltage waveforms. X-Axis: 20ms/div. (1) CH3 Ripple in flying capacitor C2A, (AC coupled) (Y -axis: 2V/div). (2) CH2 Ripple in flying capacitor C1A, (AC coupled) (Y -axis: 20V/div). (3) CH1 Ripple in CHB capacitor C3A, (Y -axis: 5mV/div). (4) A Phase current (Y -axis: 1A/div). (b) Phase Voltage Reference (VA_{ref}), Spl. Loc., Forced Discharge duration

Summary

A new 17-level inverter topology proposed for open-end induction motor,
with

- Reduced component count: Only twelve switches and three capacitors per phase
- Capacitor voltage balancing at switching frequency
  - Over entire linear modulation range
  - Any load power factor
- Iteration-less modulation and switching control scheme
- Elimination of circulating power

Setup for experiments

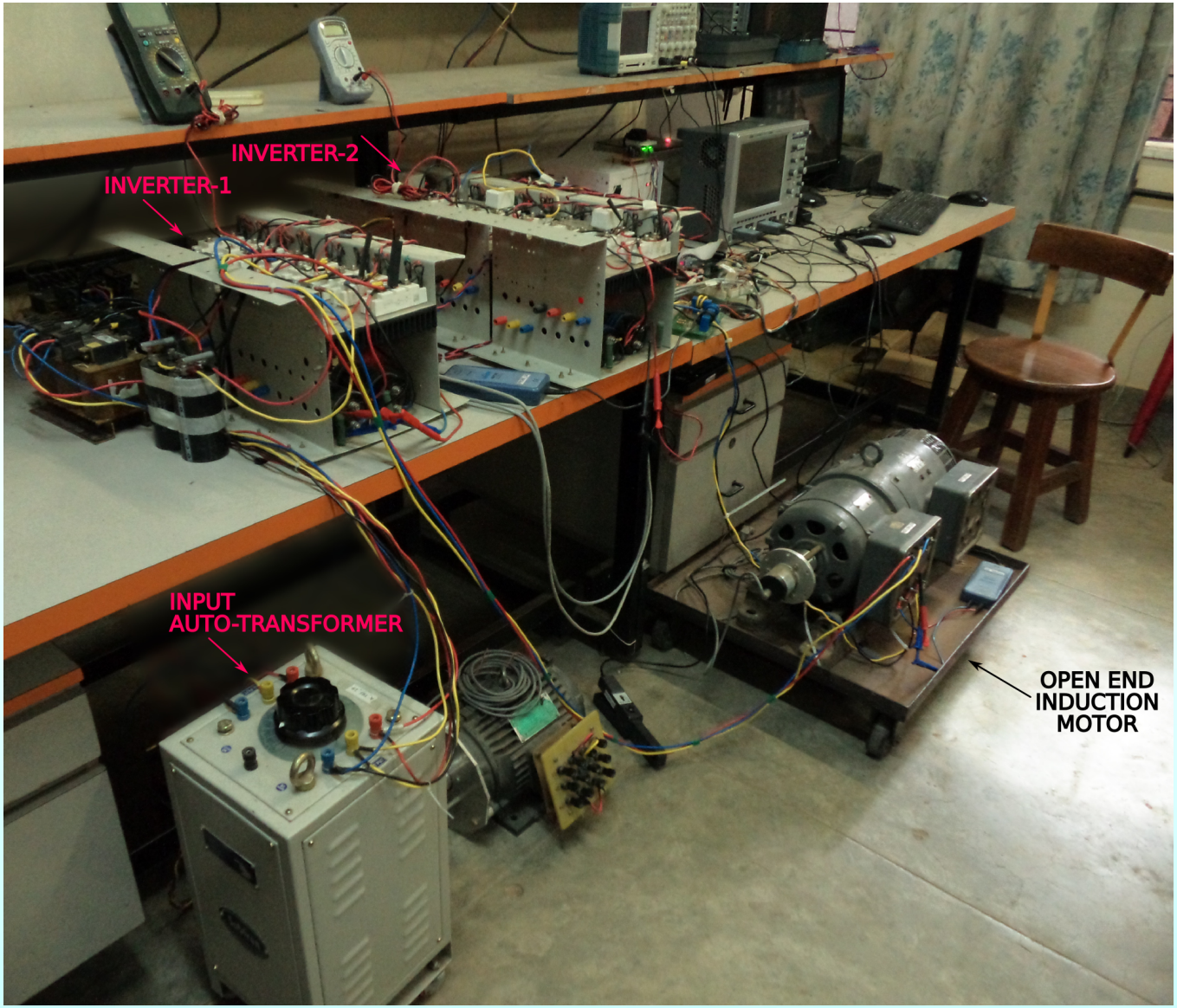


Figure 20 : Experimental Setup

Setup for experiments

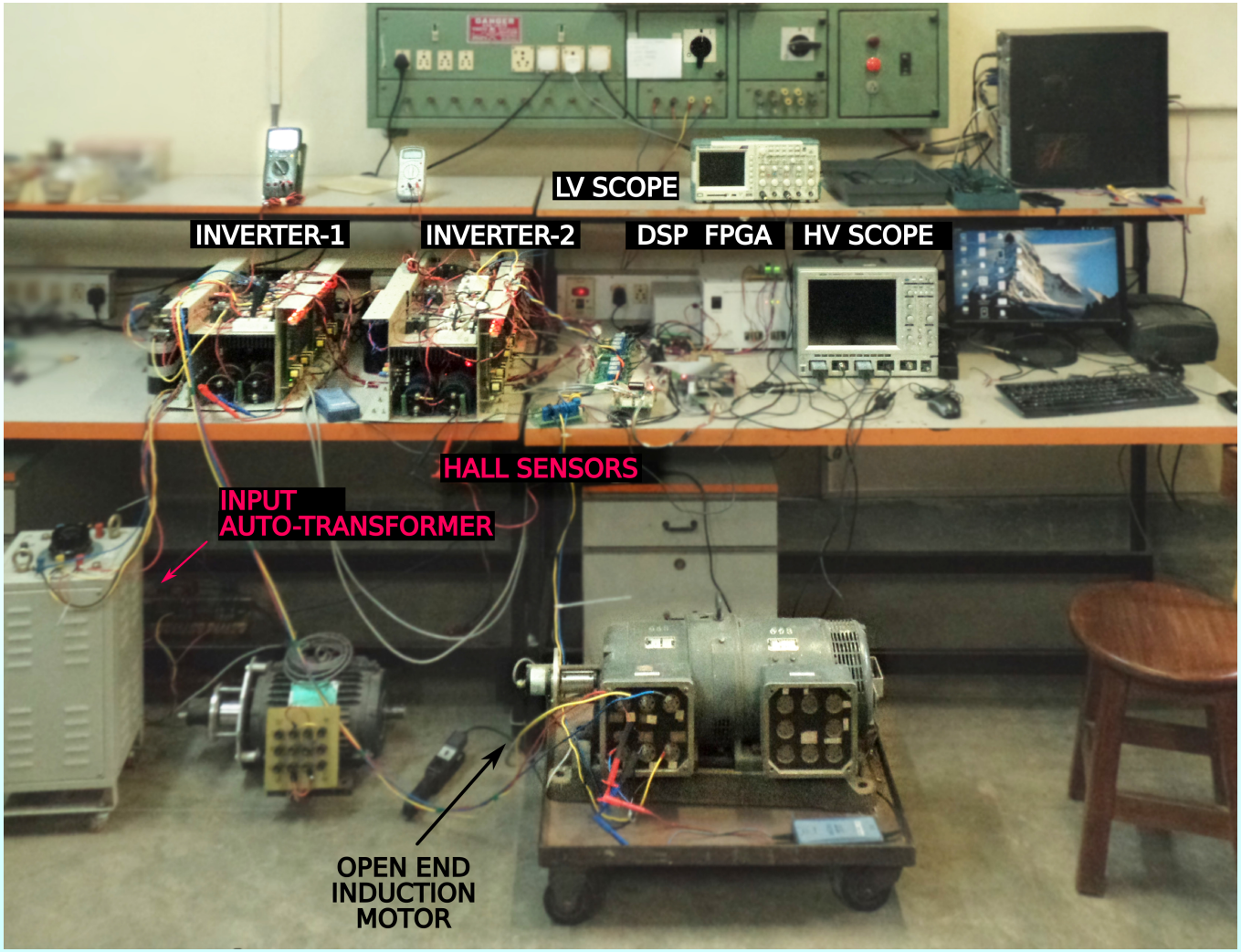


Figure 20 : Experimental Setup

THANK YOU

Multilevel Dodecagonal and Octadecagonal Voltage Space Vector Structures With a Single DC Supply Using Basic Inverter Cells

Mathews Boby
Research Supervisors: Prof. K Gopakumar & Prof. L Umanand
Department of Electronic Systems Engineering (DESE),
Indian Institute of Science,
Bangalore-12, India.
13/04/2017

Outline

- Introduction
  - Induction motor drive (IMD) systems
  - 2-level 3-phase voltage source inverter (VSI)
  - Hexagonal voltage space vector structure (Hex-VSVS)
  - Multilevel VSI
  - Harmonics
- Dodecagonal VSVS (Dod-VSVS)
  - Features & advantages
  - Prior works
- Octadecagonal VSVS (Oct-VSVS)
  - Features & advantages
  - Prior works
- Motivation for research

Outline…

- Six-Concentric-Dodecagonal Voltage Space Vector Structure for Open-End Winding IMDs Using a Single DC Source
  - Dod-VSVS using single DC source
  - Topology
  - PWM scheme
  - Capacitor balancing & design
  - Implementation
  - Results
- Six-Concentric-Dodecagonal Voltage Space Vector Structure for Star Connected IMDs Using a Single DC Source
  - Topology
  - PWM scheme
  - Capacitor balancing & design
  - Implementation
  - Results

Outline…

- Nine-Concentric-Octadecagonal Voltage Space Vector Structure for IMDs Using a Single DC Source
  - Oct-VSVS using single DC source
    - Two-level
    - Extension to multilevel
  - Topology
  - PWM scheme
  - Capacitor balancing & design
  - Implementation
  - Results
- Conclusion

Induction Motor Drive Systems

- Induction motors are widely used in industrial applications, reasons being
  - Simple construction / low cost
  - Rugged / maintenance free / long life
- Variable speed induction motor drive (IMD) system:

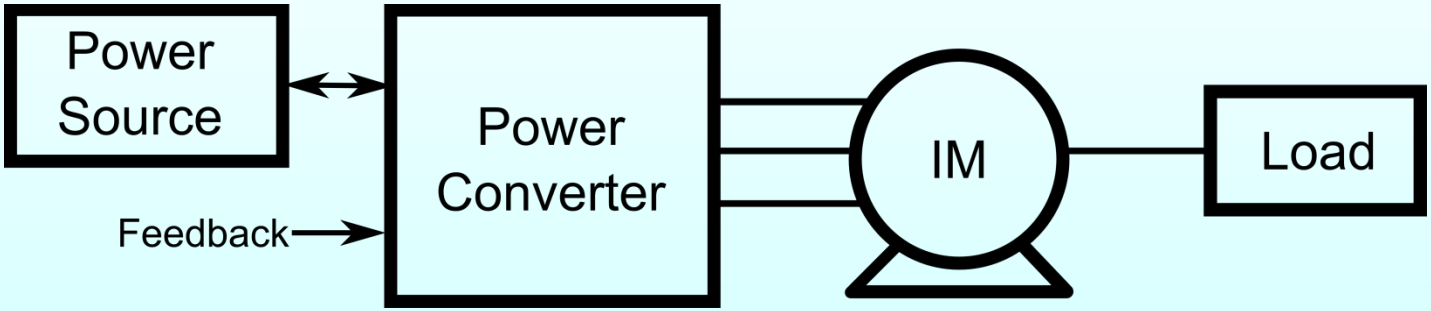


Fig: IMD System

- Focus is on the power converter, to make the system
  - Lower cost, smaller size, lower weight
  - Reliable, efficient

2-Level 3-Phase Voltage Source Inverter

- Power circuit topology:
  - 6 switches / 3 half-bridges
  - $V_{XO} = \left[-\frac{V_{dc}}{2}, +\frac{V_{dc}}{2}\right];\ X = A, B, C$
  - State '1':
    - Top switch ON
    - Bottom switch OFF
  - $2^3 = 8$ switching states in total

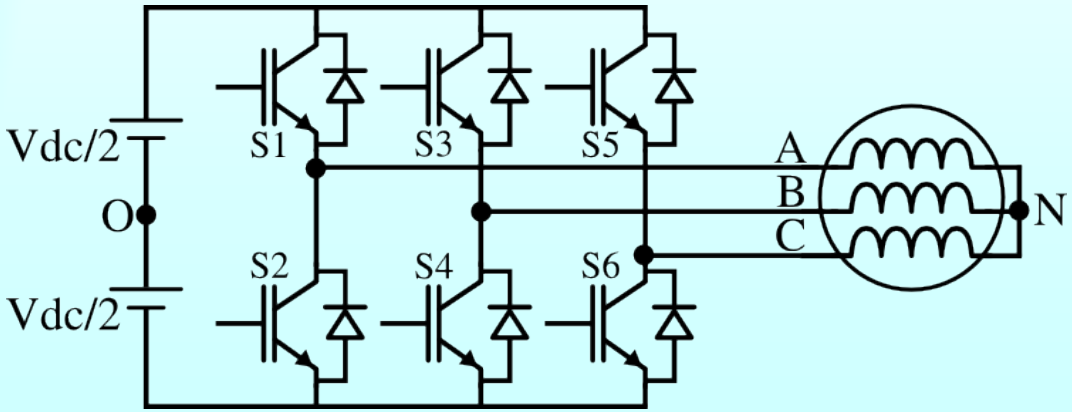


Fig: 2-level VSI topology

Table 1: 2-level Inverter Switching States

State	V_{AO}	V_{BO}	V_{CO}
100	$+\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$
110	$+\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$
010	$-\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$
011	$-\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$
001	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$
101	$+\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$
000	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$
111	$+\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$

Hexagonal Voltage Space Vector Structure

- VSVS from 2-level VSI:
  - Obtained by plotting V_A, V_B, V_C in a 2D plane ($\alpha\beta$ plane) using:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix}$$

  - Reference vector inside the hexagon can be synthesized as:

$$V_{ref} T_s = V_0 T_0 + V_6 T_1 + V_5 T_2$$
$$T_s = T_0 + T_1 + T_2$$

  - Radius of the in-circle: $\frac{\sqrt{3}}{2} V_{dc} = 0.866 V_{dc}$
  - Peak phase fundamental output
    - Linear modulation range: $\frac{2}{3} * 0.866 V_{dc} = 0.577 V_{dc}$
    - 6 step mode (M=1): $0.637 V_{dc}$

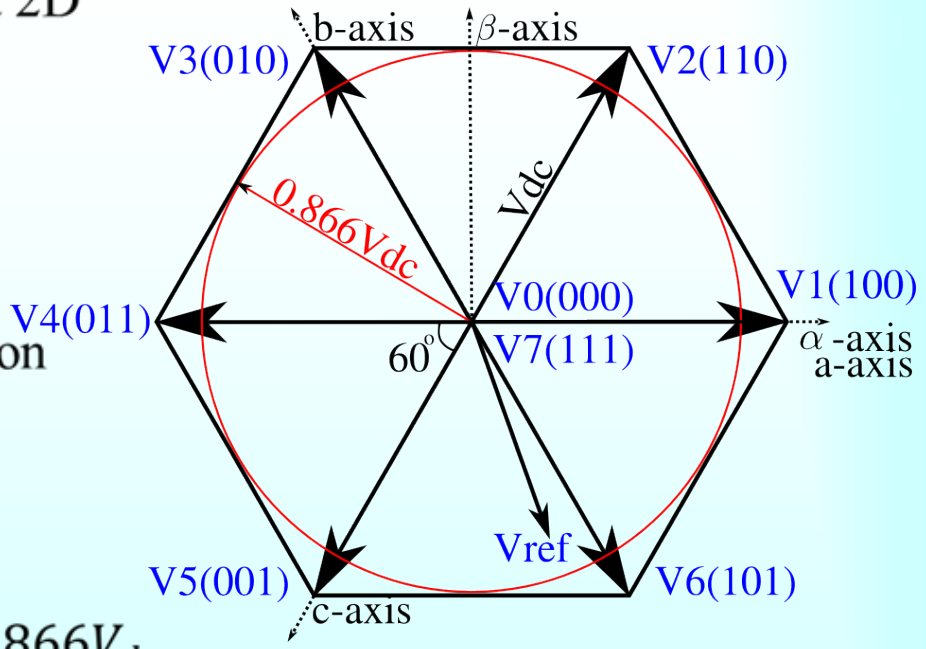
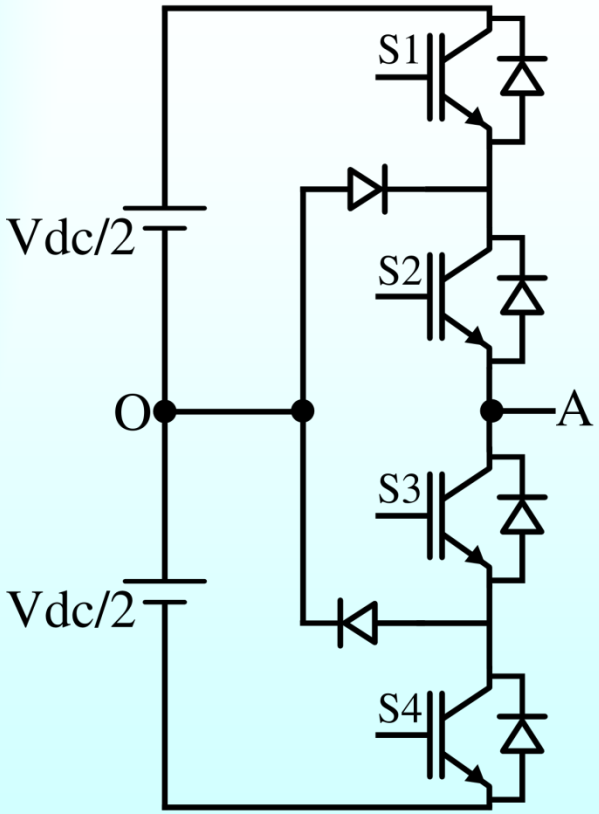


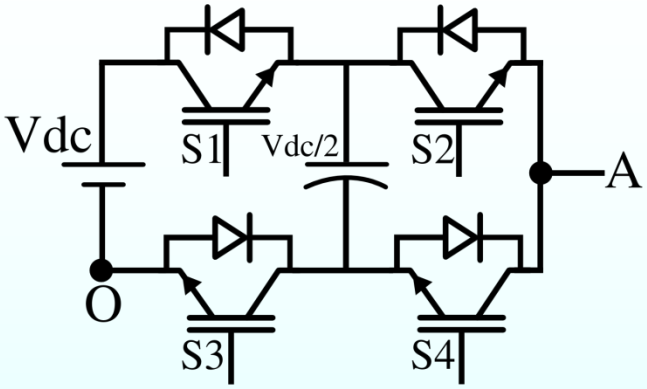
Fig: 2-level Hex-VSVS

Multilevel VSI

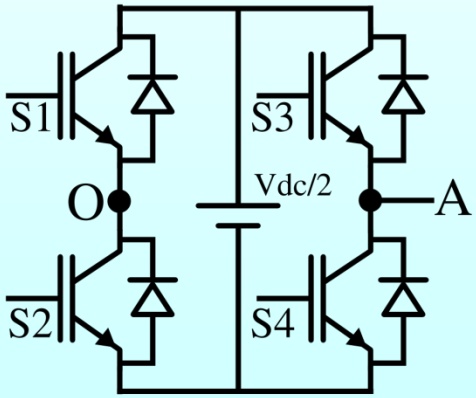
- Commonly used multilevel VSI topologies & VSVS:



(a) 3L- Diode Clamped Inverter/
Neutral Point Clamped Inverter

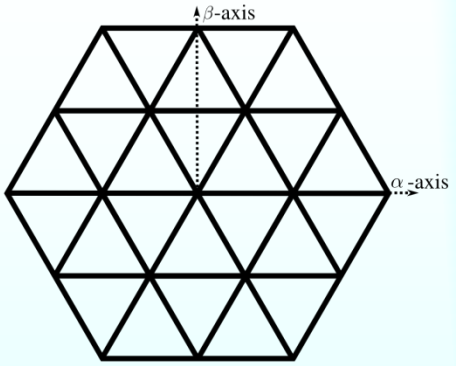


(b) 3L- Flying Capacitor Inverter

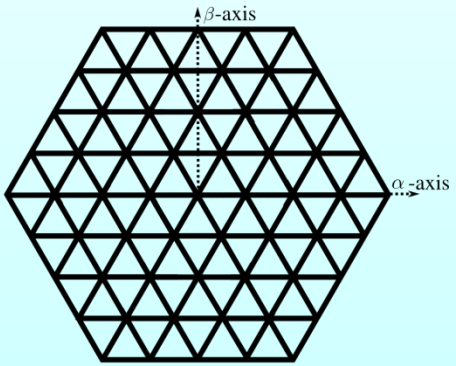


(c) H-Bridge Inverter

Fig: Multilevel Topologies



(a) 3L VSVS



(b) 5L VSVS

Fig: VSVS of Multilevel Topologies

Hexagonal Voltage Space Vector Structure…

- In six-step mode / M=1:
  - Peak phase fundamental output is: $V_1 = 0.637V_{dc}$
  - Harmonic content of V_{XN}:
    - $V_n = \frac{1}{n}V_1; n = 5,7,11,13 \ldots$
    - Creates harmonic currents
- Problems with harmonics:
  - Creates torque pulsations
    - $6^{th}, 12^{th}, \ldots$ order torque ripple
  - Affects closed loop current control
    - Requires filtering
  - Power loss due to harmonic currents

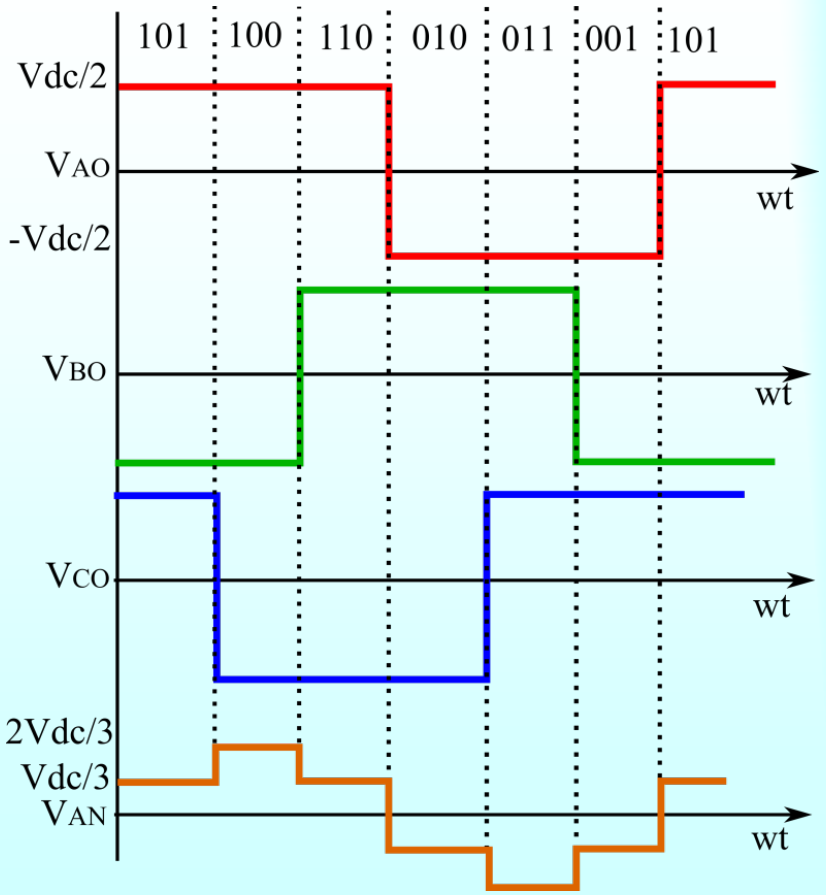


Fig: Waveforms during extreme overmodulation

Harmonic Elimination & Suppression

- Harmonic current suppression:
  - Use high frequency PWM
    - Higher switching losses
    - EMI issues
    - Good only in linear modulation range
  - Selective Harmonic Elimination PWM
    - Limited modulation range
    - Requires offline computations
  - Use passive filters
    - Efficiency degradation
    - Bulky, good for high frequency harmonics
    - Unsuitable for variable frequency operation
    - DC-link utilization is poor
  - Voltage space vector structures with more number of sides (12, 18, …)

Dodecagonal VSVS

- Dodecagonal Structure:
  - Boundary is a 12 sided polygon
  - 12 active vectors separated at 30^o angle
  - Vectors of magnitude V_d
- Projection of vectors on α-axis and scaling by 2/3 gives A-phase voltage

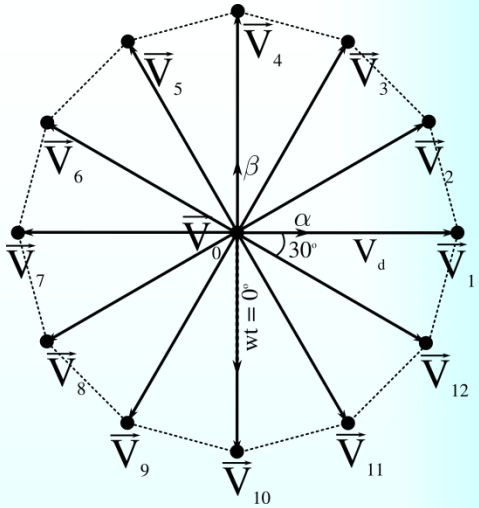


Fig: Dodecagonal space vector structure

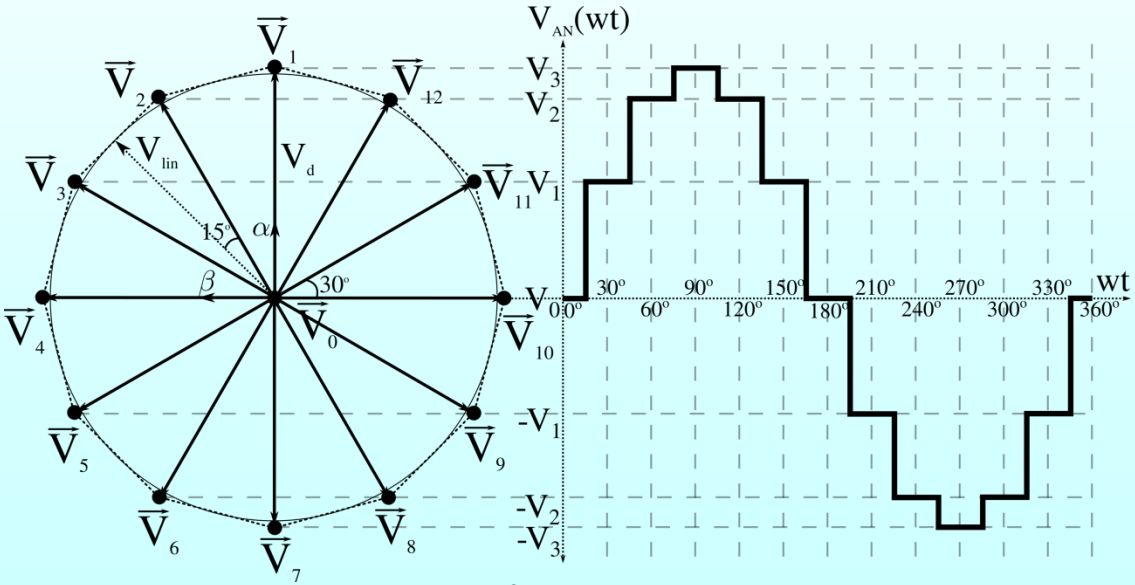


Fig: Phase voltage from dodecagonal structure

$$V_0 = 0$$
$$V_1 = 2/3 V_d cos(60^o)$$
$$V_2 = 2/3 V_d cos(30^o)$$
$$V_3 = 2/3 V_d$$

Dodecagonal VSVS - Harmonics

- Harmonics spectrum:

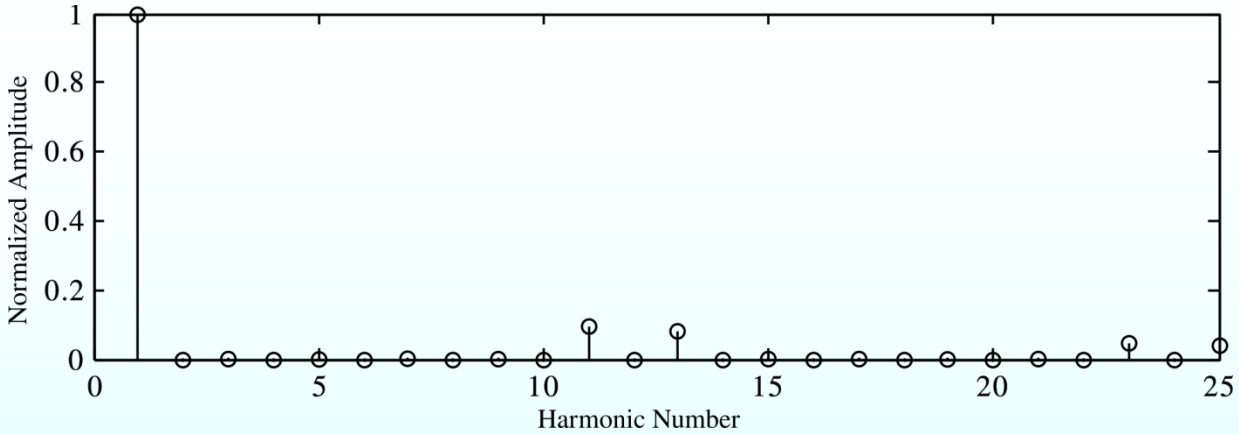


Fig: Harmonic spectrum of phase voltage from dodecagonal structure

- $6n \pm 1; n = odd$ order harmonics are absent
  - $5^{th}, 7^{th}, 17^{th}, 19^{th}$ ... harmonics are eliminated form the phase voltage
- $12n \pm 1; n = 1, 2, 3$ ... order harmonics are present
- Peak phase fundamental output is:
  - 50Hz operation, 12-step mode, M = 1: $V_{ppf-dod} = 0.659V_d$
  - Linear modulation range is $V_{lin} = \frac{2}{3}V_d \cos(15^o) = 0.644V_d$

Dodecagonal VSVS - Advantages

- Complete elimination of $6n \pm 1; n = odd$ order harmonics from the phase voltage over entire modulation range:
  - Absence of 6^{th} order torque ripple, smooth torque generation
  - Output filtering requirements could be avoided or relaxed
  - Easy current control loop design

- Linear modulation range is extended till 97.7% of base speed compared to 90.58% in a hexagonal structure
  - Hexagonal structure: $\frac{0.577V_{dc}}{0.637V_{dc}} = 90.58\% \equiv 45.3Hz$ (M=0.906)
  - Dodecagonal structure: $\frac{0.644V_{d}}{0.659V_{d}} = 97.7\% \equiv 48.86Hz$ (M=0.977)

  (For base speed of 50Hz)

Octadecagonal VSVS

- Octadecagonal Structure:
  - Boundary is an 18 sided polygon
  - 18 active vectors separated at 20^o angle
  - Vectors of magnitude V_{oct}
- Projection of vectors on α-axis and scaling by 2/3 gives A-phase voltage

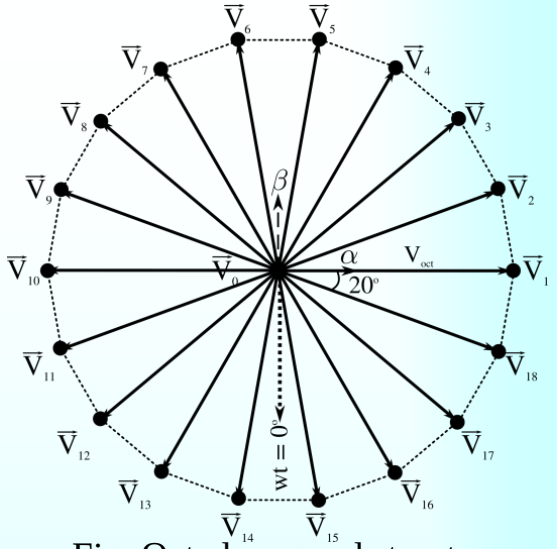


Fig: Octadecagonal structure

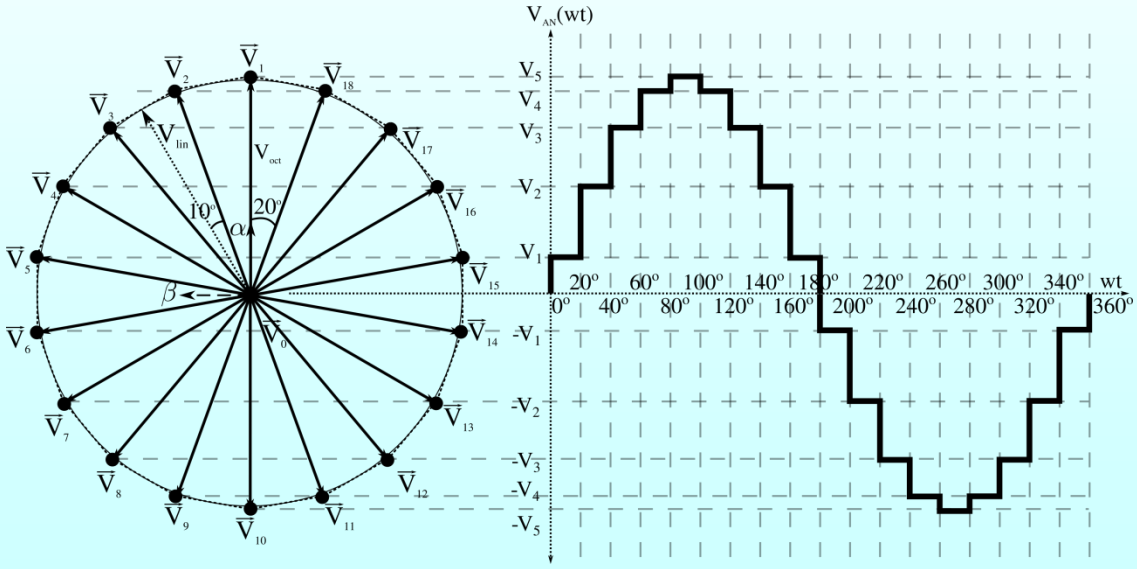


Fig: Phase voltage from octadecagonal structure

$$V_5 = \frac{2}{3} V_{oct}$$

$$V_4 = \frac{2}{3} V_{oct} cos(20^o)$$

$$V_3 = \frac{2}{3} V_{oct} cos(40^o)$$

$$V_2 = \frac{2}{3} V_{oct} cos(60^o)$$

$$V_1 = \frac{2}{3} V_{oct} cos(80^o)$$

Octadecagonal VSVS - Harmonics

- Harmonics spectrum:

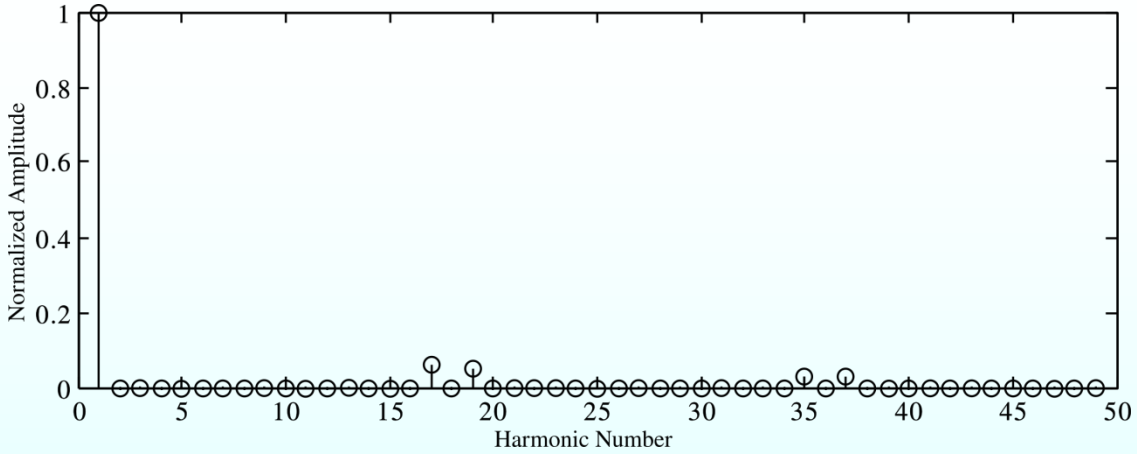


Fig: Harmonic spectrum of phase voltage from octadecagonal structure

- $6n \pm 1; n = 1, 2, 4, 5, \ldots$ order harmonics are absent
  - $5^{th}, 7^{th}, 11^{th}, 13^{th}$ ... harmonics are eliminated form the phase voltage
- $18n \pm 1; n = 1, 2, 3$ ... order harmonics are present
- Peak phase fundamental output is:
  - 50Hz / 18 step operation / M=1: $V_{ppf-oct} = 0.663V_{oct}$
  - Linear modulation range is $V_{lin} = \frac{2}{3}V_{oct}\cos(10^o) = 0.656V_{oct}$

Octadecagonal VSVS - Advantages

- Complete elimination of $6n \pm 1; n = 1, 2, 4, 5, \ldots$ order harmonics from the phase voltage over entire modulation range:
  - Absence of $6^{th}, 12^{th}$ order torque ripple, smooth torque generation
  - Output filtering requirements could be avoided or relaxed
  - Easy current control loop design

- Linear modulation range is extended till 99% of base speed
  - Hexagonal structure: $\frac{0.577V_{dc}}{0.637V_{dc}} = 90.58\% \equiv 45.3Hz$ (M=0.906)
  - Dodecagonal structure: $\frac{0.644V_{d}}{0.659V_{d}} = 97.7\% \equiv 48.86Hz$ (M=0.977)
  - Octadecagonal structure: $\frac{0.656V_{oct}}{0.663V_{oct}} = 99\% \equiv 49.5Hz$ (M=0.99)

    (For base speed of 50Hz)

Dodecagonal VSVS – Prior Works

- 2-level dodecagonal space vector structure for open-end winding IM

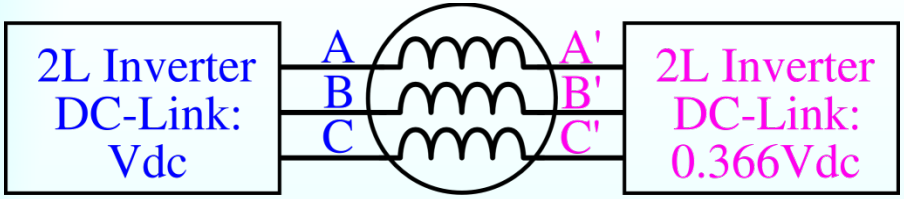


Fig: Topology for 2-level Dod-VSVS

- Requires 2 DC sources delivering active power
- DC links: V_{dc} & $0.366V_{dc}$
- Only 2 level operation

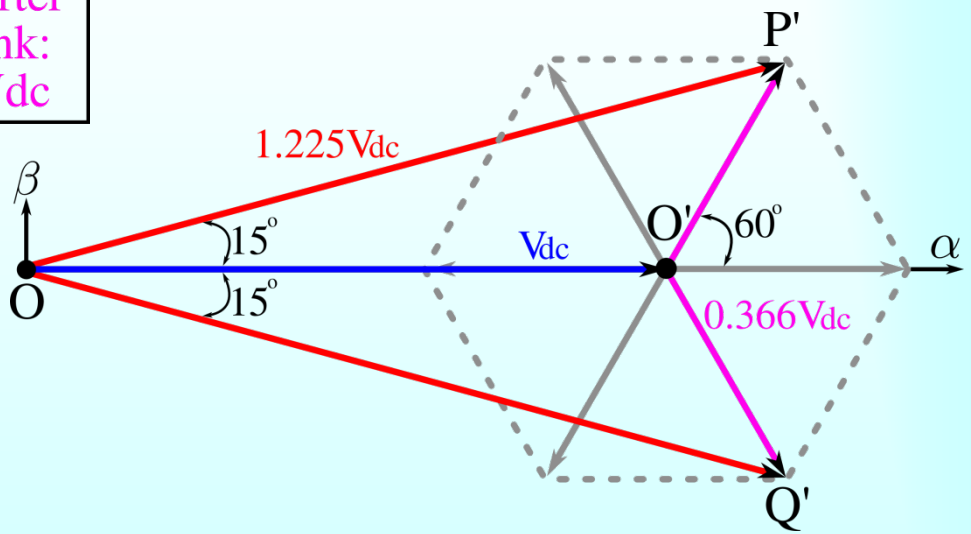


Fig: Dodecagonal vector generation

- [1] K. Mohapatra, K. Gopakumar, V. Somasekhar, and L. Umanand, "A harmonic elimination and suppression scheme for an open-end winding induction motor drive," IEEE Trans. Ind. Electron., vol. 50, pp. 1187–1198, Dec 2003.

Dodecagonal VSVS – Prior Works

- Multilevel dodecagonal space vector structure for open-end winding IM

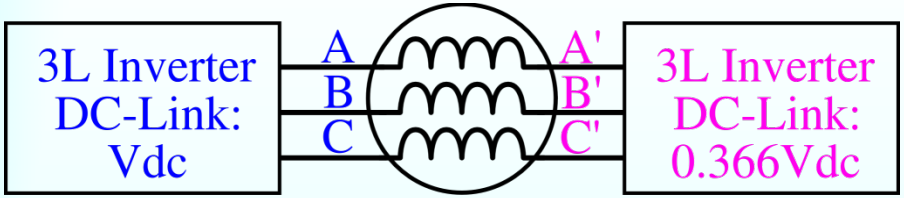


Fig: Topology for multilevel Dod-VSVS

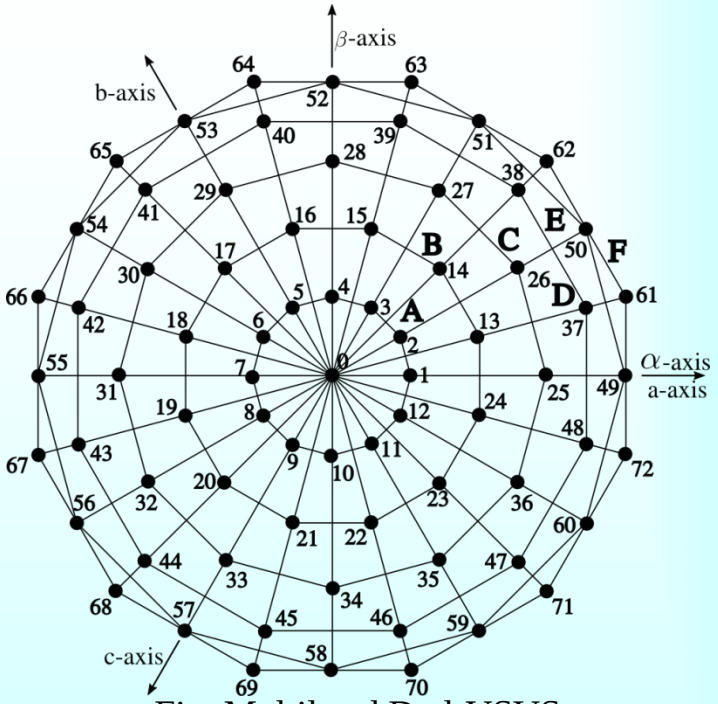


Fig: Multilevel Dod-VSVS

- Requires 2 DC sources delivering active power
- DC links: V_{dc} & $0.366V_{dc}$
- 6 concentric dodecagons giving a multilevel structure

- [2] A. Das and K. Gopakumar, "A voltage space vector diagram formed by six concentric dodecagons for induction motor drives," IEEE Trans. Power Electron., vol. 25, pp. 1480–1487, June 2010.

Dodecagonal VSVS – Prior Works

- 2-level dodecagonal space vector structure for open-end winding IM using single DC source

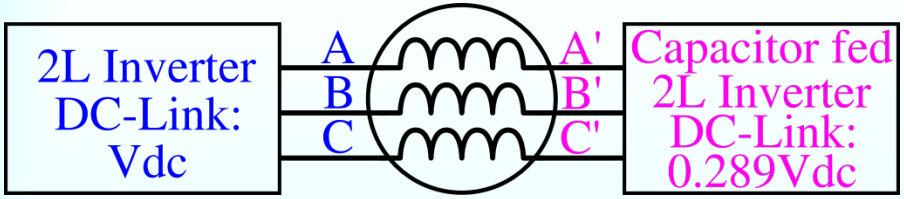


Fig: Topology for 2-level Dod-VSVS using single DC source

- Requires only one DC source delivering active power
- DC links: V_{dc} & $0.289V_{dc}$ (capacitor fed)
- Only 2-level operation

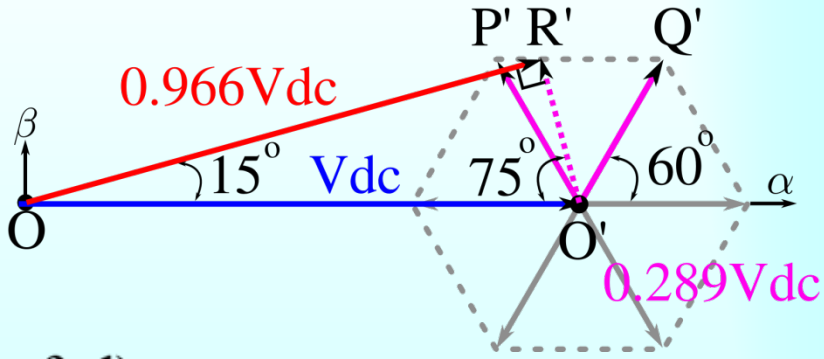


Fig: Dodecagonal vector generation

- [3] S. Pramanick, N. Azeez, R. Sudharshan Kaarthik, K. Gopakumar, and C. Cecati, "Low-order harmonic suppression for open-end winding im with dodecagonal space vector using a single dc-link supply," IEEE Trans. Ind. Electron., vol. 62, pp. 5340–5347, Sept 2015.

Octadecagonal VSVS – Prior Works

- 2-Level octadecagonal SVS first proposed in:
  - [4] S. Lakshminarayanan, G. Mondal, P. Tekwani, K. Mohapatra, and K. Gopakumar, "**Twelve-sided polygonal voltage space vector based multilevel inverter for an induction motor drive with common-mode voltage elimination**," IEEE Trans. Ind. Electron., vol. 54, DOI 10.1109/TIE.2007.899929, no. 5, pp. 2761–2768, Oct. 2007.
  - Requires **3 DC sources** delivering active power
  - Only 2-level operation

- A 3-concentric multilevel octadecagonal SVS proposed in:
  - [5] K. Mathew, K. Gopakumar, J. Mathew, N. A. Azeez, A. Dey, and L. Umanand, "**Medium voltage drive for induction motors using multilevel octadecagonal voltage space vectors**," IEEE Transactions on Power Electronics, vol. 28, pp. 3573–3580, July 2013
  - Requires **4 DC source**

Motivation For Research

- Is it possible to generate multilevel dodecagonal & octadecagonal voltage space vector structures using a single DC source?
  - Single DC source:
    - Permits easy 4-quadrant operation
    - Reduces cost and size of the system
  - Multilevel operation brings:
    - Lower switching frequency operation
    - Improved voltage and current THD
    - Lower EMI concerns
    - Reduced filtering requirements
  - Dodecagonal & Octadecagonal structure brings:
    - Absence of low order harmonics in phase voltage
    - Improved linear modulation range

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- A drive scheme for an open-end winding IM to generate a multilevel Dod-VSVS using a single DC source is proposed.
  - Obtaining a 2-level Dod-VSVS[1]
  - Obtaining a 2-level Dod-VSVS using a single DC source[2]
  - Obtaining a multilevel Dod-VSVS[3] using a single DC source
  - Power circuit topology
  - Dod-VSVS features
  - PWM scheme
  - Capacitor balancing
  - Implementation
  - Results

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Obtaining a 2L Dod-VSVS[1]:
  - (a) Method 1
    - INV2 DC-link is $0.366V_{dc}$
    - Resultant vector is of $1.225V_{dc}$
    - INV2 sources power
  - (b) Method 2
    - INV2 DC-link is $0.268V_{dc}$
    - Resultant vector is of $0.896V_{dc}$
    - INV2 sinks power
- If we make fundamental voltage output of resultant Dod-VSVS same as that of INV1, average power delivered by INV2 equals zero.

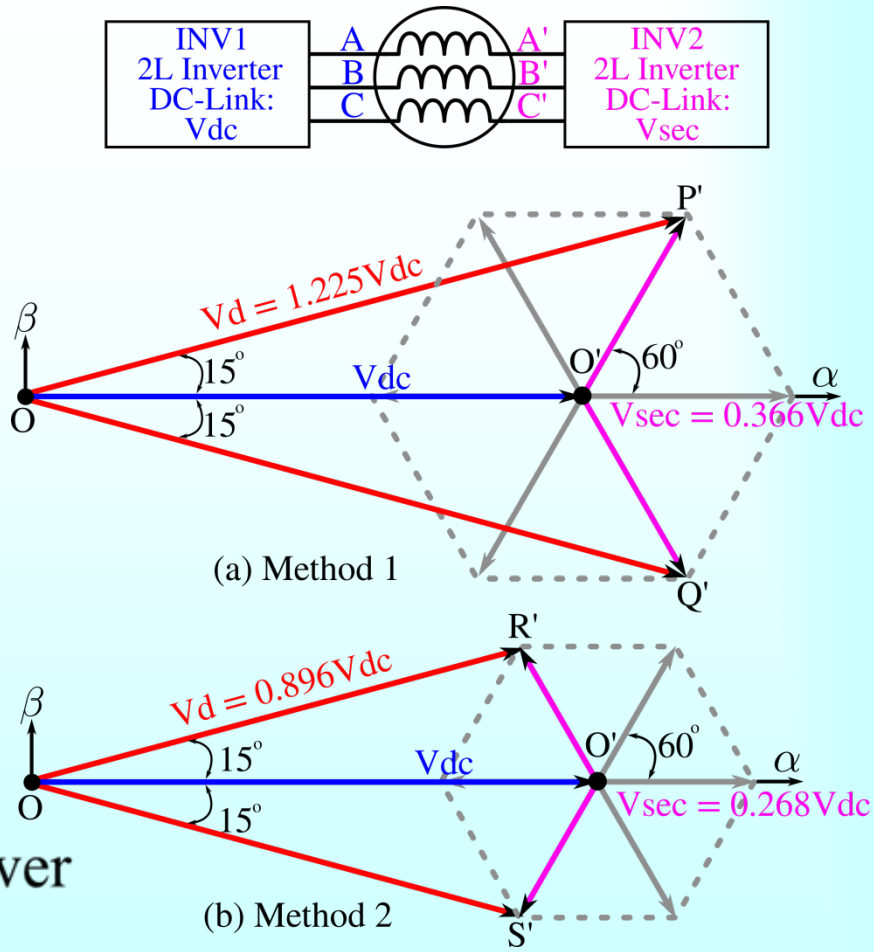


Fig: Methods for generation of 2L dodecagonal VSVS

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Obtaining a 2-level Dod-VSVS using a single DC source[3]:
  - Fundamental output from resultant dodecagon = output from hexagon (INV1)
  - $0.659V_d = 0.637V_{dc}; \boldsymbol{V_d = 0.966V_{dc}}$
  - Zero power delivered by INV2, replace DC source in INV2 by a capacitor
  - $V_{pseudo} = O'R' = 0.259V_{dc}\angle 75^o$
  - O'P' (inner vector) and O'Q' (outer vector) are averaged to get dodecagonal vector O'R'

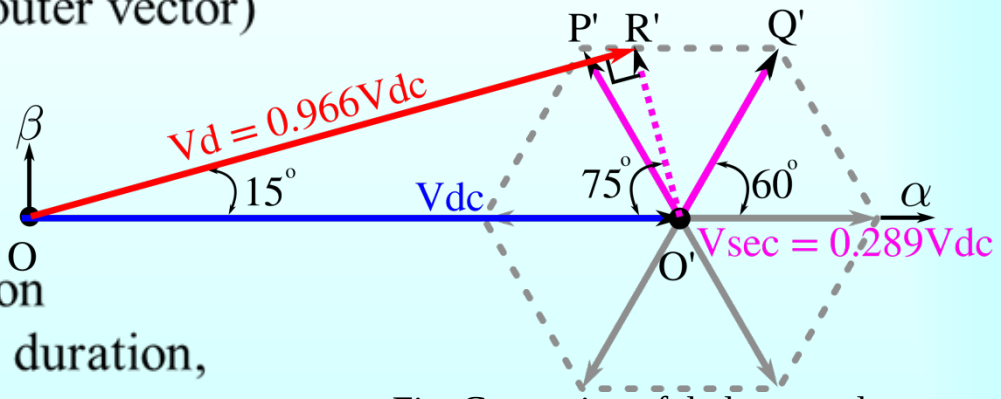


Fig: Generation of dodecagonal vector using single DC source

  - O'P' is applied for $k * T$ duration
    O'Q' is applied for $(1-k) * T$ duration,
    - T is the duration for which OR' is applied
  - Nominal $k = 0.732$, adjust k to balance INV2 capacitor voltage
    - $k > 0.732$ charges & $k < 0.732$ discharges INV2 DC-link capacitor

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Obtaining a multilevel Dod-VSVS using a single DC source:
  - A 6-concentric Dod-VSVS is obtained from superposition of two 2L Dod-VSVS
  - DOD1:[0 ,1 ,2 , …,11 ,12]
  - DOD2:[0',1',2',…,11',12']
  - Superposition example:
    - B1 = DOD1[1]+DOD2[0']
    - D2 = DOD1[1]+DOD2[3']
    - F1 = DOD1[1]+DOD2[1']
    - and so on…

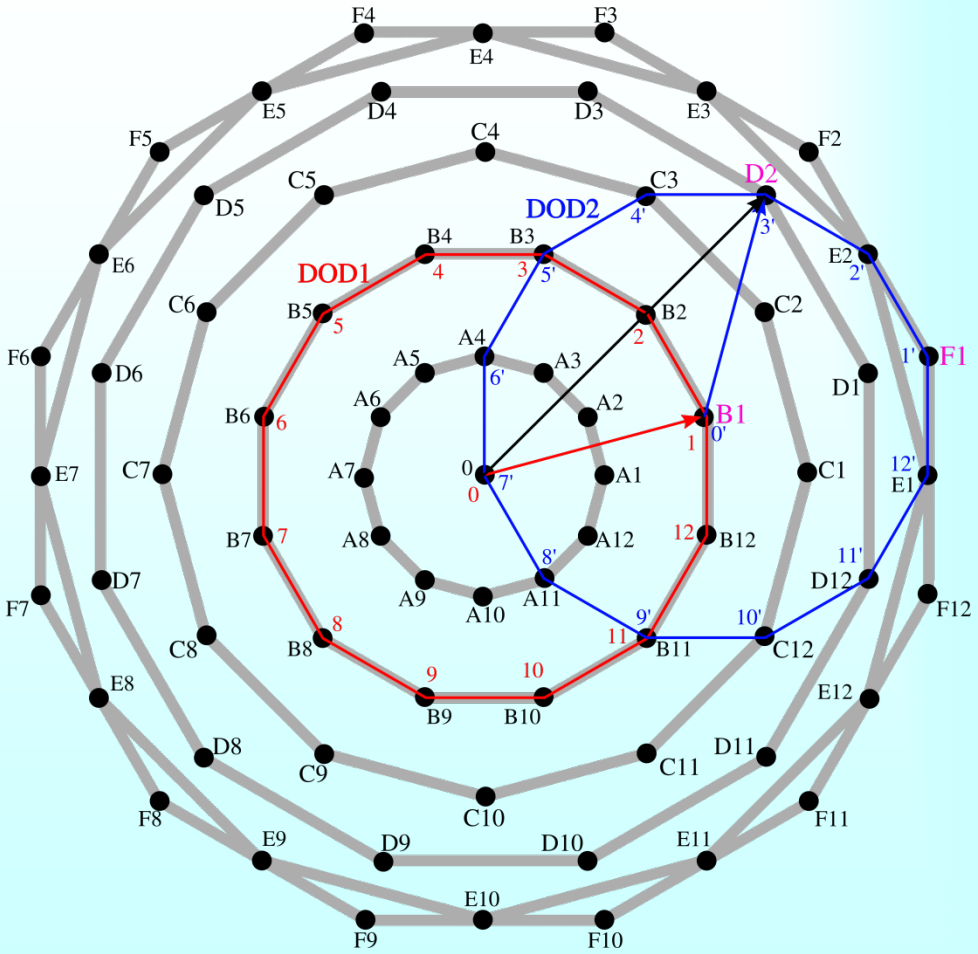


Fig: 6-concentric Dod-VSVS as superposition of 2 dodecagons

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- 6-con Dod-VSVS as superposition of hexagons:
  - DOD1 is generated using HEX1_PRI & switched averaged vectors from HEX1_SEC
  - DOD2 is generated using HEX2_PRI & switched averaged vectors from HEX2_SEC
  - 6-conc Dod-VSVS is obtained as superposition of DOD1 & DOD2
  - A 3L Hex-VSVS is a superposition of two 2L Hex-VSVS
  - Hence, 6-conc Dod-VSVS is obtained from HEX_3L_PRI and switched averaged vectors from HEX_3L_SEC

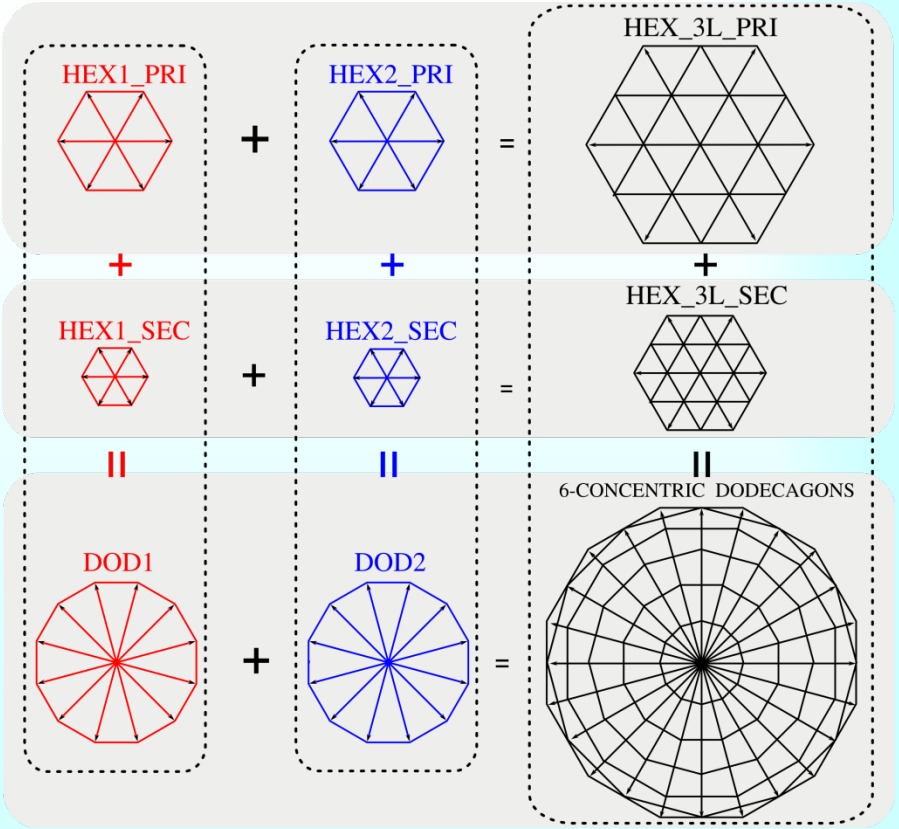


Fig: 6-concentric Dod-VSVS as superposition hexagons

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Power Circuit Topology:
- DC-links:
  - $V_{prim} = V_{dc}$
  - $V_{sec} = 0.289V_{dc}$
- Device counts:
  - 12 half bridges
  - 7 capacitors
- Device voltage ratings:
  - INV1: $V_{dc}/2$
  - INV2: $0.1445V_{dc}$
- Capacitor ratings:
  - INV1: $V_{dc}/2$
  - INV2:
    - FCs: $0.1445V_{dc}$
    - DC-link: $0.289V_{dc}$

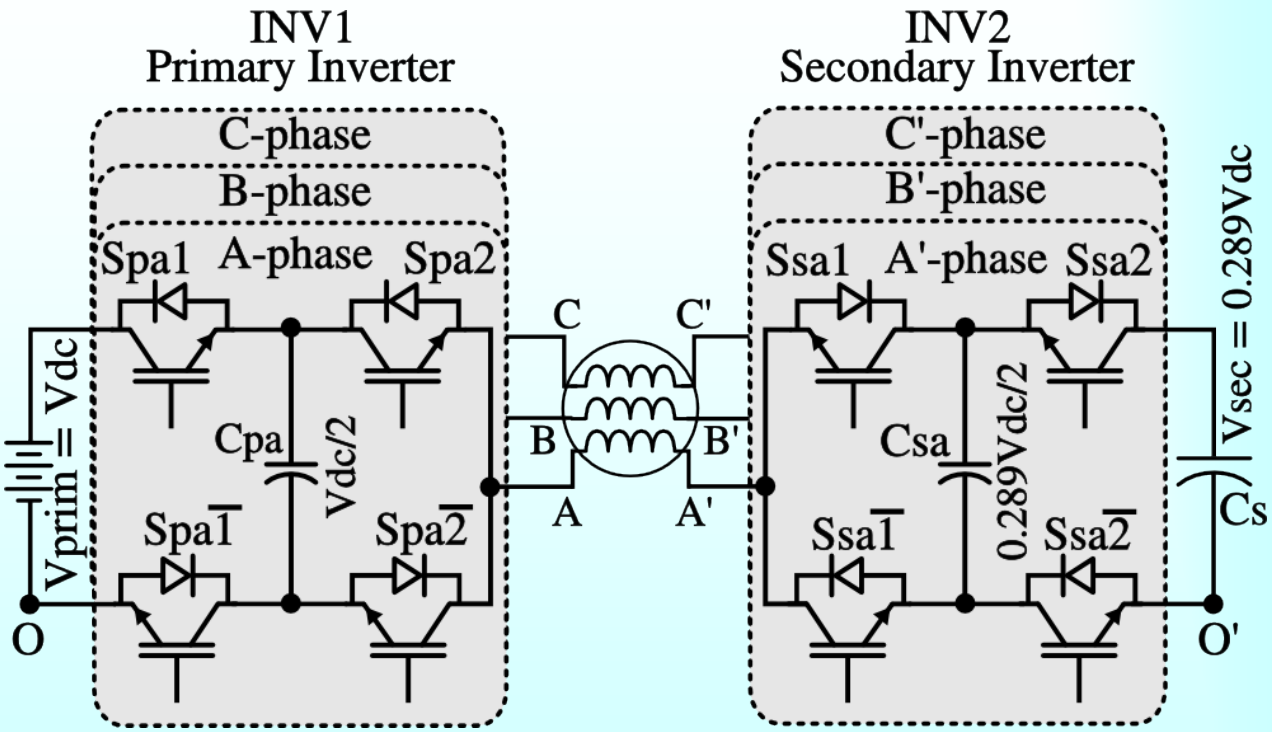


Fig: Power circuit topology for 6-con Dod-VSVS for open-end winding IMD

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Topology:
  - Open-end winding IM permits superposition of two VSVS
  - HEX_3L_PRI from INV1 & HEX_3L_SEC from INV2
  - Flying capacitor topology is used
  - INV1:
    - $OX = V_{dc}/2; OY = V_{dc}$
    - States: `2′ → $V_{dc}$;`1′ → $V_{dc}/2$; `0′ → 0
  - INV2:
    - $OX = 0.1445V_{dc}; OY = 0.289V_{dc}$
    - States: `2′ → $0.289V_{dc}$; `1′ → $0.1445V_{dc}$; `0′ → 0

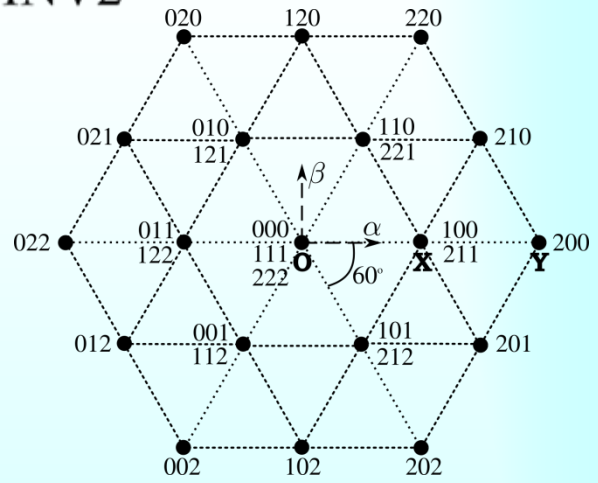


Fig: VSVS of 3L inverters

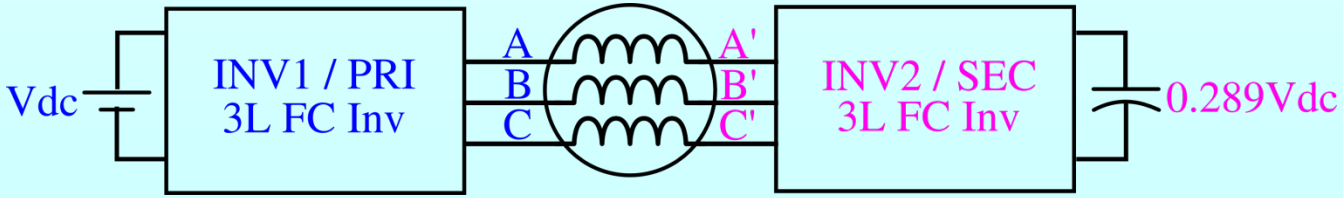


Fig: Topology for 6-con Dod-VSVS for open-end winding IM drive

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Raw VSVS:
  - Obtained by superposition of primary and secondary three-level hexagonal structures
  - Dodecagonal vectors are generated using vectors from primary inverter and pseudo vectors from secondary inverter
  - Pseudo vectors are generated by switched averaging of two vectors from secondary inverter

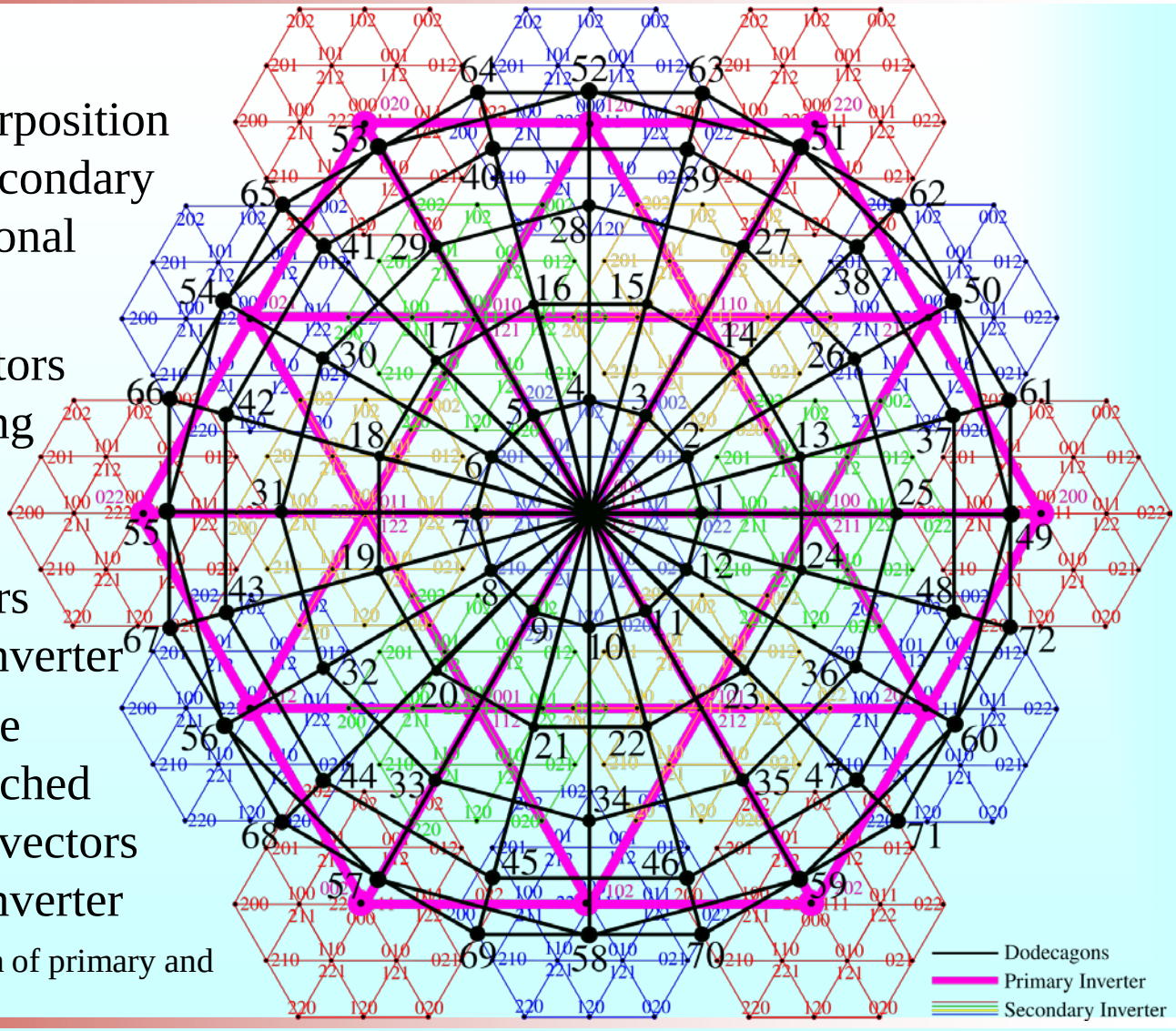


Fig: VSVS obtained by superposition of primary and secondary hexagons

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Example of dodecagonal vector generation using pseudo vectors (dotted lines):
  - Space vector structures are subtracted because of open-end winding connection
  - Vector 13 generated by averaging 101 and 112 with $k = 0.732$
  - Vector 61 generated by averaging 202 and 102 with $k' = 2k - 1 = 0.464$
    - $k' = 0.464$ used for vectors 49, 51, 53, 55, 57 & 59 in E and all vectors (61 to 72) in F
    - Prevents exceeding machine phase voltage rating & reduces INV2 dv/dt

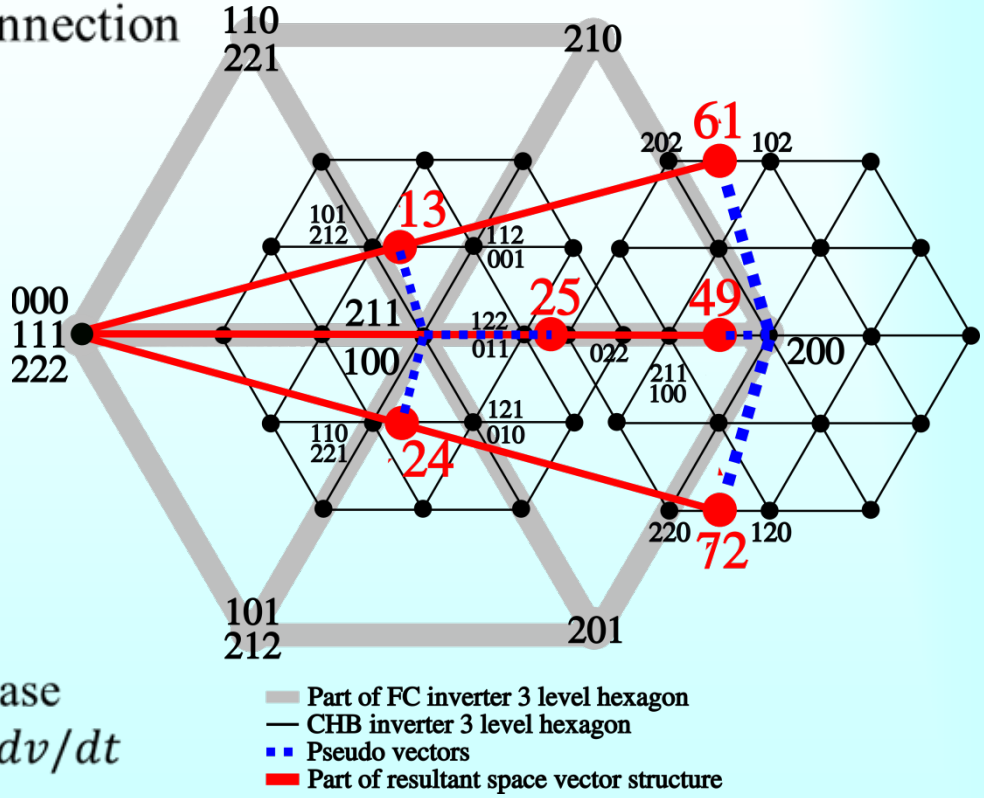


Fig: Dodecagonal vector generation

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Space vector structure:
  - 6 concentric dodecagons: A-F
  - 73 vectors including zero vector
  - Two types of dodecagons:
    - Type1: B, D, F
    - Type2: A, C, E
  - $R_A : R_B : R_C : R_D : R_E : R_F = \cos(75^o) : \cos(60^o) : \cos(45^o) : \cos(30^o) : \cos(15^o) : \cos(0^o)$
  - $R_F = 0.966 V_{dc}$
  - Density increases at higher modulation range
  - Dodecagons are formed in a switched average sense

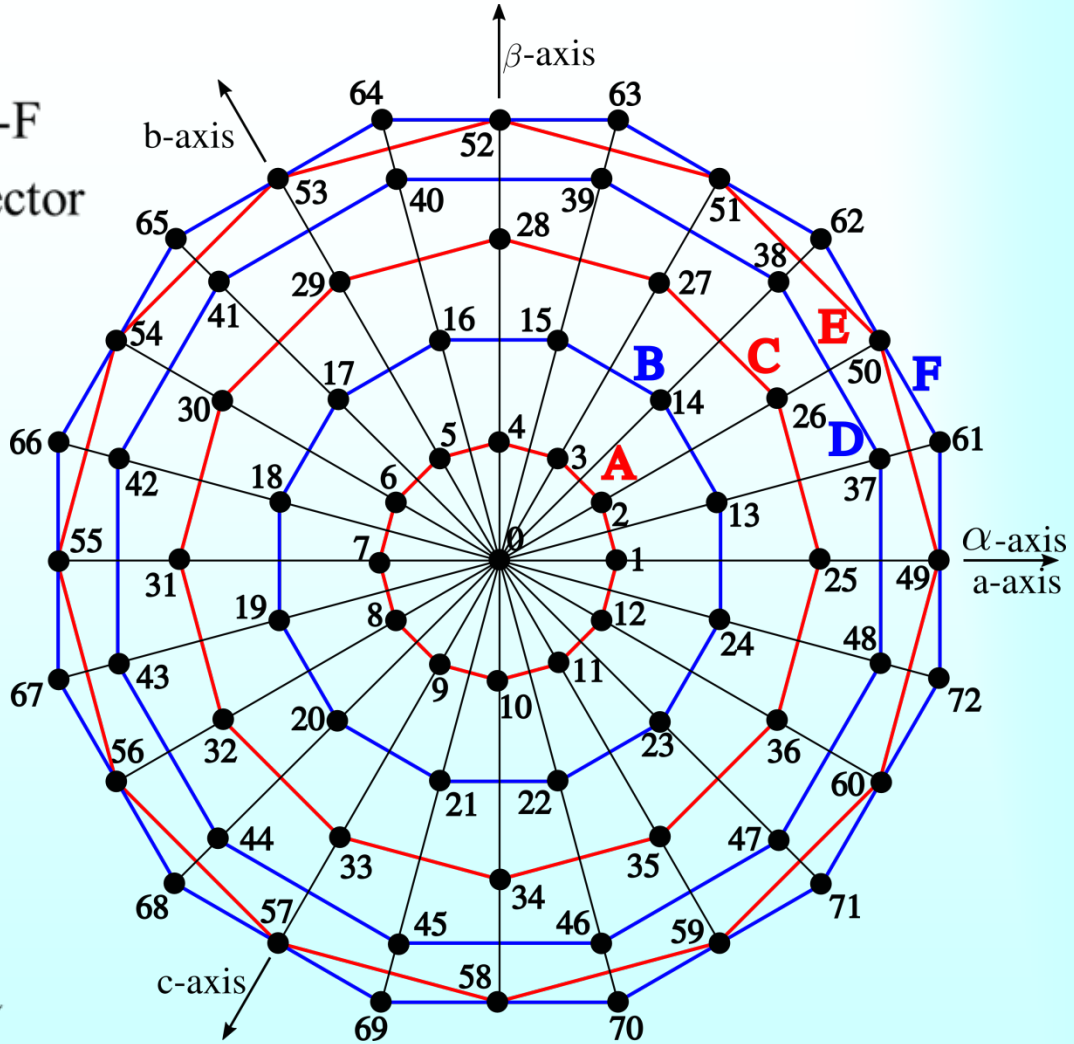


Fig: Resultant 6-con Dod-VSVS

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- PWM Scheme:
  - Sampled reference based SVPWM timing calculation is implemented

$$V_{ref}T_s = V_0T_0 + V_1T_1 + V_2T_2$$

$$T_s = T_0 + T_1 + T_2$$

    - $[V_0, V_1, V_2]$ are the adjacent vectors to V_{ref} forming a triangular boundary
    - T_s is the sampling duration
    - $[T_0, T_1, T_2]$ are durations for which $[V_0, V_1, V_2]$ are applied
  - Aim is to find $[V_0, V_1, V_2]$ & $[T_0, T_1, T_2]$
  - Involves:
    - Sector identification
    - Dodecagon identification
    - Triangle identification
    - Vector selection from a LUT

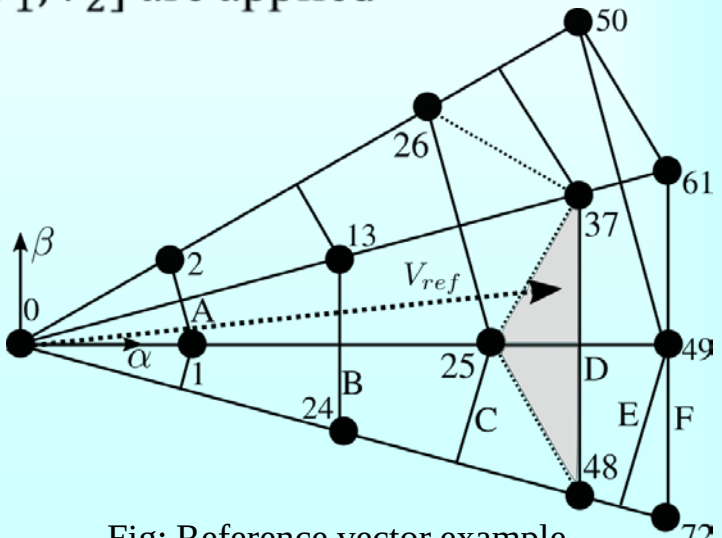


Fig: Reference vector example

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- PWM Scheme1:
  - Conventional SVPWM sequence
  - $V_0 \rightarrow V_1 \rightarrow V_2 \rightarrow V_0 \rightarrow V_2 \rightarrow V_1 \rightarrow V_0$
  - $\frac{T_0}{4} \rightarrow \frac{T_1}{2} \rightarrow \frac{T_2}{2} \rightarrow \frac{T_0}{2} \rightarrow \frac{T_2}{2} \rightarrow \frac{T_1}{2} \rightarrow \frac{T_0}{4}$
  - $k = 0.732\ (0.464)$ at SS
  - When a vector V_x is applied from INV1, V_x^i & V_x^o is applied from INV2
  - Scheme1 is used for lower modulation ranges

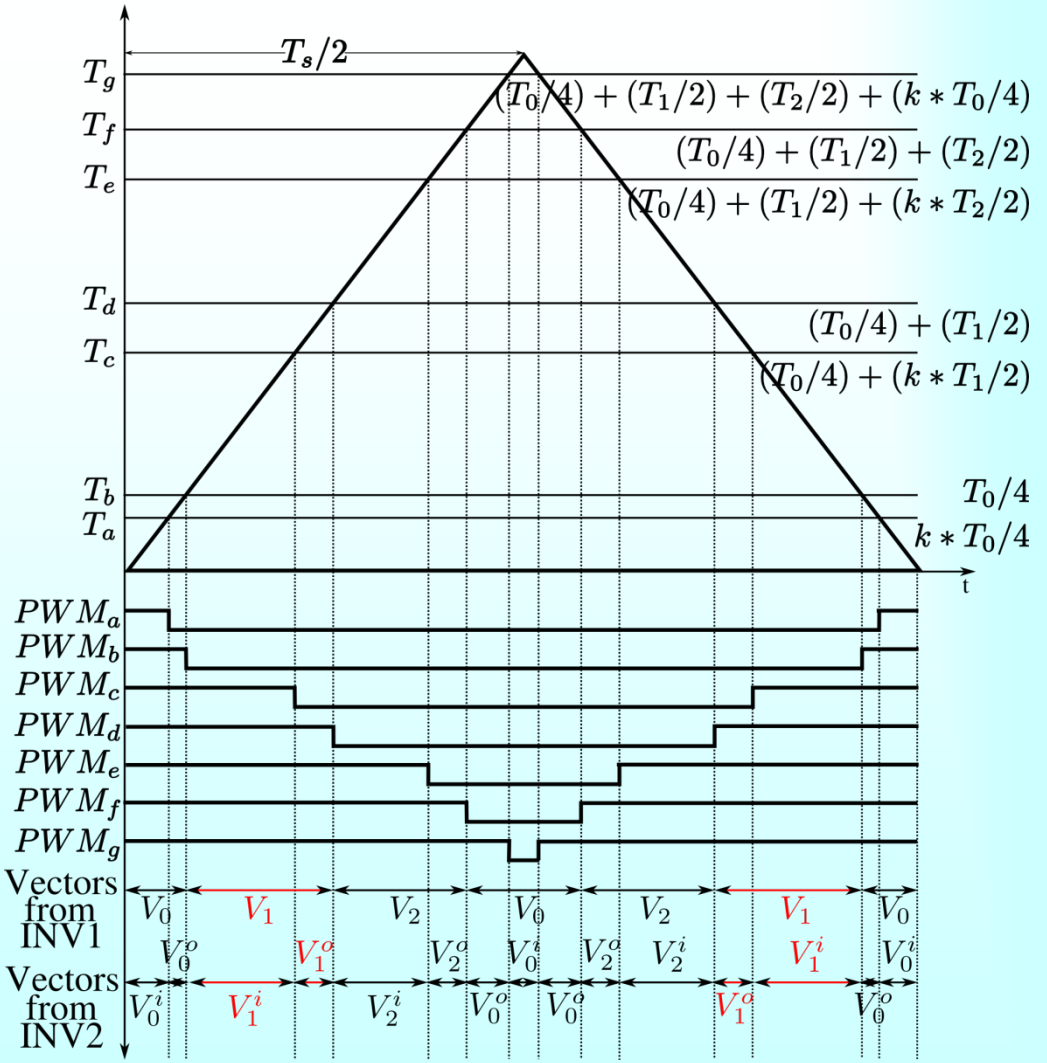


Fig: PWM Scheme1

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- PWM Scheme2:
  - Take advantage of the denser SVS at higher modulation indices
  - $V_1 \rightarrow V_0 \rightarrow V_2$ for $T_1 \rightarrow T_0 \rightarrow T_2$
  - Reduced switching
  - Quasi-square output from INV1

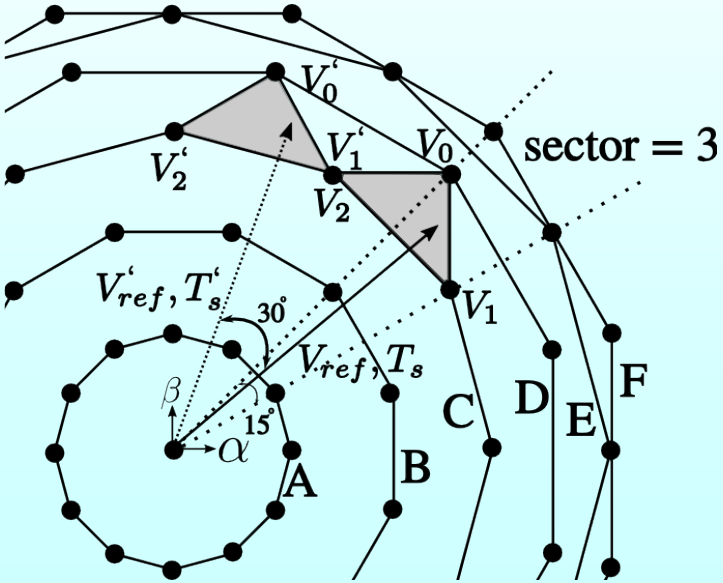


Fig28: Vector switching in PWM Scheme2

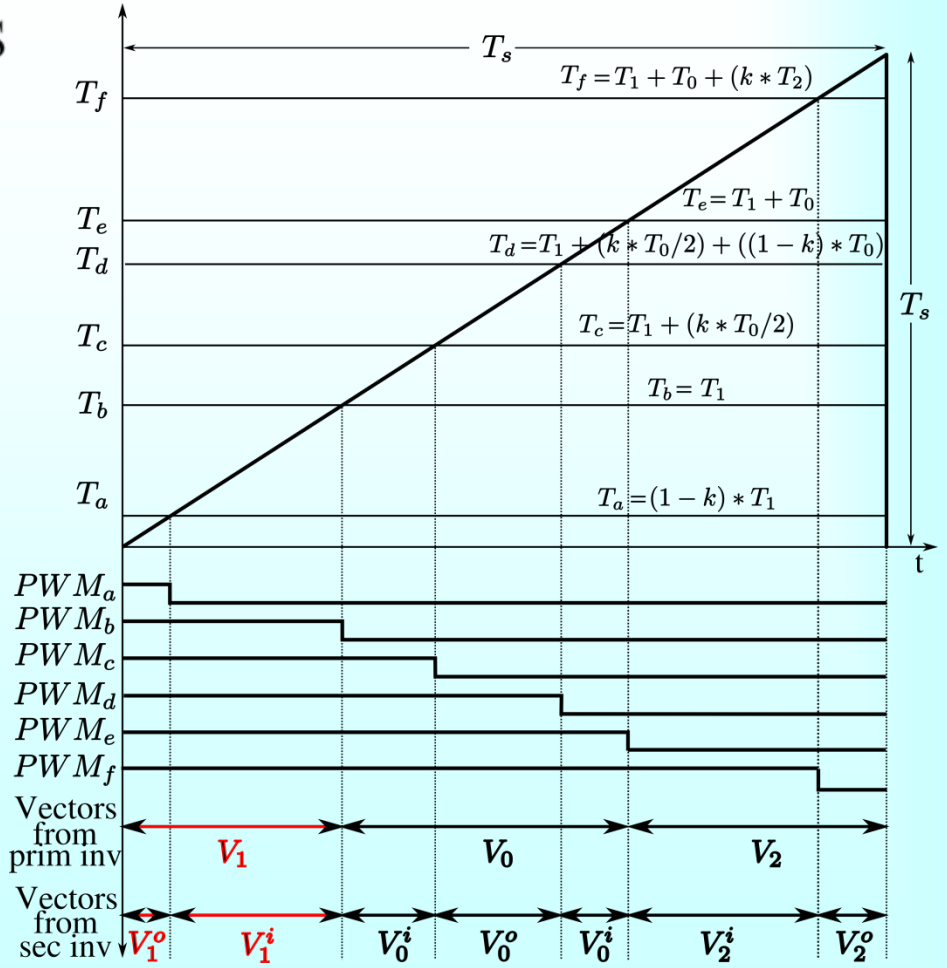


Fig: PWM Scheme2

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Capacitor Balancing:
  - Flying capacitor balancing:
    - Utilizing pole voltage redundancy available in generating $\frac{V_{dc}}{2}$ pole voltage (switching state 1).

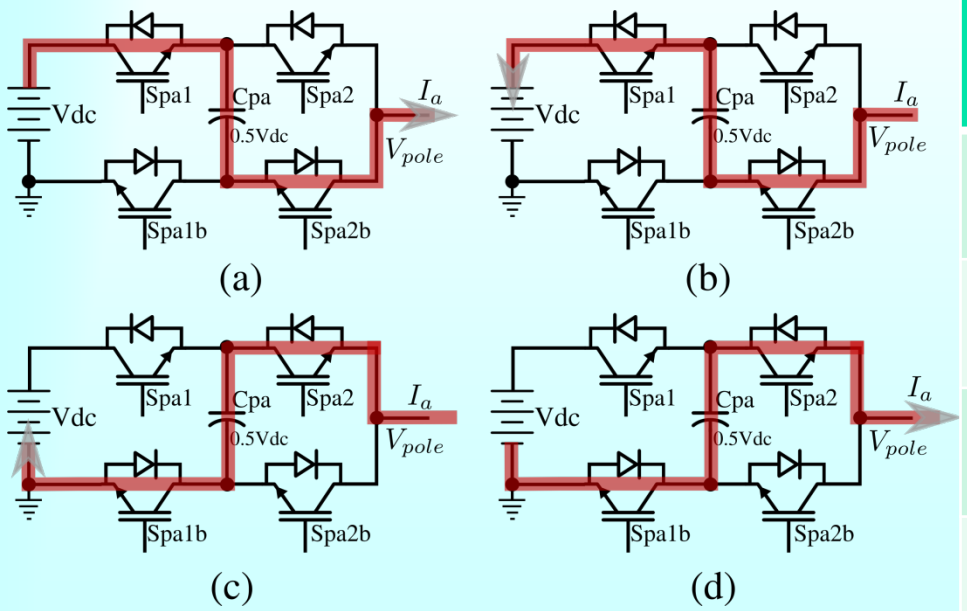


Fig: FC voltage balancing

Fig	Current Dir.	Sensed Capacitor Voltage	Switches Turned ON	Pole Voltage
(a)	+	$V_{C_{pa}} < \frac{V_{dc}}{2}$	S_{pa1} & S_{pa2b}	$V_{dc} - V_{C_{pa}}$
(b)	-	$V_{C_{pa}} < \frac{V_{dc}}{2}$	S_{pa1} & S_{pa2b}	$V_{dc} - V_{C_{pa}}$
(c)	-	$V_{C_{pa}} < \frac{V_{dc}}{2}$	S_{pa2} & S_{pa1b}	$V_{C_{pa}}$
(d)	+	$V_{C_{pa}} > \frac{V_{dc}}{2}$	S_{pa2} & S_{pa1b}	$V_{C_{pa}}$

Table: FC voltage balancing

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Capacitor Balancing:
  - Secondary DC-link capacitor balancing:
    - Is naturally balanced
    - Forced balancing used for startup and to meet non-idealities
    - A simple control loop adjusting value of k
      - $k > 0.732$ ($k' > 0.464$) increases capacitor voltage (INV2 sinks power)
      - $k < 0.732$ ($k' < 0.464$) decreases capacitor voltage (INV2 sources power)
    - Vector check logic selects k or k' depending on vector to be applied

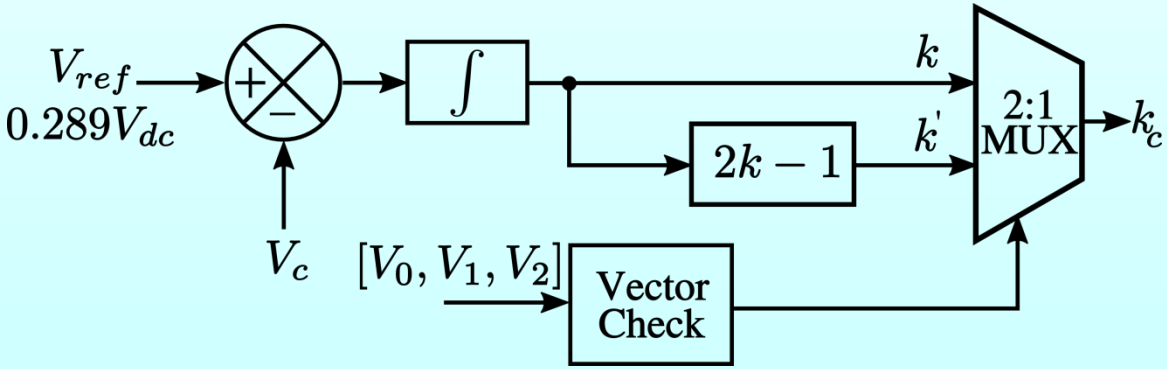


Fig: Secondary DC-link capacitor balancing

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Capacitor Design: Primary side flying capacitors
  - Nominal operating voltage = $V_{dc}/2$
  - Capacitors are bypassed during states `0′ & `2′, balancing has to be done whenever state `1′ is applied
  - Design:
    - Peak current through capacitor (phase current) = I_p (A)
    - Sampling time duration (duration for which state `1′ is applied) = T_s (s)
    - Nominal capacitor voltage = V_c (V)
    - Allowable capacitor voltage ripple = r (%)
    - Capacitor value, $C = \frac{100 * I_p * T_s}{r * V_c}$
  - Example: For $50Hz$ operation at $12spc$, $V_c = 100V$, $I_p = 10A$ and target $r = 5\%$: $C = \frac{100*10*\left(\frac{1}{50*12}\right)}{5*100} = 3333uF$

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Capacitor Design: Secondary side flying capacitors
  - Nominal operating voltage = $0.1445V_{dc}$
  - Capacitors are bypassed during states `0′ & `2′, balancing has to be done whenever state `1′ is applied
  - Design:
    - Peak current through capacitor (phase current) = I_p (A)
    - Sampling time duration (duration for which state `1′ is applied) = T_s (s)
    - Nominal capacitor voltage = V_c (V)
    - Allowable capacitor voltage ripple = r (%)
    - Capacitor value, $C = \frac{100 * I_p * T_s}{r * V_c}$
  - Example: For $50Hz$ operation at $12spc$, $V_c = 28.9V$, $I_p = 10A$ and target $r = 5\%$: $C = \frac{100*10*\left(\frac{1}{600}\right)}{5*28.9} = 11534uF$

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Capacitor Design: Secondary side DC-link capacitor
  - Nominal operating voltage = $0.289V_{dc}$
  - $I_{C_s} = sgn(S_A - 1) + sgn(S_B - 1) + sgn(S_C - 1)$
  - Example: 210
    - $I_{C_s} = I_A + I_B + I_C$
    - $I_{C_s} = -2I_C$
  - Worst case capacitor current is $2I_p$
  - Capacitor value, $C = \frac{100*2*I_p*T_s}{r*V_c}$
  - Example: For $50Hz$ operation at $12spc$, $V_c = 57.8V$, $I_p = 10A$ and target $r = 5\%$:

$$C = \frac{100 * 2 * 10 * \left(\frac{1}{600}\right)}{5 * 57.8} = 1154uF$$

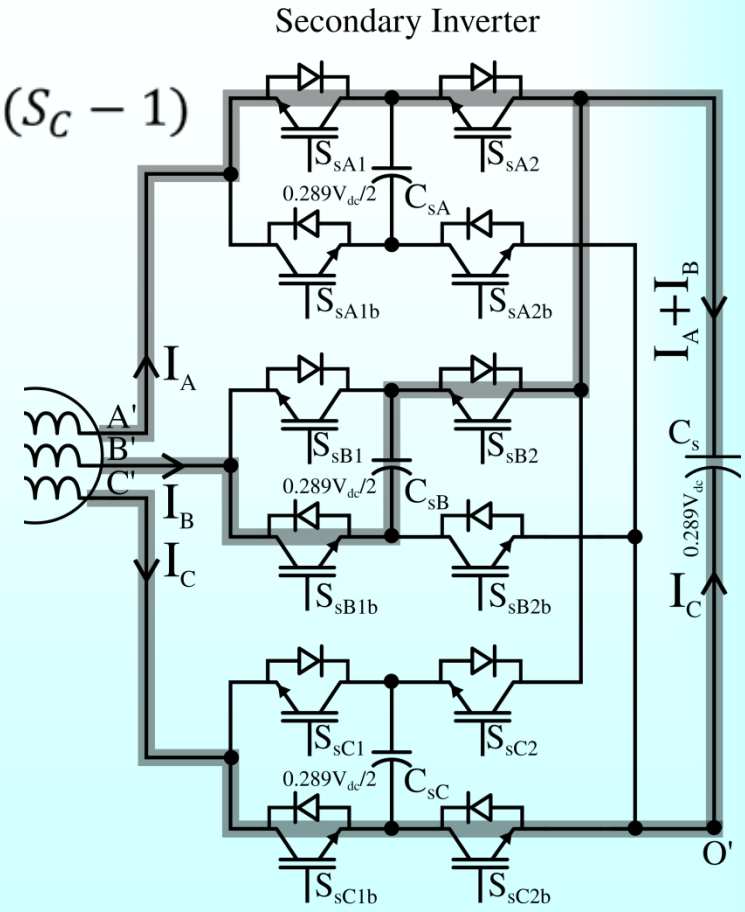


Fig: Secondary inverter capacitor current for state 210

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Implementation:
  - $V_{dc} = 200V$
  - $V_{sec} = 57.8V$
  - SKM75GB12T4 (75A, 1200V) IGBT half-bridge based inverters
  - 3phase currents, capacitor voltages, V_{dc} & V_{sec} are sensed
  - Capacitors:
    - INV1 FC: 2200uF
    - INV2 FC: 2200uF
    - INV2 DC-link: 2200uF

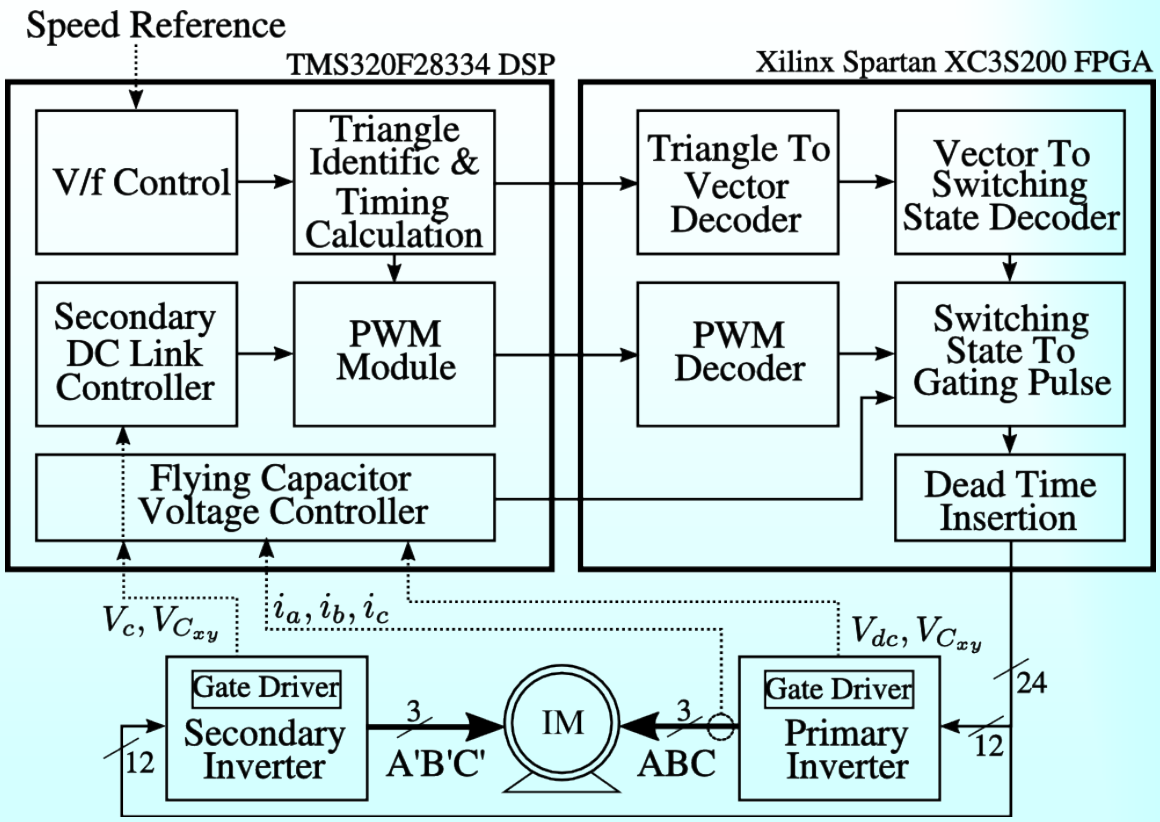


Fig: Hardware implementation block diagram

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Implementation:

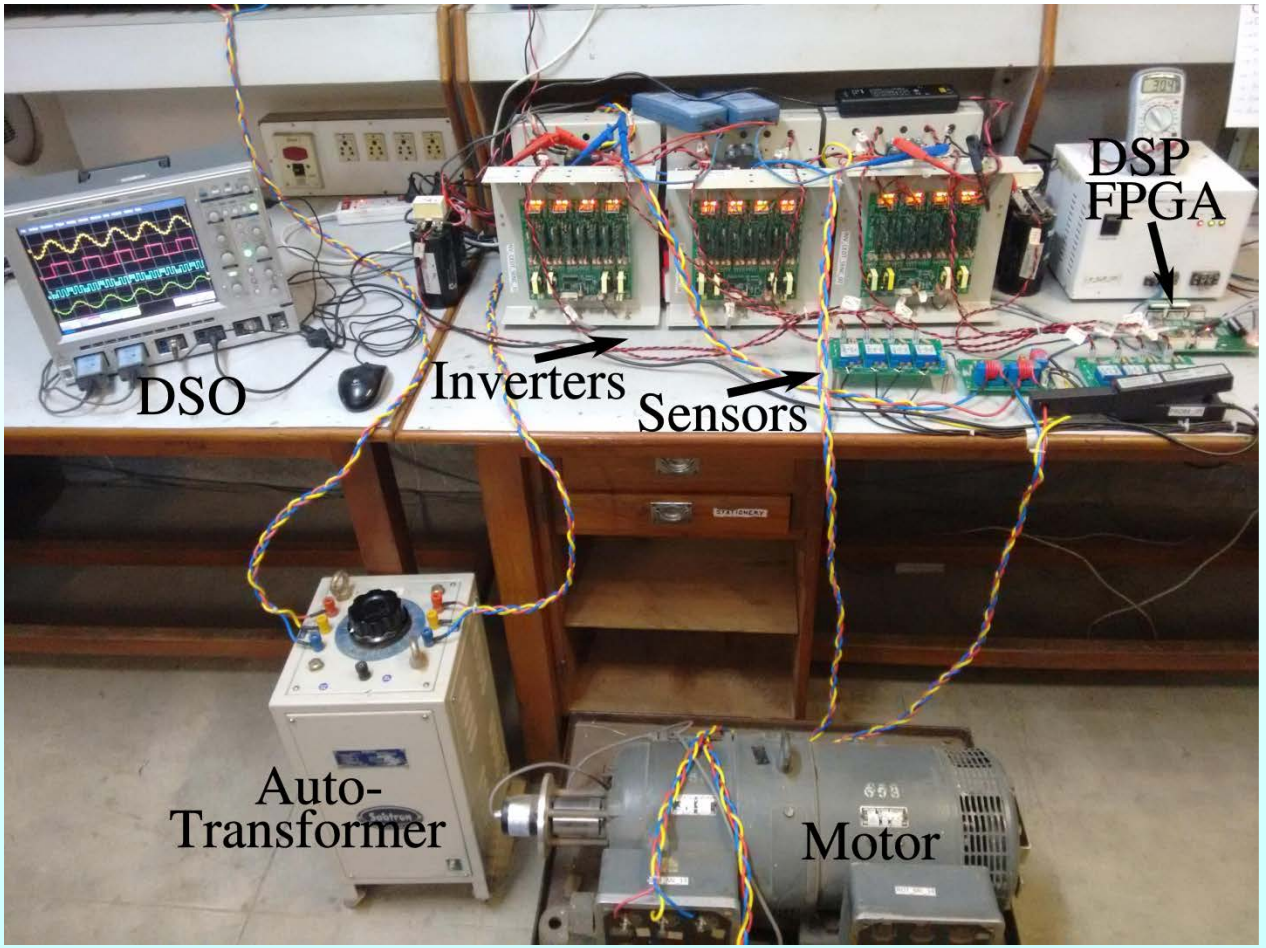


Fig: Hardware implementation

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Steady state results:

10Hz (M=0.2) Operation – 48spc – PWM1

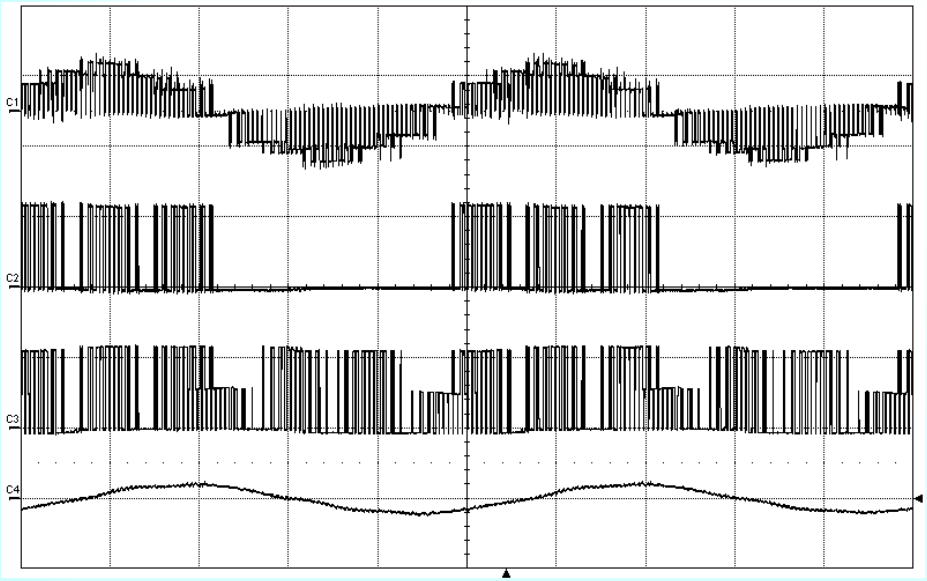


Fig: Vdc=200V (1) Phase voltage, 50V/div, (2) Primary inverter pole voltage, 100V/div, (3) Secondary inverter pole voltage, 50V/div, (4) Current, 2A/div; X-axis: 20mS/div

30Hz (M=0.6) Operation – 24spc – PWM1

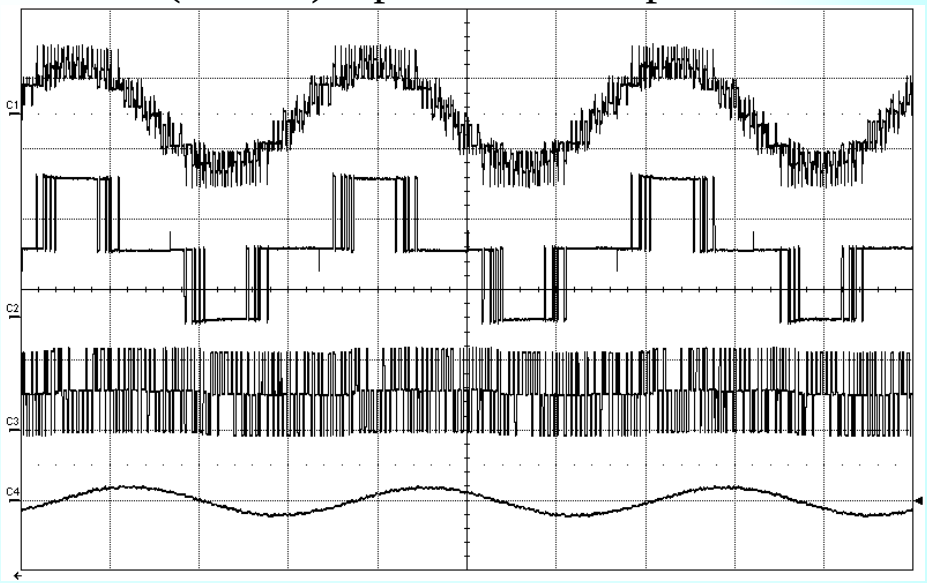


Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) Primary inverter pole voltage, 100V/div, (3) Secondary inverter pole voltage, 50V/div, (4) Current, 2A/div; X-axis: 10mS/div

- Higher frequency switching happens in secondary inverter at low voltage

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Steady state results:

40Hz (M=0.8)Operation – 12spc – PWM2

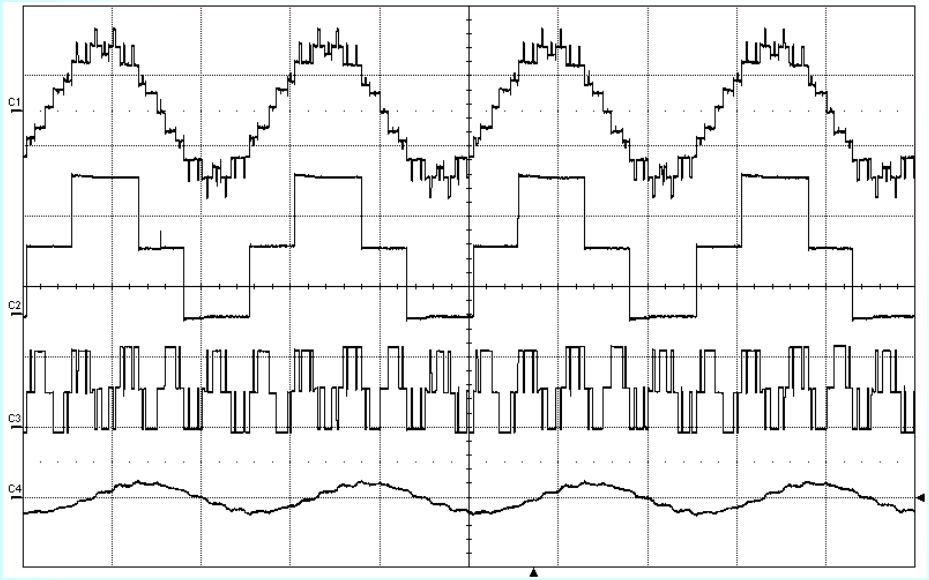


Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) Primary inverter pole voltage, 100V/div, (3) Secondary inverter pole voltage, 50V/div, (4) Current, 2A/div; X-axis: 10mS/div

45Hz (M=0.9)Operation – 12spc – PWM2

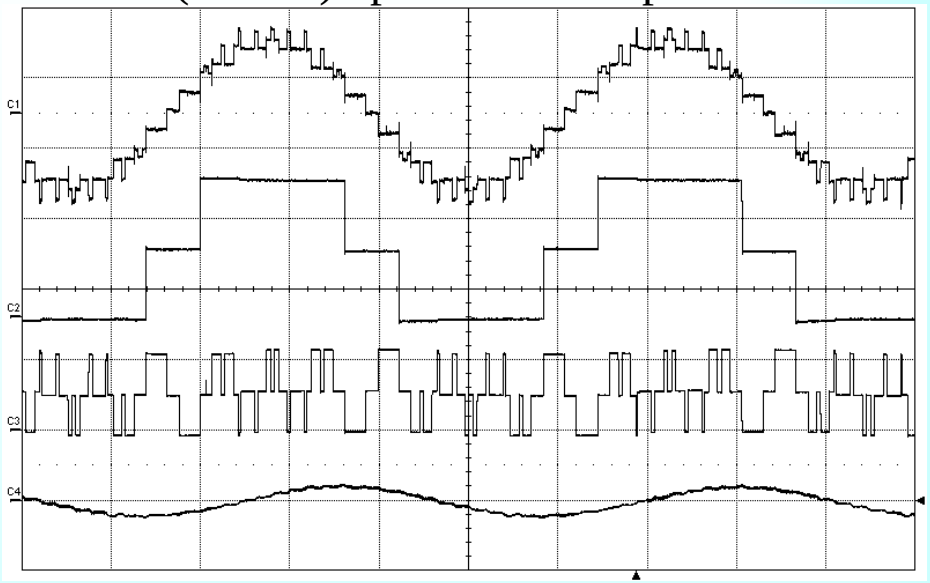


Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) Primary inverter pole voltage, 100V/div, (3) Secondary inverter pole voltage, 50V/div, (4) Current, 2A/div; X-axis: 5mS/div

- Primary inverter switches in quasi-square mode, switching losses are reduced

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Steady state results:

50Hz (M=1), 12 step mode – 12spc – PWM2

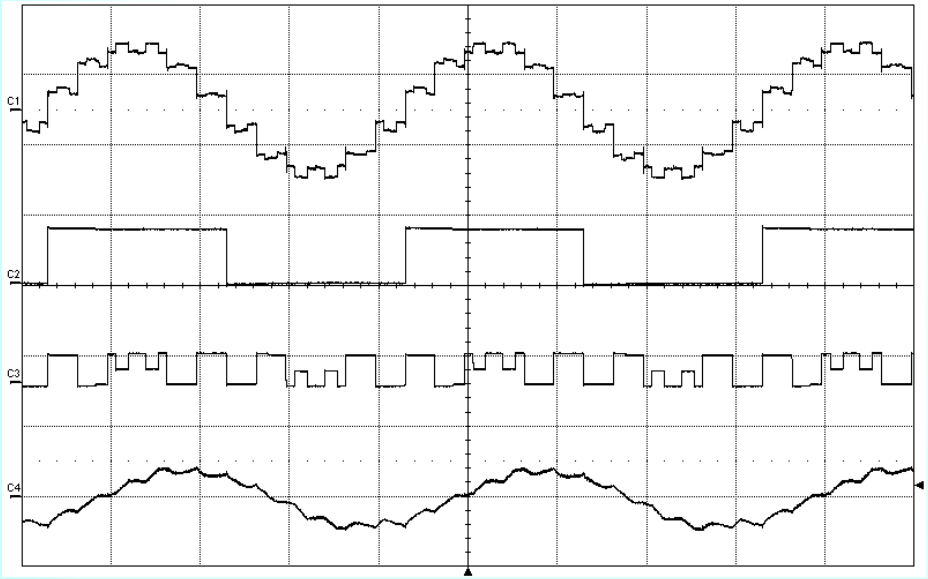


Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) Primary inverter pole voltage, 100V/div, (3) Secondary inverter pole voltage, 50V/div, (4) Current, 2A/div; X-axis: 10mS/div

FFT - 50Hz (M=1)Operation – 12spc

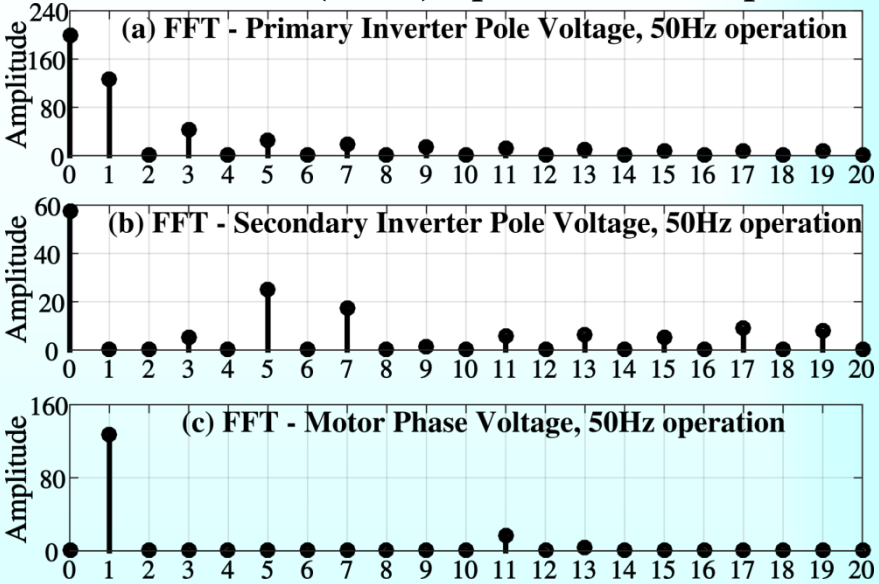


Fig: FFT of (a) primary inverter pole voltage; (b) secondary inverter pole voltage; (c) motor phase voltage; X-axis: Harmonic number; Y-axis: Voltage

- Prim inverter pole voltage is square waveform in extreme overmodulation
- No fundamental voltage contribution form secondary inverter

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Transient results:

10-48Hz (M=0.2 to 0.96) Acceleration – 12spc

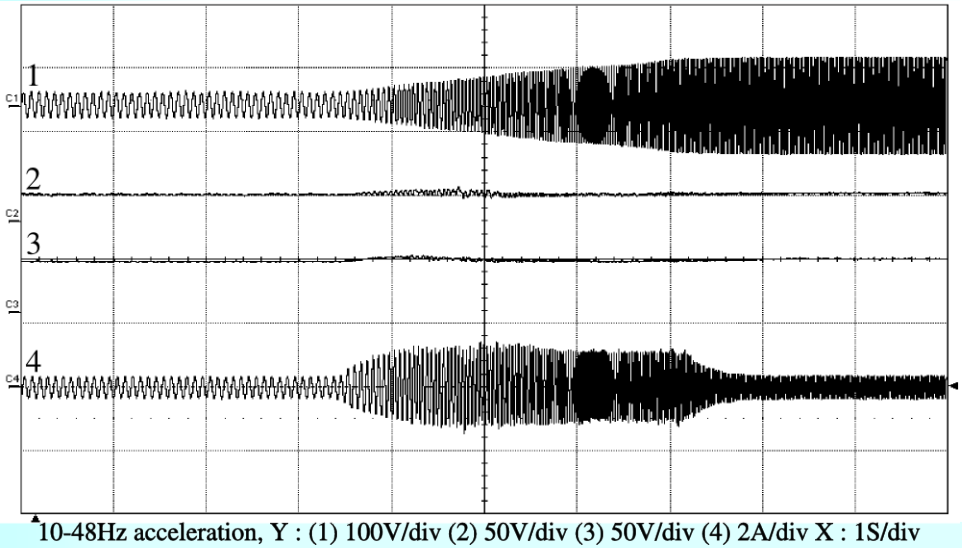


Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) Sec flying cap, 50V/div, (3) Secondary DC-link, 50V/div, (4) Current, 2A/div; X-axis: 1S/div

Startup – 48Hz (M=0.96)

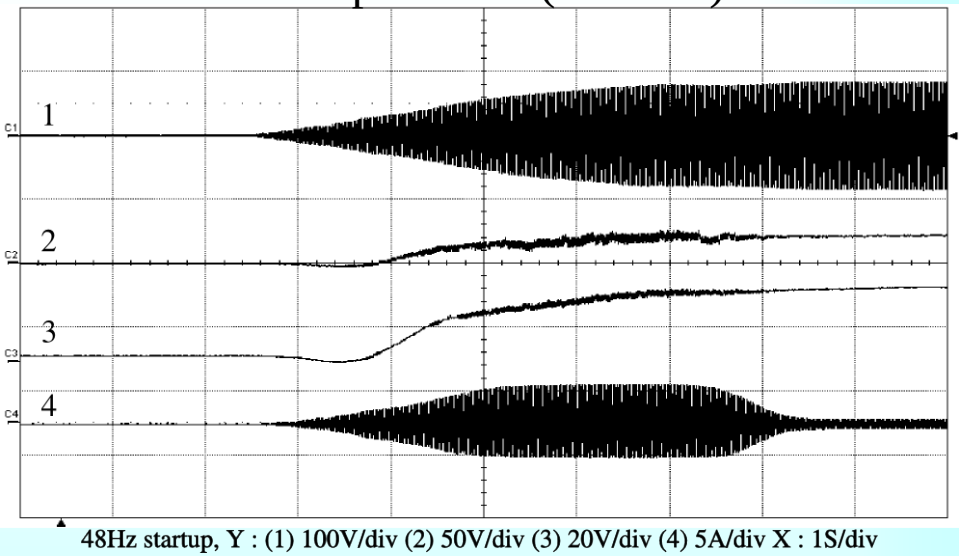


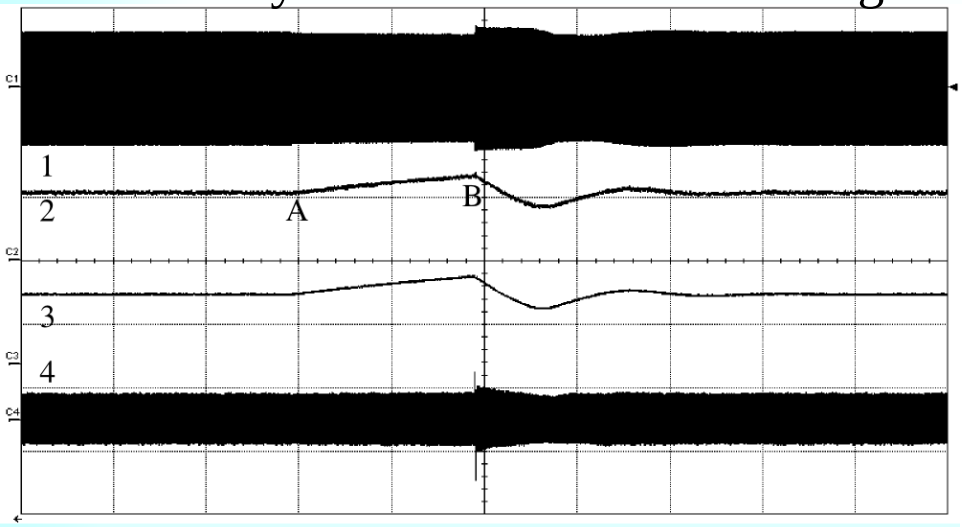
Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) Sec flying cap, 50V/div, (3) Secondary DC-link, 50V/div, (4) Current, 2A/div; X-axis: 1S/div

- Capacitor voltages reaches steady-state without the need of any pre-charging circuitry, voltage balancing happens inherently with the PWM

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Transient results:

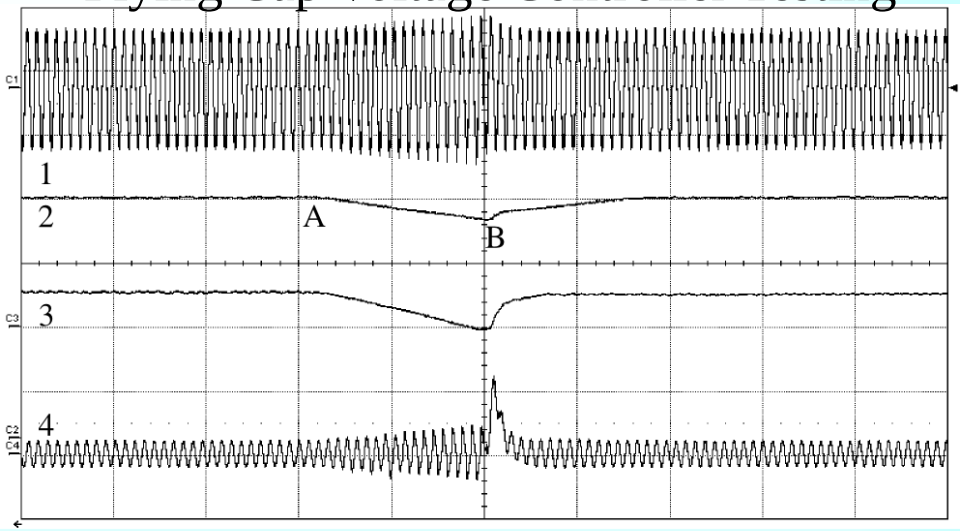
Secondary DC-link Controller Testing



Capacitor unbalance, Y : (1) 100V/div (2) 20V/div (3) 50V/div (4) 1A/div X : 2S/div

Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) Sec flying cap, 20V/div, (3) Secondary DC-link, 50V/div, (4) Current, 1A/div; X-axis: 2S/div

Flying Cap Voltage Controller Testing



Capacitor unbalance, Y : (1) 100V/div (2) 20V/div (3) 20V/div (4) 2A/div X : 200mS/div

Fig: (1) Phase voltage, 100V/div, (2) Pri flying cap, 20V/div, (3) Sec flying cap, 20V/div, (4) Current, 2A/div; X-axis: 200mS/div

- Controllers are disabled at point A and then re-enabled at point B

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Conclusion:
  - A multilevel dodecagonal space vector structure using a single DC source for an open-end winding IM is obtained
  - Four quadrant operation is easier since only one DC source is required
  - $6n \pm 1, n = odd$ order harmonics in the phase voltage are eliminated over the entire modulation range
  - Dominant 6^{th} order harmonic torque generation avoided
  - Switching losses are less both in primary and secondary inverters
  - Multilevel structure brings advantages like lesser dv/dt and better THD
  - No capacitor pre-charging circuitry is required, voltage buildup & balancing happens inherently with PWM
  - Linear modulation till $48.83Hz$ $(0.622V_{dc})$
  - Machine phase voltage rating never exceeded
  - Suitable for high performance medium voltage IM drive applications

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- A drive scheme for a star connected IM to generate a multilevel Dod-VSVS using a single DC source is proposed.
  - Power circuit topology
  - Dod-VSVS
  - Capacitor balancing
  - PWM Scheme
  - Implementation
  - Results

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Power Circuit Topology
  - FC inverter followed by a cascaded H-Bridge (CHB)
  - 12 half bridges:
    - 6 rated for $V_{dc}/2$
    - 6 rated for $0.1445V_{dc}$
  - 6 capacitors:
    - 3 rated for $V_{dc}/2$
    - 3 rated for $0.1445V_{dc}$
  - Pole voltages:
    - $V_{AO} = V_{A'O} + V_{AA'}$
    - $V_{A'O} \in [0, \frac{V_{dc}}{2}, V_{dc}]$
  - $V_{AA'} \in [-0.1445V_{dc}, 0 \,\&\, +0.1445V_{dc}]$

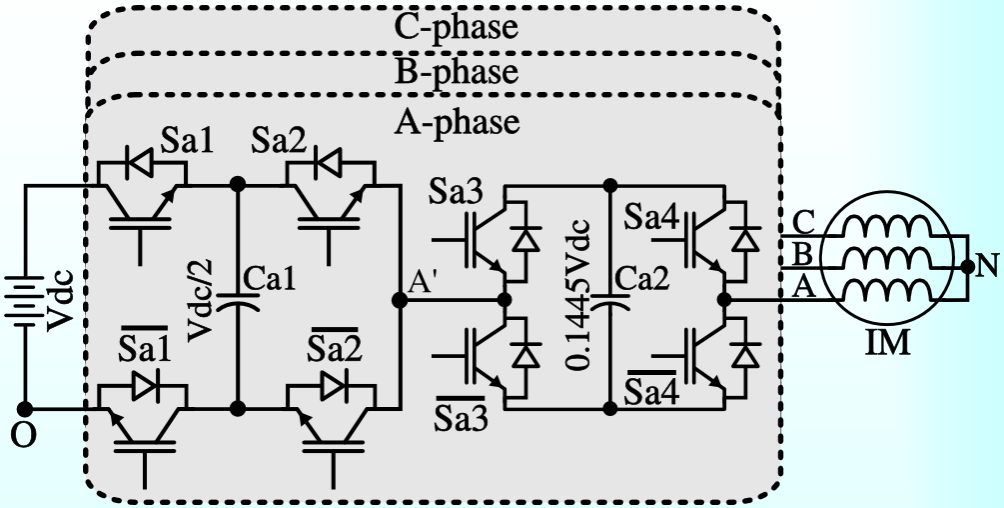


Fig: Power circuit topology for 6-con Dod-VSVS for star connected IMD

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Space Vector Structure
  - Obtained by superposition of VSVS of FC and CHB
  - For FC inverter:
    - $OX = \frac{V_{dc}}{2}; OY = V_{dc}$
    - Pole voltage ($V_{A'O}$) for switching state
      - `2′: V_{dc}
      - `1′: $\frac{V_{dc}}{2}$
      - `0′: 0
  - For CHB inverter:
    - $OX = 0.1445V_{dc}; OY = 0.289V_{dc}$
    - Pole voltage ($V_{AA'}$) for switching state
      - `2′: $+0.1445V_{dc}$
      - `1′: 0
      - `0′: $-0.1445V_{dc}$

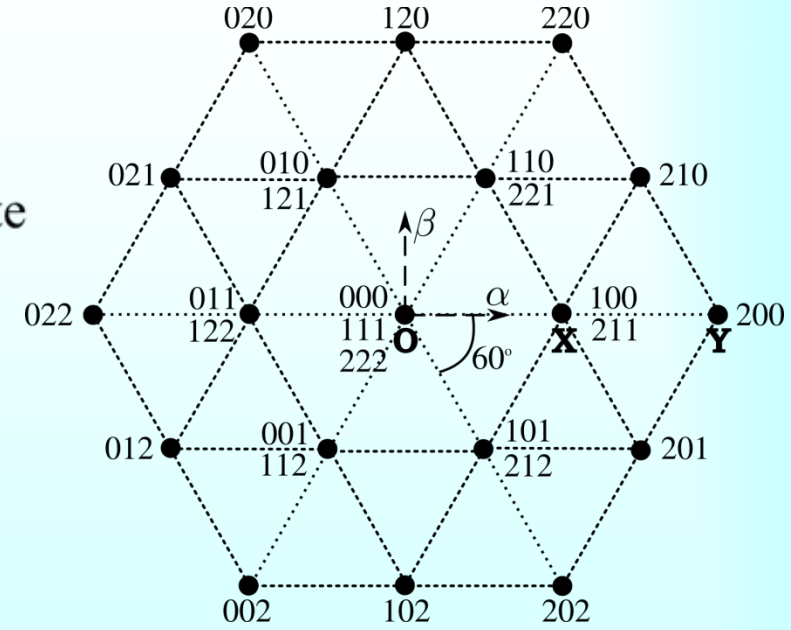


Fig: VSVS of 3L FC & CHB inverters

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Raw VSVS:
  - Obtained by superposition of primary and secondary three-level hexagonal structures
  - Dodecagonal vectors are generated using vectors from primary inverter and pseudo vectors from secondary inverter
  - Pseudo vectors are generated by switched averaging of vectors from secondary inverter

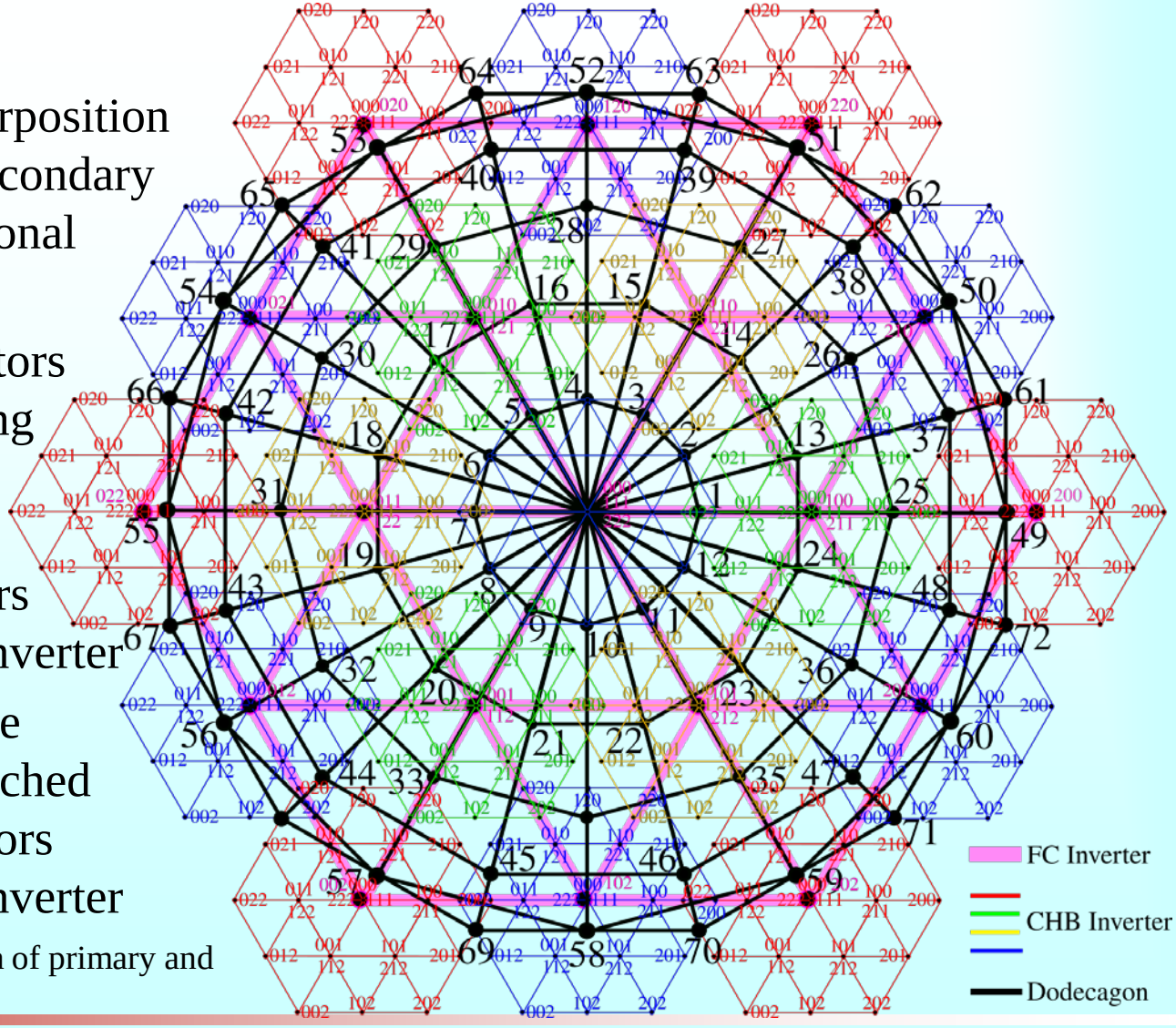


Fig: VSVS obtained by superposition of primary and secondary hexagons

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Example of dodecagonal vector generation using pseudo vectors (dotted lines):
  - Space vector structures are added together instead of subtracting as in the case of open-end winding
  - Vector 13 generated by averaging 101 and 112 with $k = 0.732$
  - Vector 61 generated by averaging 202 and 102 with $k' = 2k - 1 = 0.464$
    - $k' = 0.464$ used for odd-numbered vectors in E and all vectors in F
    - Prevents exceeding machine phase voltage rating & reduces INV2 dv/dt

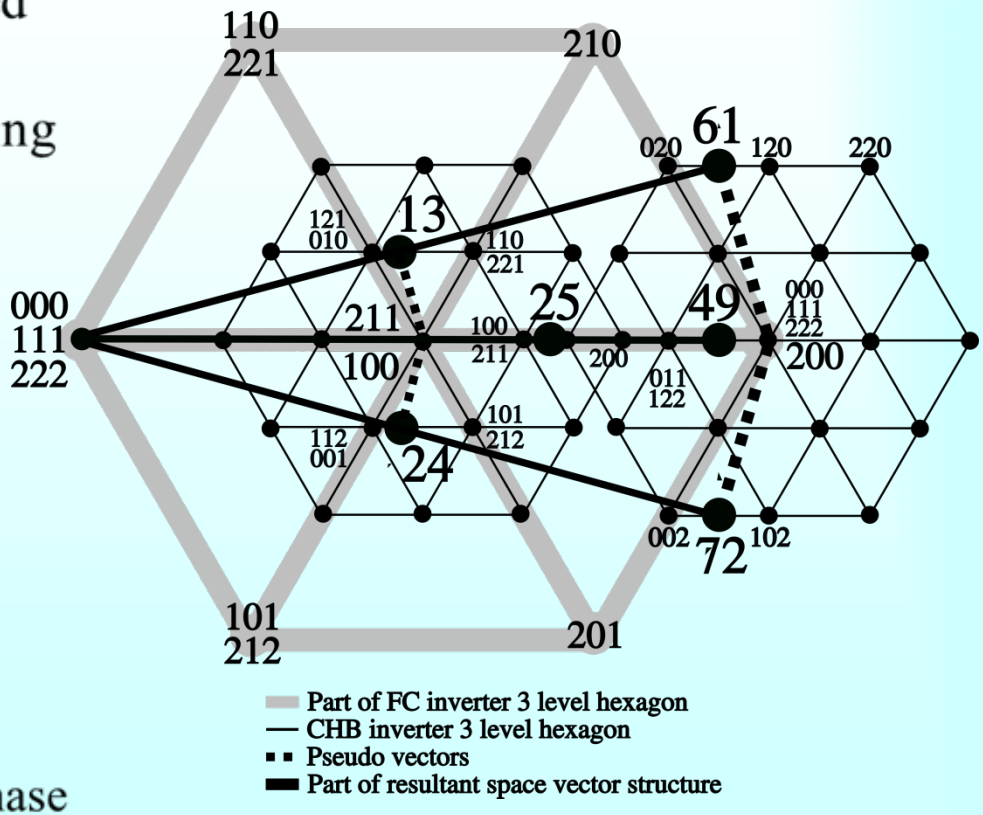


Fig: Dodecagonal vector generation

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Three vector switching:
  - Some of the dodecagonal vectors lie inside a triangle of secondary hexagon
  - Switching the vectors forming the triangular boundary results in reduced dv/dt in the phase voltage
  - For example, dodecagonal vector 48:
    - Could use vectors 120 and 210
      - k = 0.732 is used
    - But vectors [120, 220, 110] are used
      - $[k_0, k_1, k_2] = [0.464, 0.268, 0.268]$
  - Dodecagonal vectors having three vector switching are: 26, 28, 30, 32, 34, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 50, 52, 54, 56, 58, 60
  - Requires three k values: $[k_0, k_1, k_2];\ k_0 + k_1 + k_2 = 1$

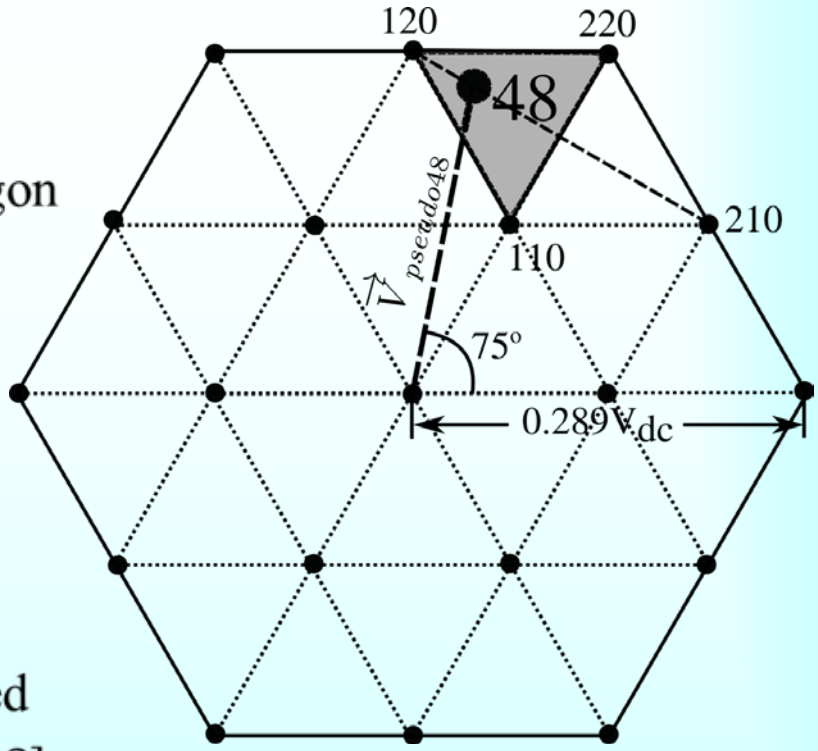


Fig: Dodecagonal vector generation using 3 vector switching

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Set of k values used:
  - Denoted as $[k_0, k_1, k_2]; k_0 + k_1 + k_2 = 1$

Dodecagonal Vectors	k values
0, 2, 4, 6, 8, 10, 12	[1, 0, 0]
1, 3, 5, 7, 9, 11, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 27, 29, 31, 33, 35	[0.732, 0, 0.268]
26, 28, 30, 32, 34, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 50, 52, 54, 56, 58, 60	[0.464, 0.268, 0.268]
49, 51, 53, 55, 57, 59, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72	[0.464, 0, 0.536]

Table: k-value sets used for secondary inverter vector switching

- An LUT stores this information inside the digital controller

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Space vector structure:
  - 6 concentric dodecagons: A-F
  - 73 vectors including zero vector
  - Two types of dodecagons:
    - Type1: B, D, F
    - Type2: A, C, E
  - $R_A : R_B : R_C : R_D : R_E : R_F = \cos(75^o) : \cos(60^o) : \cos(45^o) : \cos(30^o) : \cos(15^o) : \cos(0^o)$
  - $R_F = 0.966 V_{dc}$
  - Density increases at higher modulation range
  - Dodecagons are formed in a switched average sense

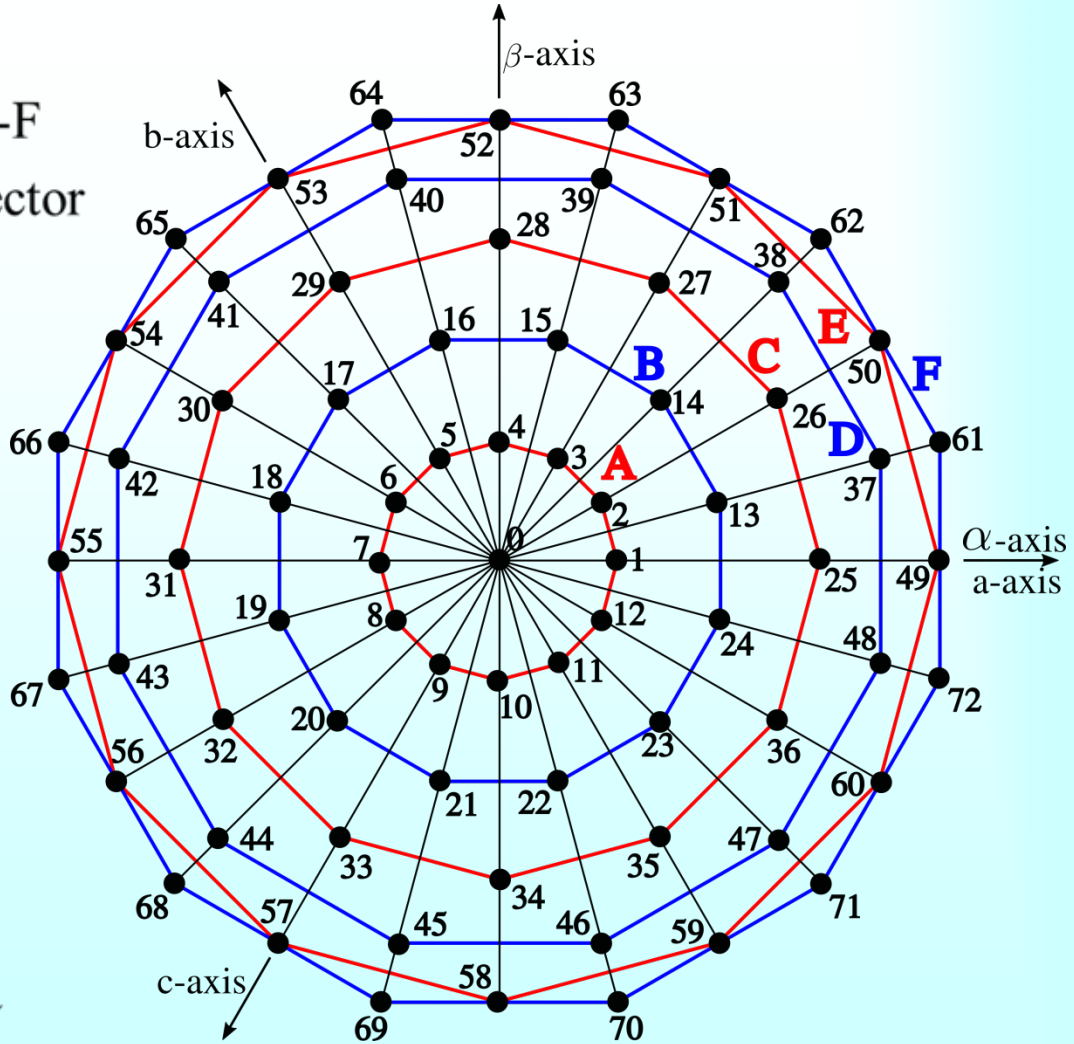
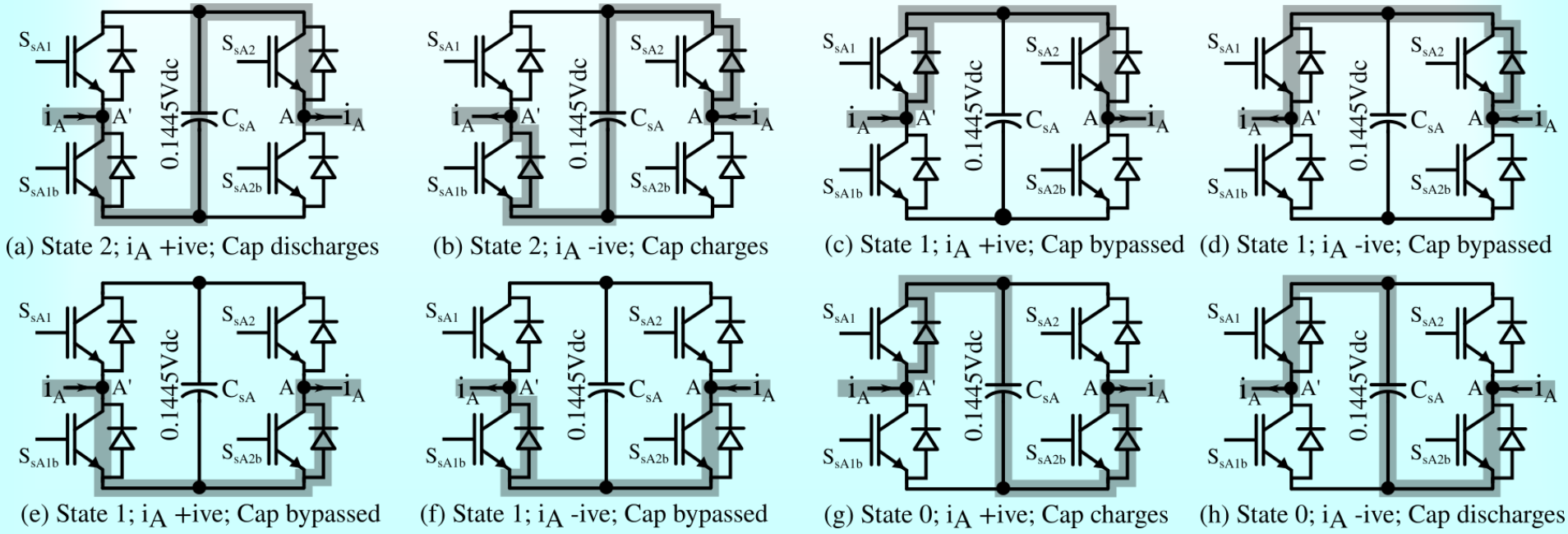


Fig: Resultant 6-con Dod-VSVS

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Capacitor Balancing:
  - FC capacitor balancing (C_{a1}, C_{b1}, C_{c1}) is same as explained before
  - CHB capacitors (C_{a2}, C_{b2}, C_{c2}) have to be balanced individually
    - Adjusting k value
  - Capacitor voltage ripple depends on applied state and phase current direction



(a) State 2; i_A +ive; Cap discharges (b) State 2; i_A -ive; Cap charges (c) State 1; i_A +ive; Cap bypassed (d) State 1; i_A -ive; Cap bypassed

(e) State 1; i_A +ive; Cap bypassed (f) State 1; i_A -ive; Cap bypassed (g) State 0; i_A +ive; Cap charges (h) State 0; i_A -ive; Cap discharges

Fig: CHB inverter switching states, currents and effect on capacitor

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- CHB Capacitor Balancing:
  - State `2′ discharges & `0′ charges cap for a positive current
  - State `2′ charges & `0′ discharges cap for a negative current
  - CHB capacitors are naturally balanced, forced balancing is required during startup and to meet non-idealities
  - CHB capacitors (C_{a2}, C_{b2}, C_{c2}) have to be balanced individually
    - Adjusting k value
  - Forced balancing depends on the vectors applied from CHB inverter to generate the pseudo vectors. Example:
    - 020 & 120 (to generate vector 61)
      - Modifying k affects A-phase cap only
    - 102 & 201 (to generate vector 37)
      - Modifying k affects A & C-phase caps
    - 200 & 201 (to generate vector 69)
      - Modifying k affects C-phase cap only

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- CHB Cap Balancing:
  - Consider CHB vector pair 200 & 201(to generate vector 69)
    - Assume 200 & 201 are switched averaged over time duration T_x
      - 200 applied for kT_x duration & 201 applied for $(1-k)T_x$ duration
    - A-phase: State 2 applied for entire T_x duration
    - B-phase: State 0 applied for entire T_x duration
    - C-phase:
      - State 0 applied for $k * T_x$ duration
      - State 1 applied for $(1-k) * T_x$ duration
    - Changing the value of k affects only C-phase capacitor
    - For positive C-phase current:
      - Applying state 0 for longer duration charges C-phase cap
      - Applying state 1 for longer duration discharges C-phase cap
    - For negative C-phase current:
      - Applying state 0 for longer duration discharges C-phase cap
      - Applying state 1 for longer duration charges C-phase cap

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- CHB Cap Balancing:
  - Dodecagonal vectors 1, 7, 13, 18, 19, 24, 25, 30, 31, 36, 37, 42, 43, 48, 49, 55, 60, 61, 66, 67 & 72 are used for balancing A-phase cap (C_{a2})
  - Vectors shifted 120^o & 240^o to above vectors are used for balancing B-phase & C-phase caps (C_{b2} &C_{c2}) respectively
  - SVL in RED used for A-phase cap
  - SVL in GREEN used for B-phase cap
  - SVL in BLUE used for C-phase cap
  - Stored in an LUT

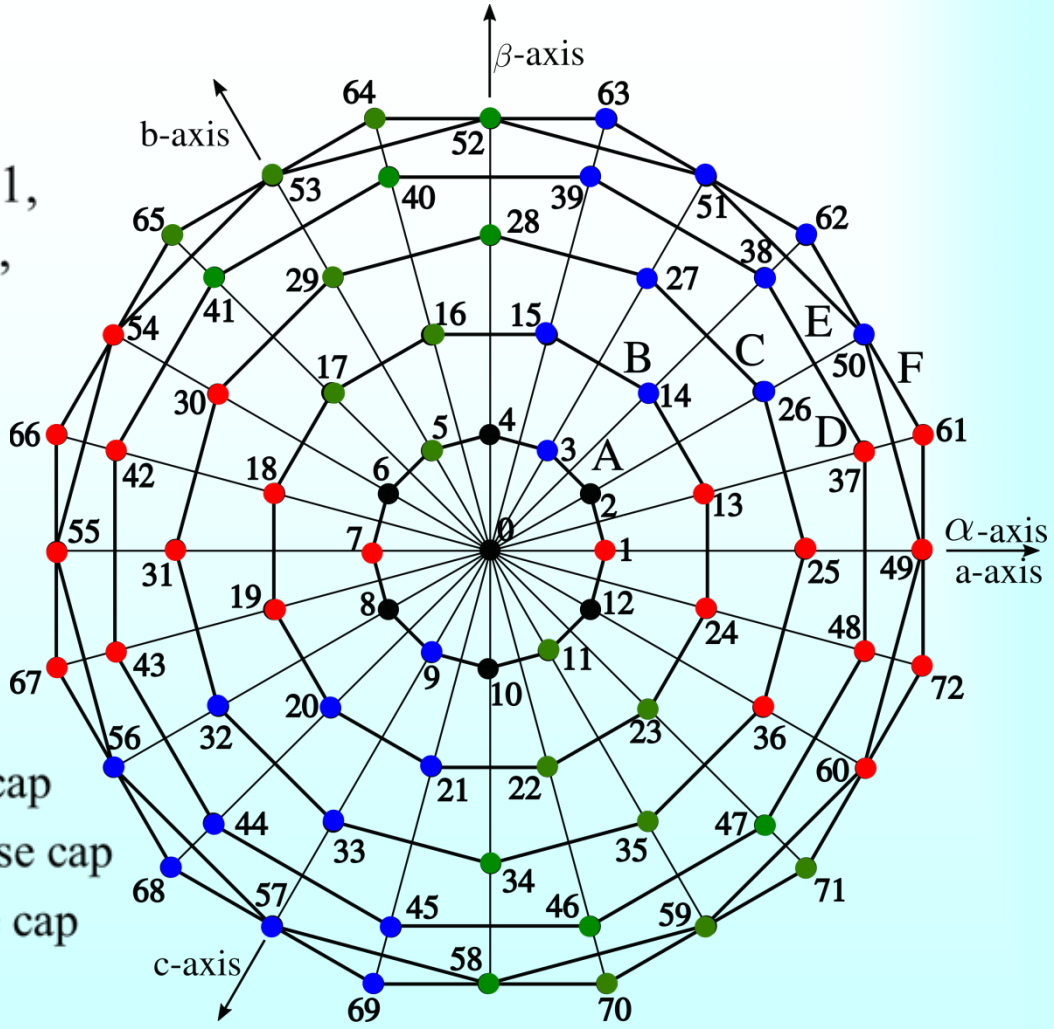


Fig: Vectors used in capacitor balancing

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- CHB Cap Balancing:
  - Capacitor voltage errors are obtained and checked whether they are within a band
  - Polarity of error, direction of current and control sense are used to generate polarity of Δk
  - LUT gives the k values and the control sense
  - Control sense:
    - Which k values to modify
    - In what direction to modify (increase or decrease)

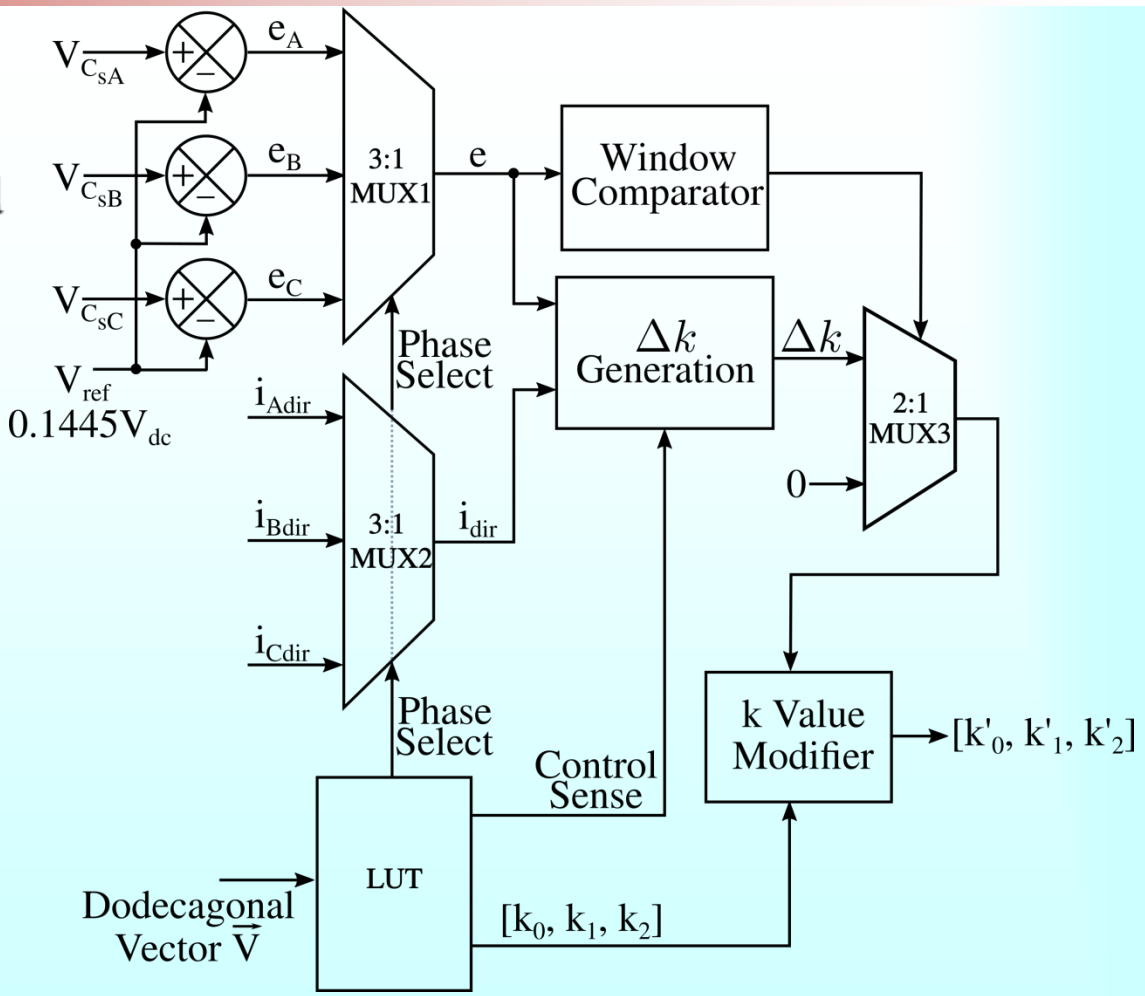


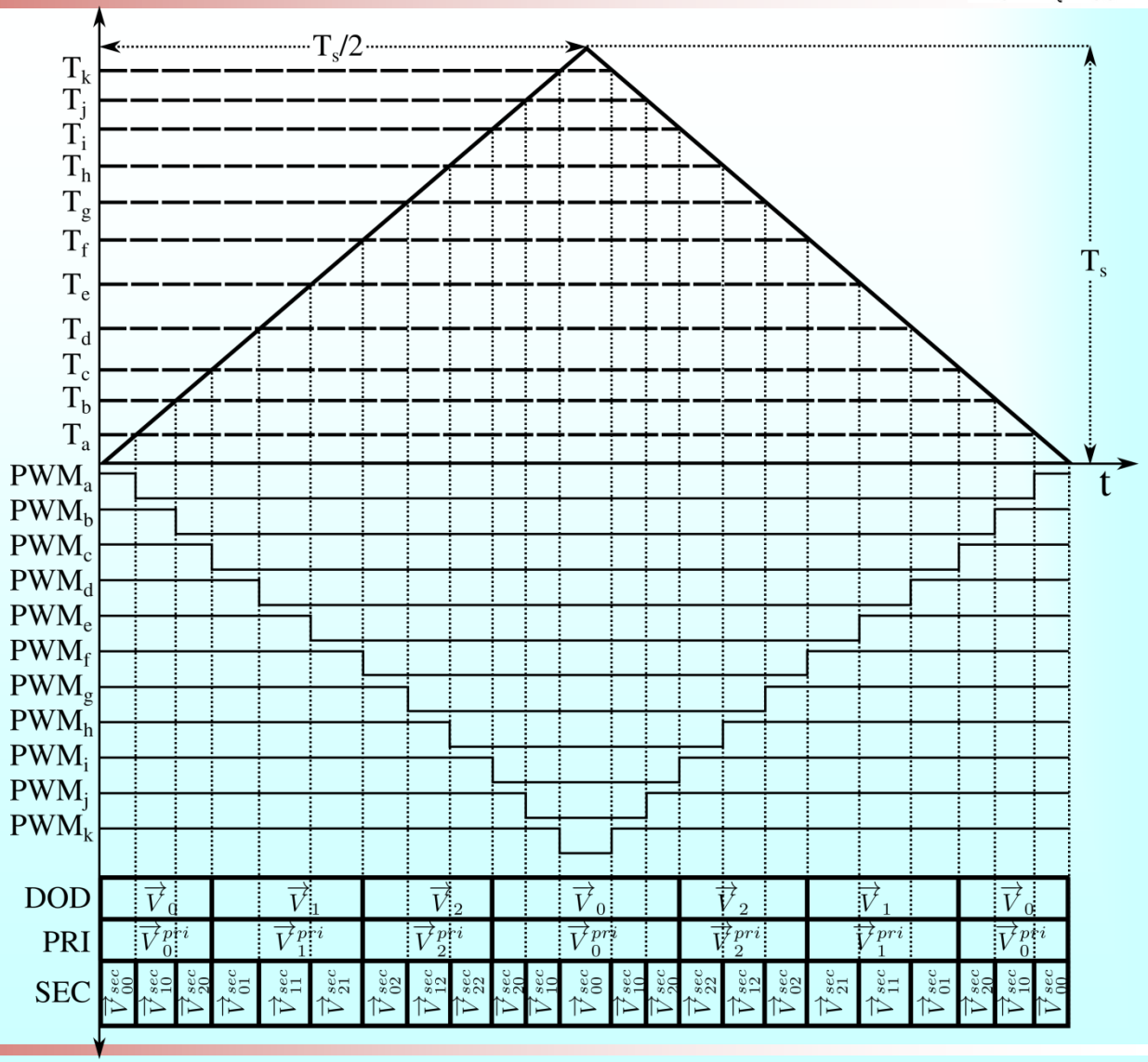
Fig: CHB capacitor voltage controller

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Capacitor Design:
  - Flying capacitors design is same as before
  - CHB capacitor design:
    - Nominal voltage $=0.1445V_{dc}$
    - CHB capacitor charges when state `0′ is applied
    - CHB capacitor discharges when state `2′ is applied
    - CHB capacitor is unaffected when state `1′ is applied
  - Design CHB capacitors for longest duration for which state `0′ or `2′ is applied (T_{st02}) with peak current flowing through them
    - $C = \frac{(100 * I_p * T_{st02})}{r * V_c}$; $T_{st02} = \frac{1}{spc * f_m}$
  - Example: For $50Hz$ operation at $12spc$, $V_c = 28.9V$, $I_p = 10A$ and target $r = 5\%$: $C = \frac{100*10}{12*50*5*28.9} = 11534uF$

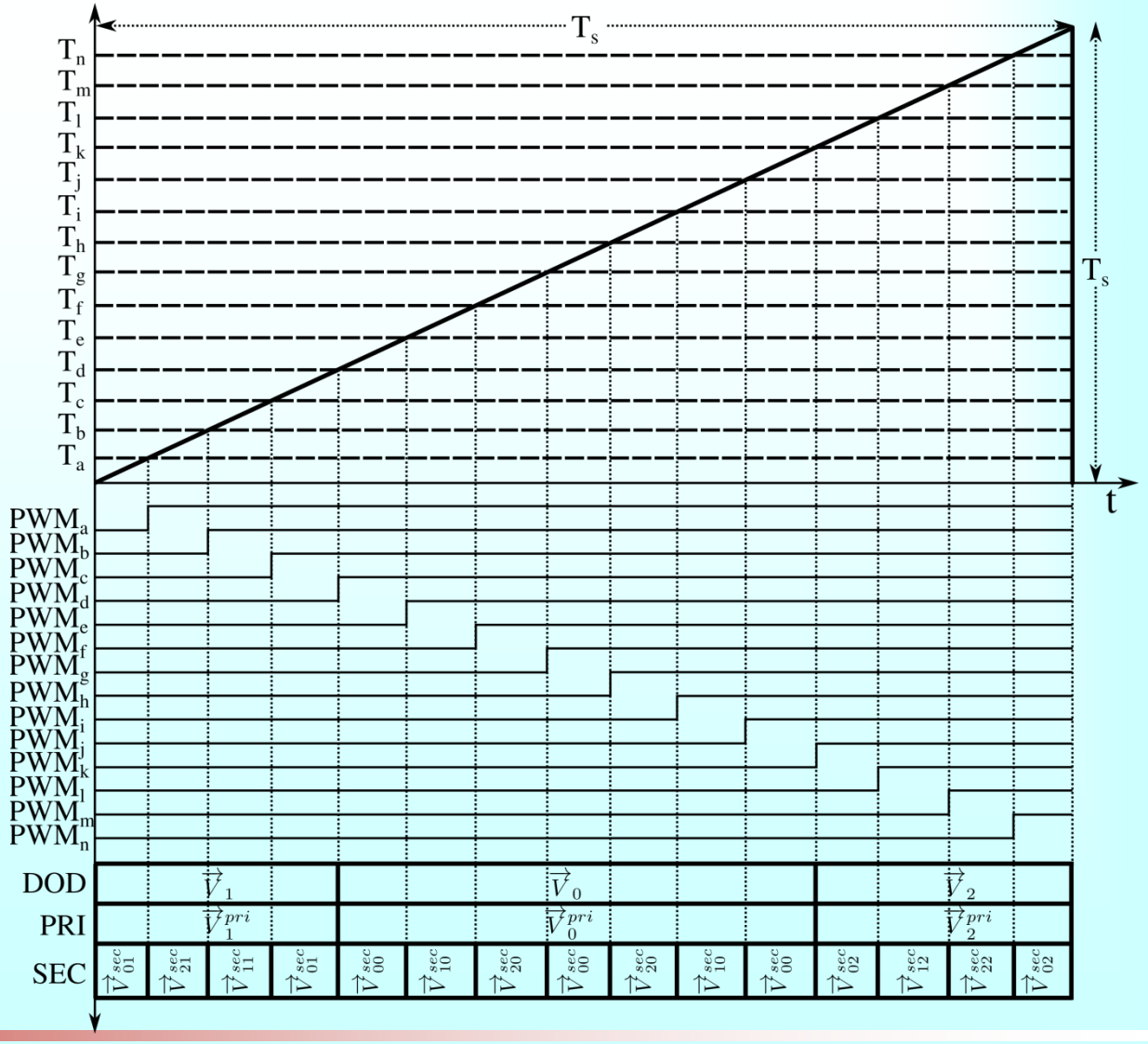
Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- PWM Schemes:
- Scheme1
- 0-1-2-0-2-1-0 seq
- Timing values T_0, T_1, T_2 and vectors V_0, V_1, V_2 obtained as before
- Scheme1 is used at lower modulation indices



Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- PWM Schemes:
- Scheme2
- 1-0-2 sequence
- Scheme2 is used at higher modulation indices
- Results in quasi-square switching of primary inverter



Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Implementation:
  - $V_{dc} = 200V$
  - SKM75GB12T4 (75A, 1200V) IGBT half-bridge based inverters
  - 3phase currents, capacitor voltages & V_{dc} are sensed
  - Capacitors:
    - INV1 FC: 2200uF
    - INV2 CHB: 2200uF

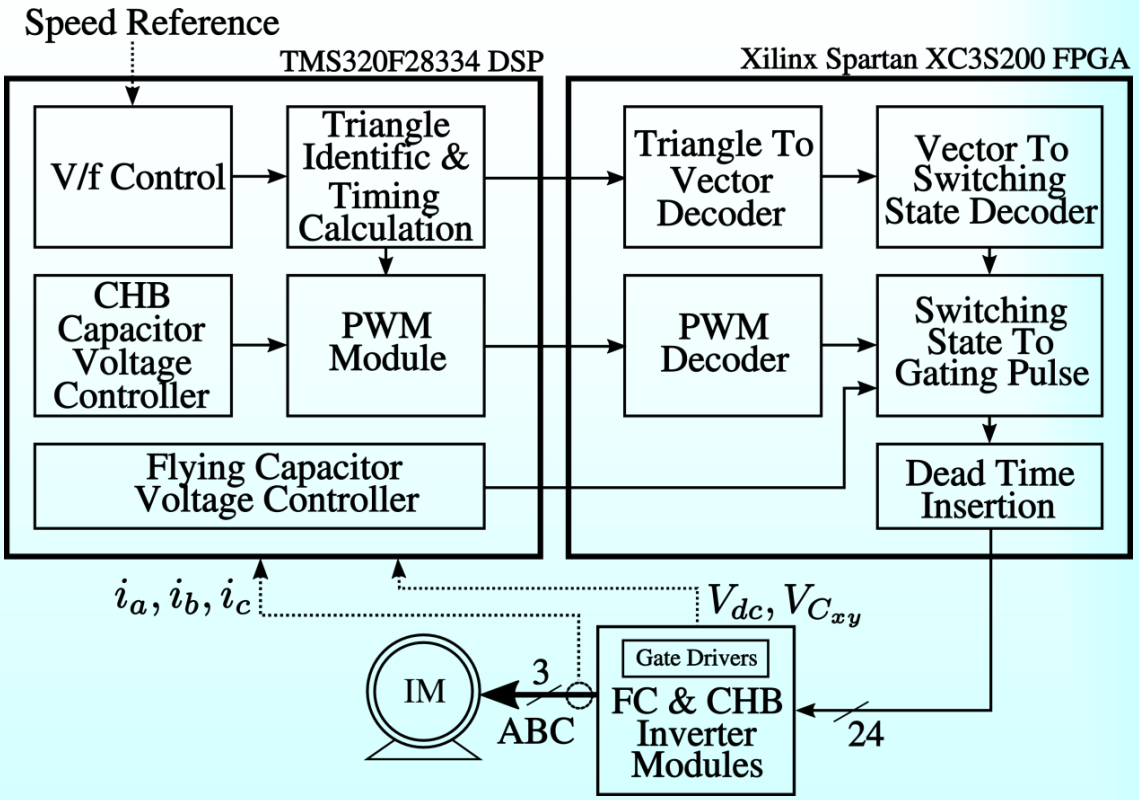


Fig: Hardware implementation block diagram

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Implementation:

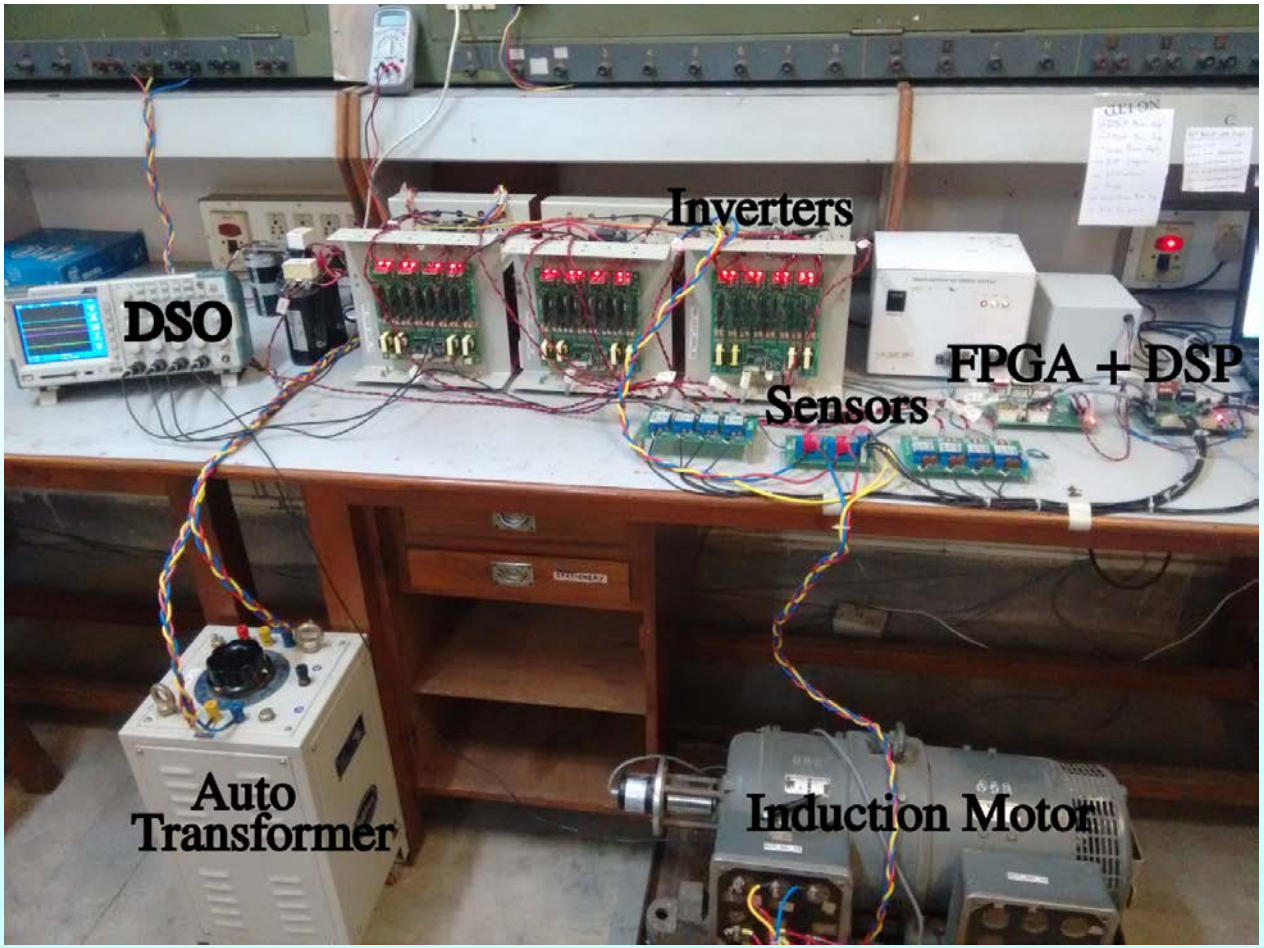


Fig: Hardware implementation

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Steady state results:

10Hz (M=0.2)Operation – 48spc – PWM1

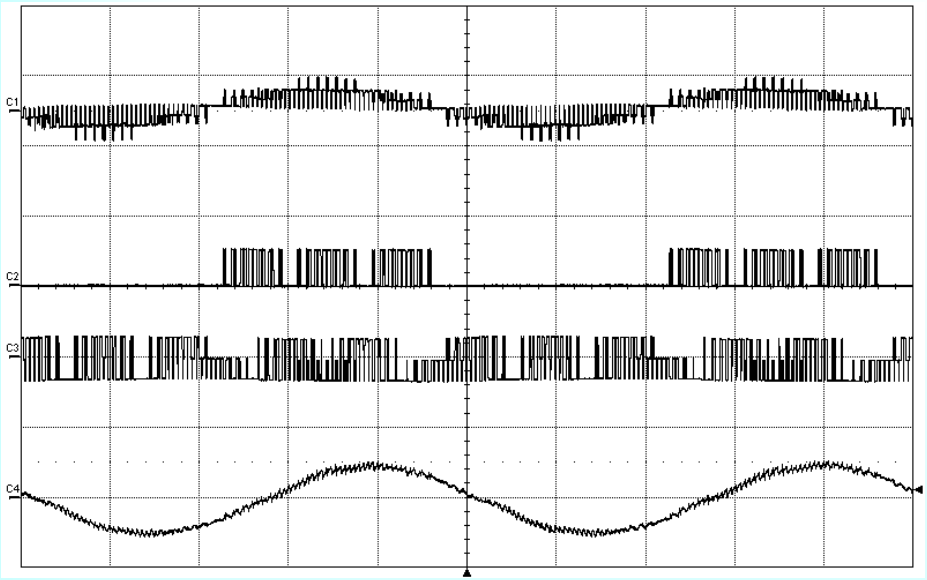


Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 100V/div, (4) Current, 1A/div; X-axis: 20mS/div

30Hz (M=0.6) Operation – 24spc – PWM1

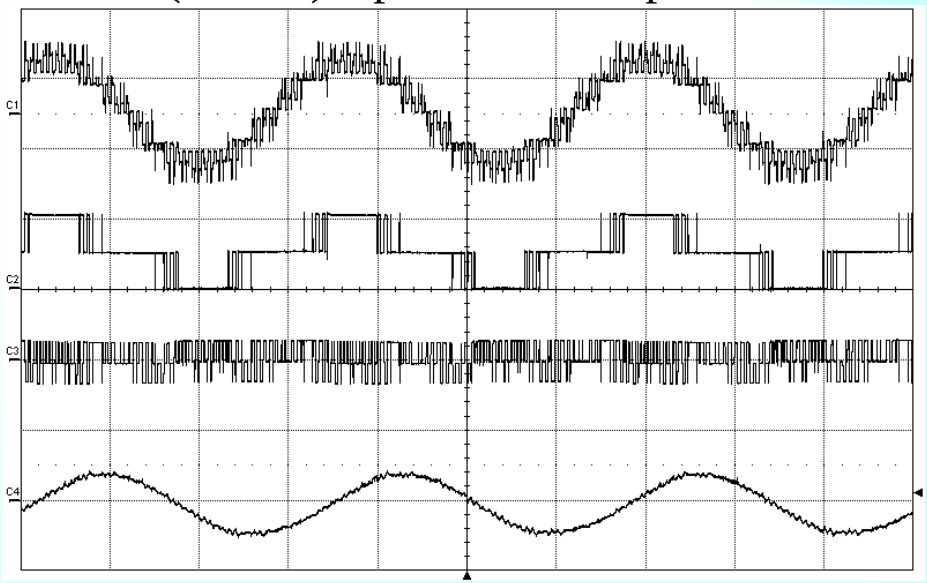


Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 100V/div, (4) Current, 1A/div; X-axis: 10mS/div

- Higher frequency switching happens in secondary inverter at low voltage

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Steady state results:

40Hz (M=0.8) Operation – 24spc – PWM1

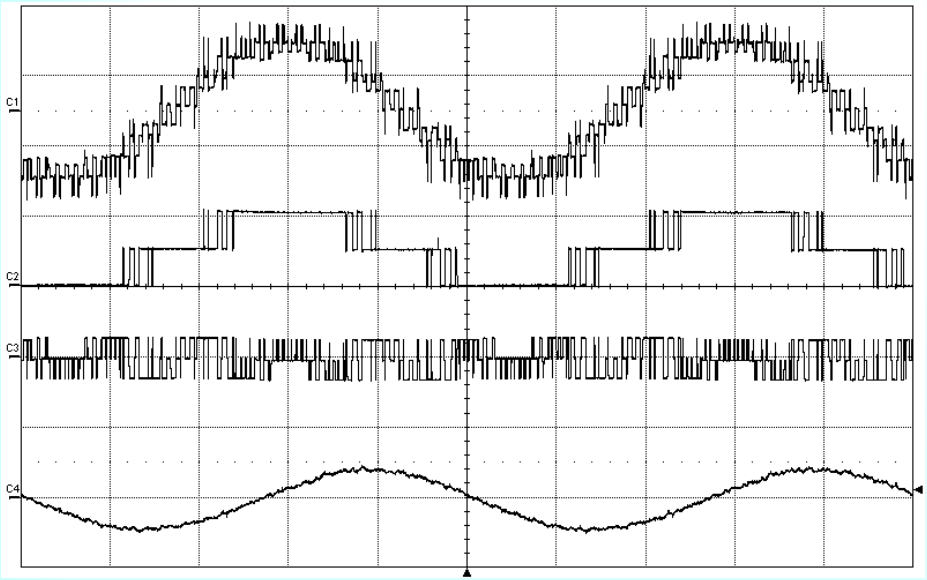


Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 100V/div, (4) Current, 1A/div; X-axis: 5mS/div

48Hz (M=0.96)Operation – 12spc – PWM2

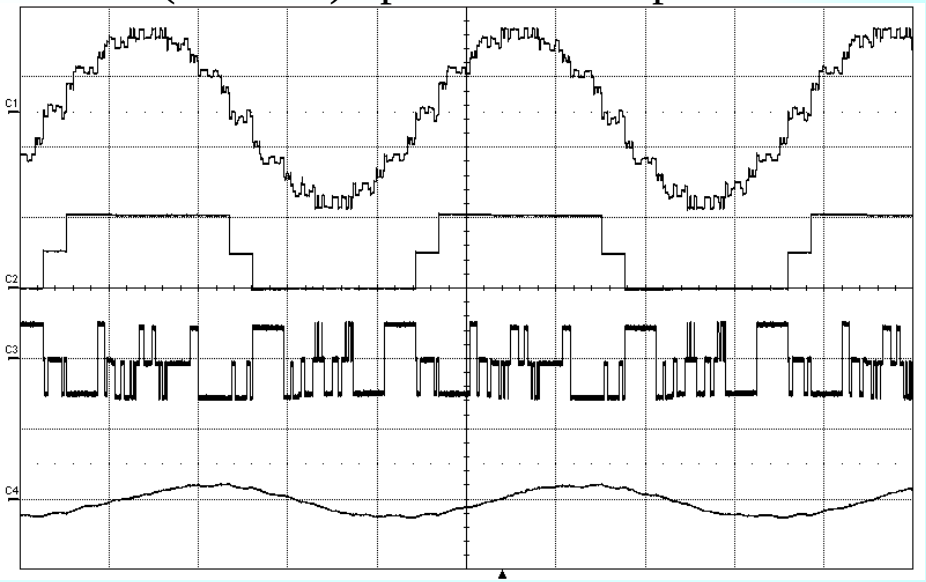


Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 100V/div, (4) Current, 2A/div; X-axis: 5mS/div

- Primary inverter switches in quasi-square mode, switching losses are reduced

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Steady state results:

50Hz (M=1), 12-step mode – 12spc – PWM2

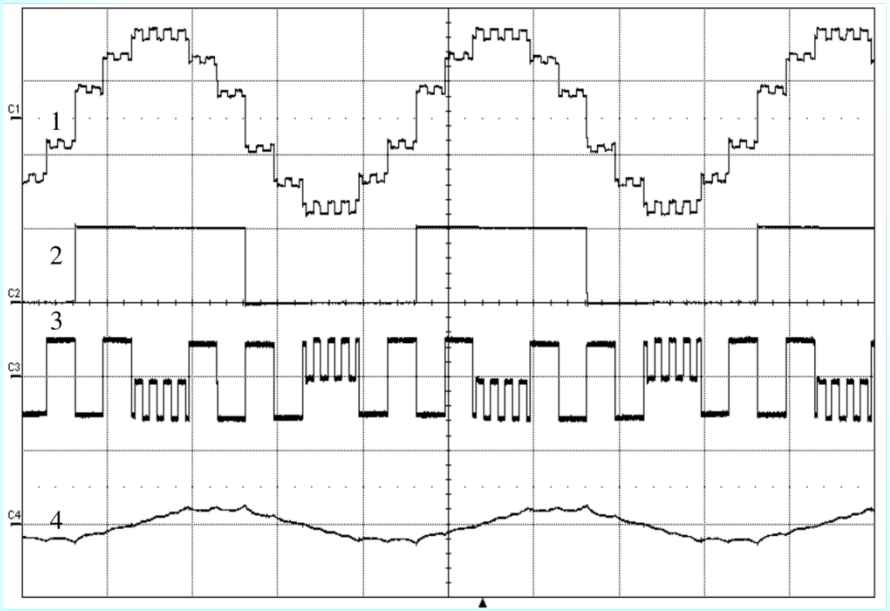


Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 100V/div, (3) CHB inverter pole voltage, 100V/div, (4) Current, 2A/div;

FFT - 50Hz (M=1) Operation – 12spc

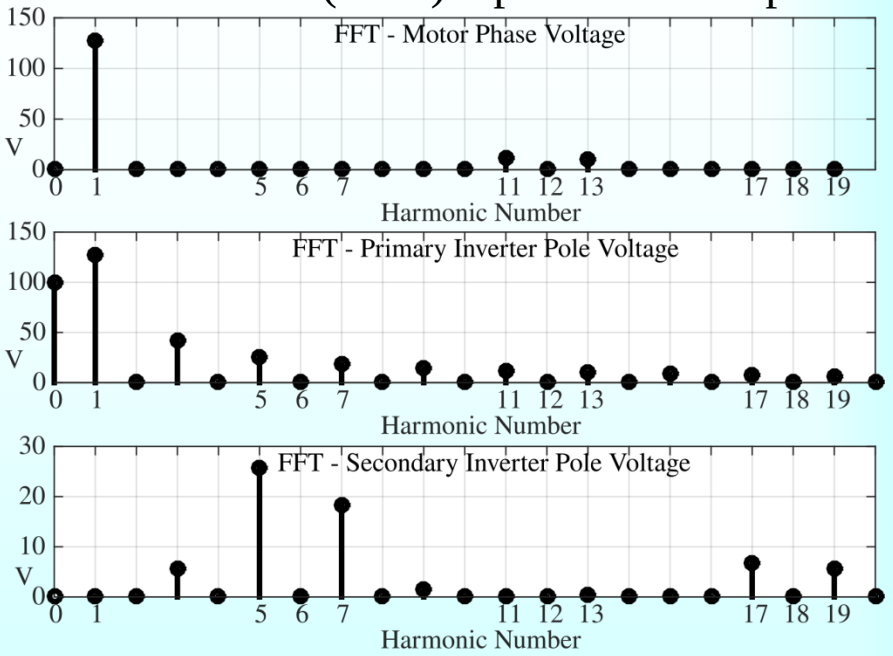


Fig: FFT of (a) FC inverter pole voltage; (b) CHB inverter pole voltage; (c) motor phase voltage;

- Primary inverter switches in square wave mode
- No fundamental voltage contribution form INV2/CHB inverter

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Transient results:

10-48Hz (M=0.2 to 0.96) Acceleration – 12spc

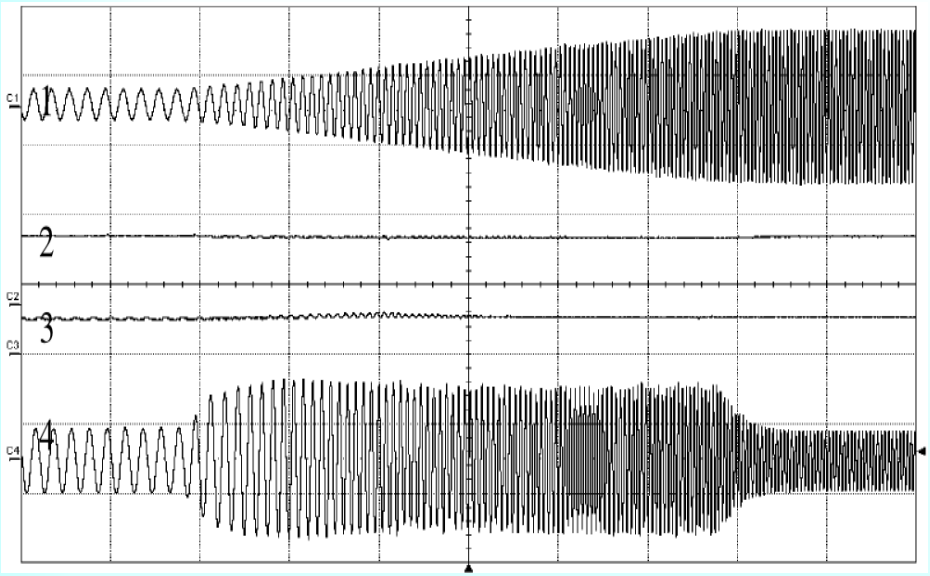


Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) Sec flying cap, 50V/div, (3) Secondary DC-link, 50V/div, (4) Current, 2A/div; X-axis: 1S/div

Startup – 48Hz (M=0.96)

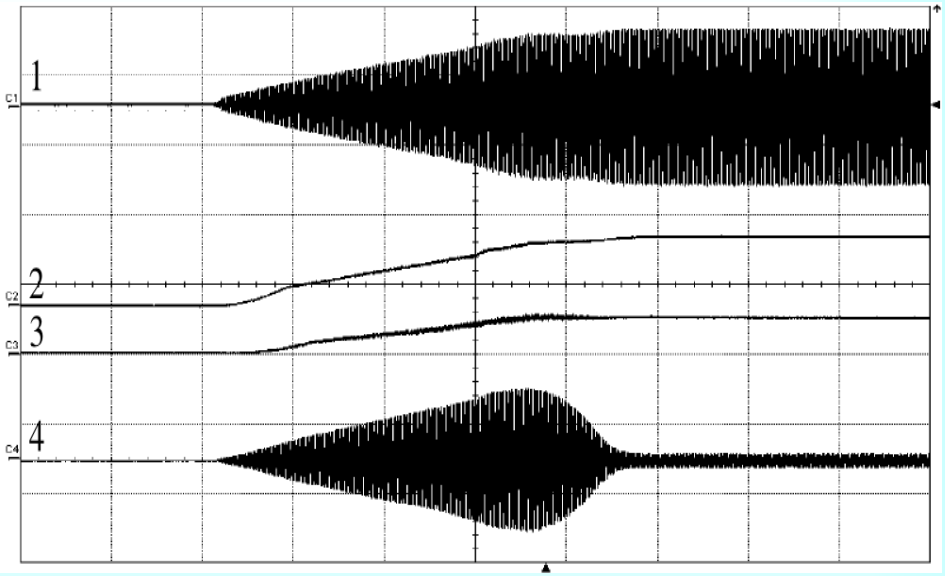


Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter flying cap, 100V/div, (3) CHB inverter floating cap, 50V/div, (4) Current, 5A/div; X-axis: 1S/div

- Capacitor voltages reaches steady-state without the need of any pre-charging circuitry, voltage balancing happens inherently with the PWM

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Transient results:

CHB Cap Voltage Controller Testing

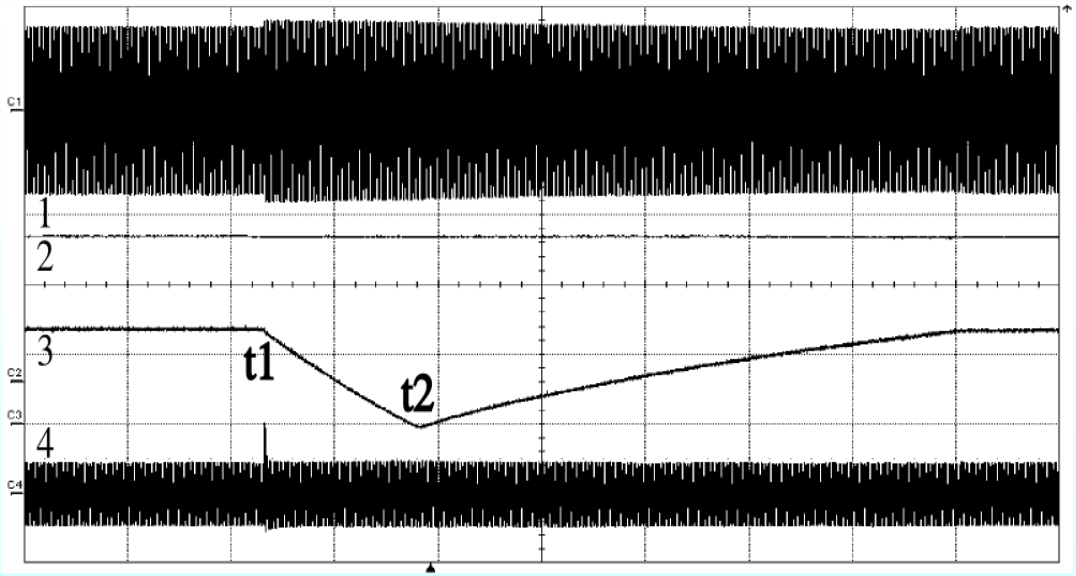


Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter flying cap, 50V/div, (3) CHB inverter floating cap, 20V/div, (4) Current, 1A/div; X-axis: 1S/div

- Controllers are disabled at point t1 and then re-enabled at point t2

Multilevel Dod-VSVS Using a Single DC Source for a Star Connected IMD

- Conclusion:
  - A multilevel dodecagonal space vector structure using a single DC source for a star connected IM is obtained
  - Four quadrant operation is easier since only one DC source is required
  - $6n \pm 1, n = odd$ order harmonics in the phase voltage are eliminated over the entire modulation range
  - Dominant 6^{th} order harmonic torque generation avoided
  - Switching losses are less both in primary and secondary inverters
  - Multilevel structure brings advantages like lesser dv/dt and better THD
  - No capacitor pre-charging circuitry is required, voltage buildup & balancing happens inherently with PWM
  - Linear modulation till $48.83Hz$ $(0.622V_{dc})$
  - Machine phase voltage rating never exceeded
  - Suitable for high performance medium voltage IM drive applications

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Oct-VSVS using single DC source
  - Two-level
  - Extension to multilevel
- Topology
- PWM scheme
- Capacitor balancing & design
- Implementation
- Results

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Octadecagon Using Single DC Source:
- Octadecagonal vectors generated in a switched-averaged sense
  - Two inverters, primary and secondary; two hexagons, primary and secondary
  - Pseudo vectors are generated from secondary hexagon to form octadecagonal vectors
- Example

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Octadecagon Using Single DC Source:
- Octadecagonal vectors generated in a switched-averaged sense
  - Two inverters, primary and secondary; two hexagons, primary and secondary
  - Pseudo vectors are generated from secondary hexagon to form octadecagonal vectors
- Example
  - Primary inverter applies vector **OA**
  - Secondary inverter generates pseudo vectors **Vp18**, **Vp1**, **Vp2**
  - **V18 = OA + Vp18**
    V1 = OA + Vp1
    V2 = OA + Vp2

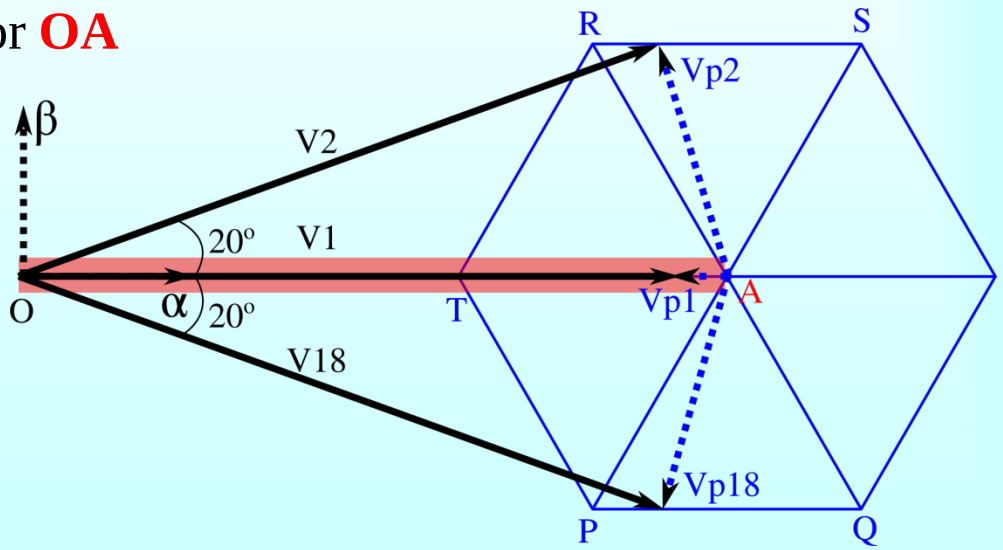


Fig: Octadecagonal Vector Generation

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Octadecagon Using Single DC Source:
- If the resultant octadecagon generates fundamental voltage output equal to the fundamental voltage output from primary inverter:
  - Secondary inverter delivers zero average power
- The condition is given by:
  - Voct = |V18| = |V1| = |V2|
  - 0.637Vdc = 0.6637Voct
  - Voct = 0.9598Vdc
  - Values of **Vp18**, **Vp1**, **Vp2** found using vector algebra

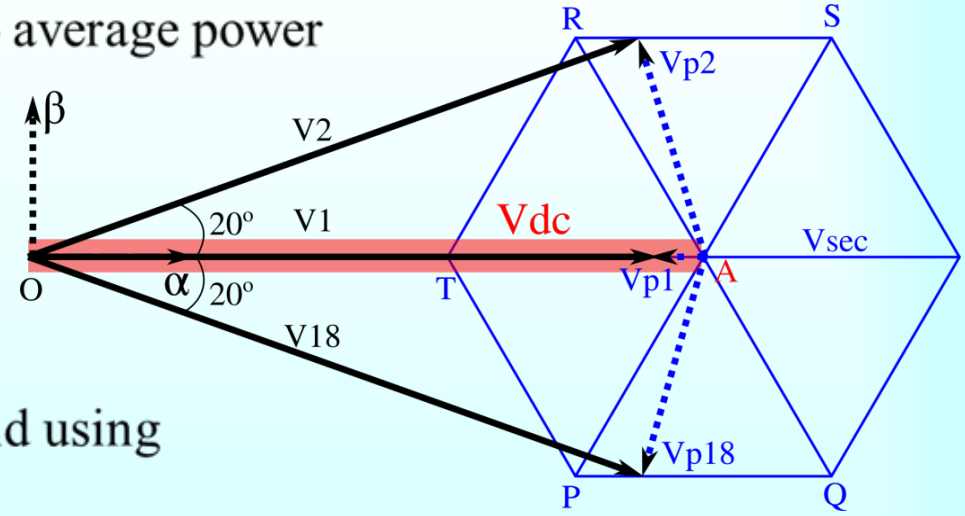


Fig: Octadecagonal Vector Generation

- Single DC source operation
  - DC source of Vdc for primary inverter
  - Secondary inverter DC-link maintained using capacitor

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Octadecagon Using Single DC Source:
- Values of Vp18, Vp1 & Vp2 (pseudo vectors) are:
  - $Vp18 = 0.3426Vdc\angle -106.63^o$
  - $Vp1 = 0.0402Vdc\angle 180^o$
  - $Vp2 = 0.3426Vdc\angle 106.63^o$
- Secondary inverter DC-link voltage $Vsec = 0.379Vdc$
- Pseudo vectors are generated in a switched-averaged sense:
  - $Vp2 * T_s = [AR * T_s * k] + [AS * T_s * (1 - k)]$
  - T_s is the duration for which V2 has to be applied & $0 \leq k \leq 1$
  - $k = 0.7587$ is obtained
- Similarly other pseudo vector values and 'k' values are obtained

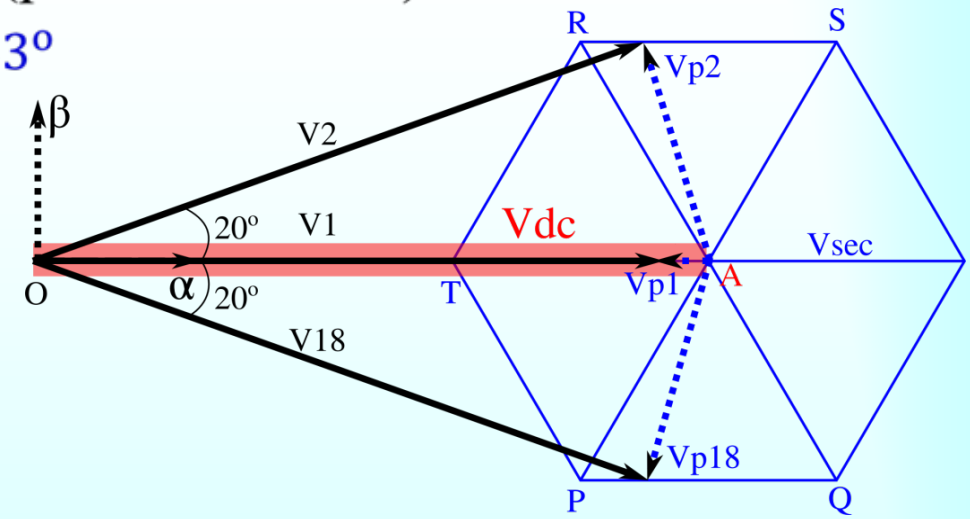


Fig: Octadecagonal Vector Generation

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Octadecagon Using Single DC Source:
  - Requires two 2-level inverters
  - The structure is only a 2-level octadecagon
  - How to get a multilevel structure using single DC source?
    - Generate two independent octadecagons & take superposition of all vectors
    - 162 active vectors forming a 9-concentric octadecagonal structure is obtained

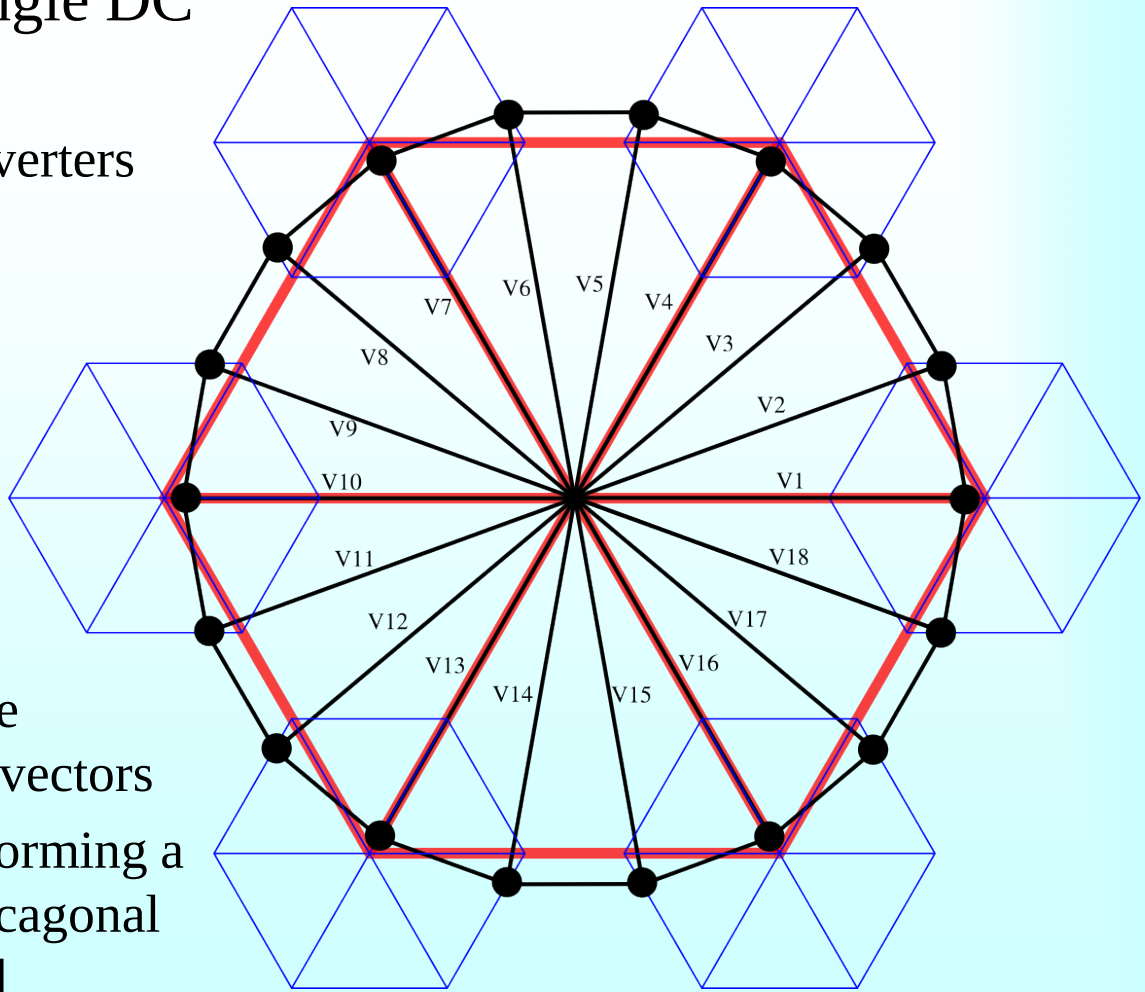


Fig: 2-level Octadecagon Generation

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Superposition:

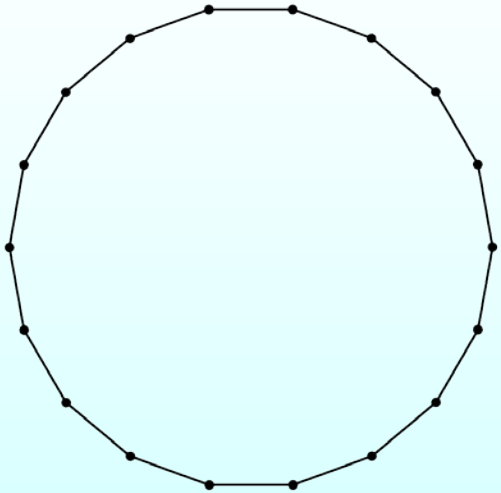


Fig: Superposition of two 2-level octadecagons

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Superposition:

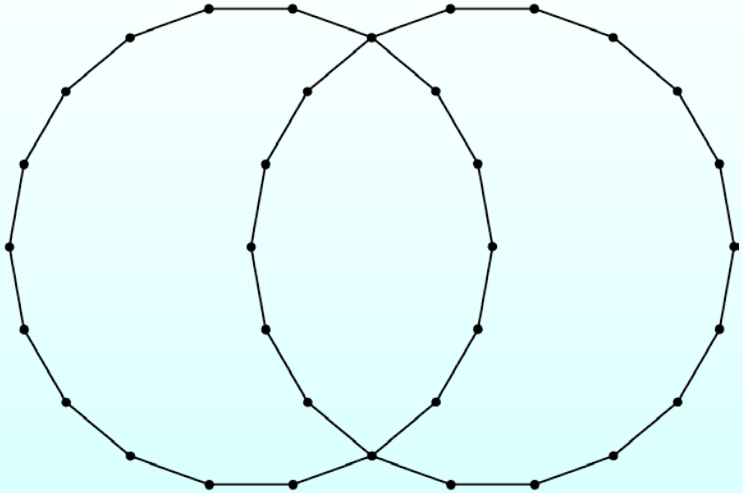


Fig: Superposition of two 2-level octadecagons

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Superposition:

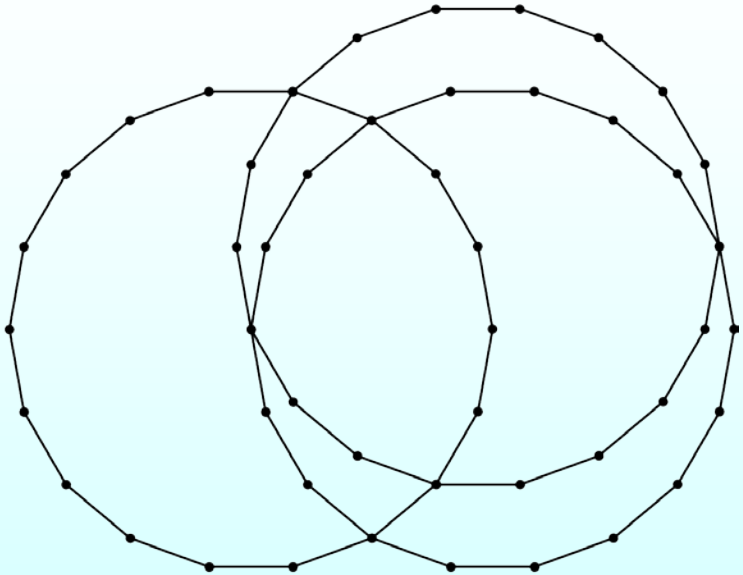


Fig: Superposition of two 2-level octadecagons

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Superposition:

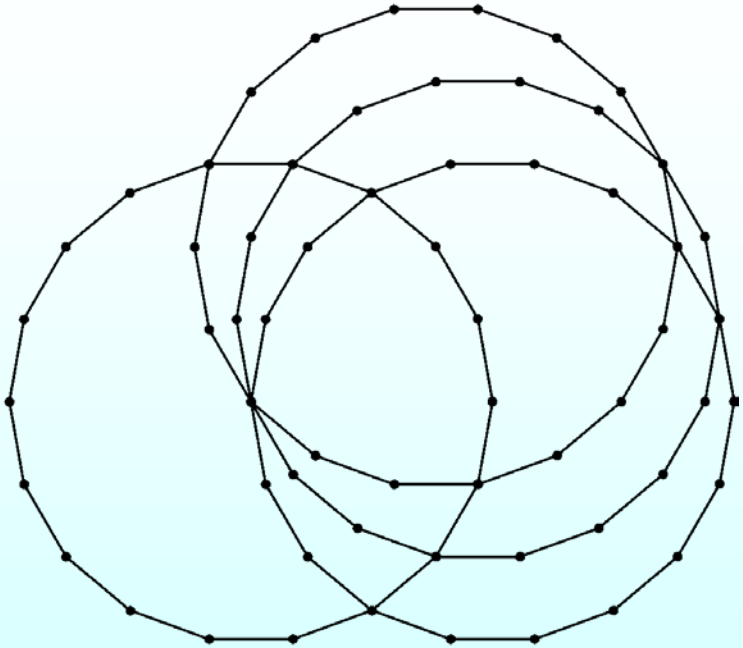


Fig: Superposition of two 2-level octadecagons

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Superposition:

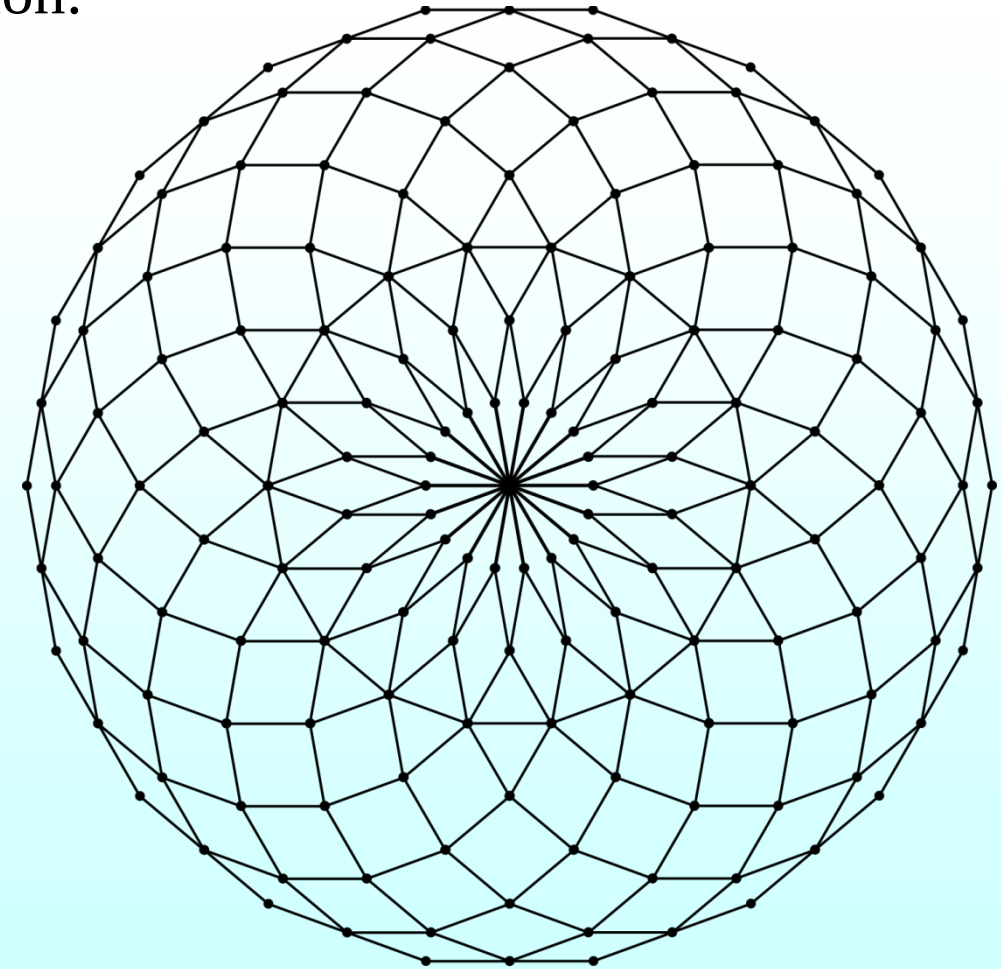


Fig: Superposition of two 2-level octadecagons

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Superposition:

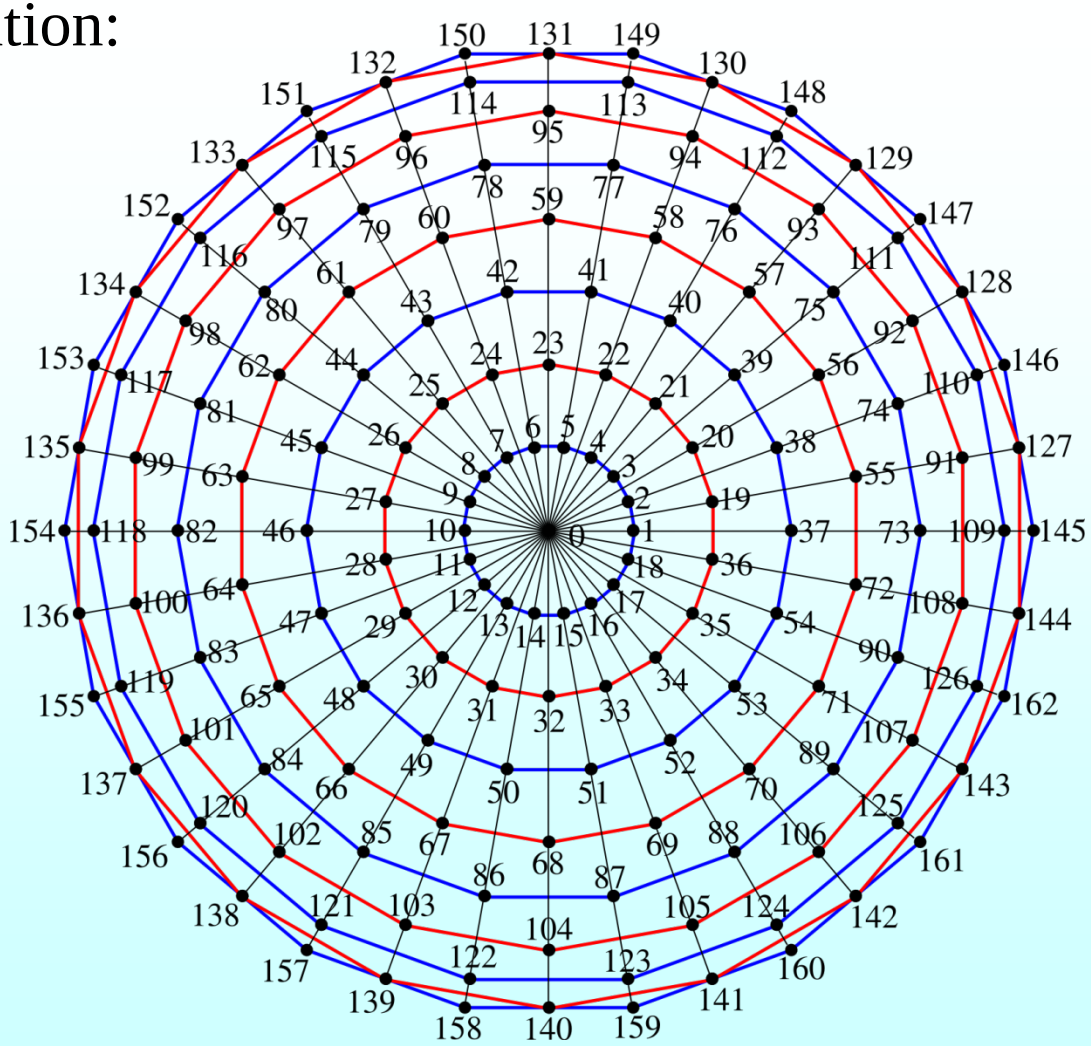


Fig: Superposition of two 2-level octadecagons

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Raw VSVS:
  - Obtained by superposition of primary and secondary three-level hexagonal structures
  - Octadecagonal vectors are generated using vectors from primary inverter and pseudo vectors from secondary inverter
  - Pseudo vectors are generated by switched averaging of vectors from secondary inverter

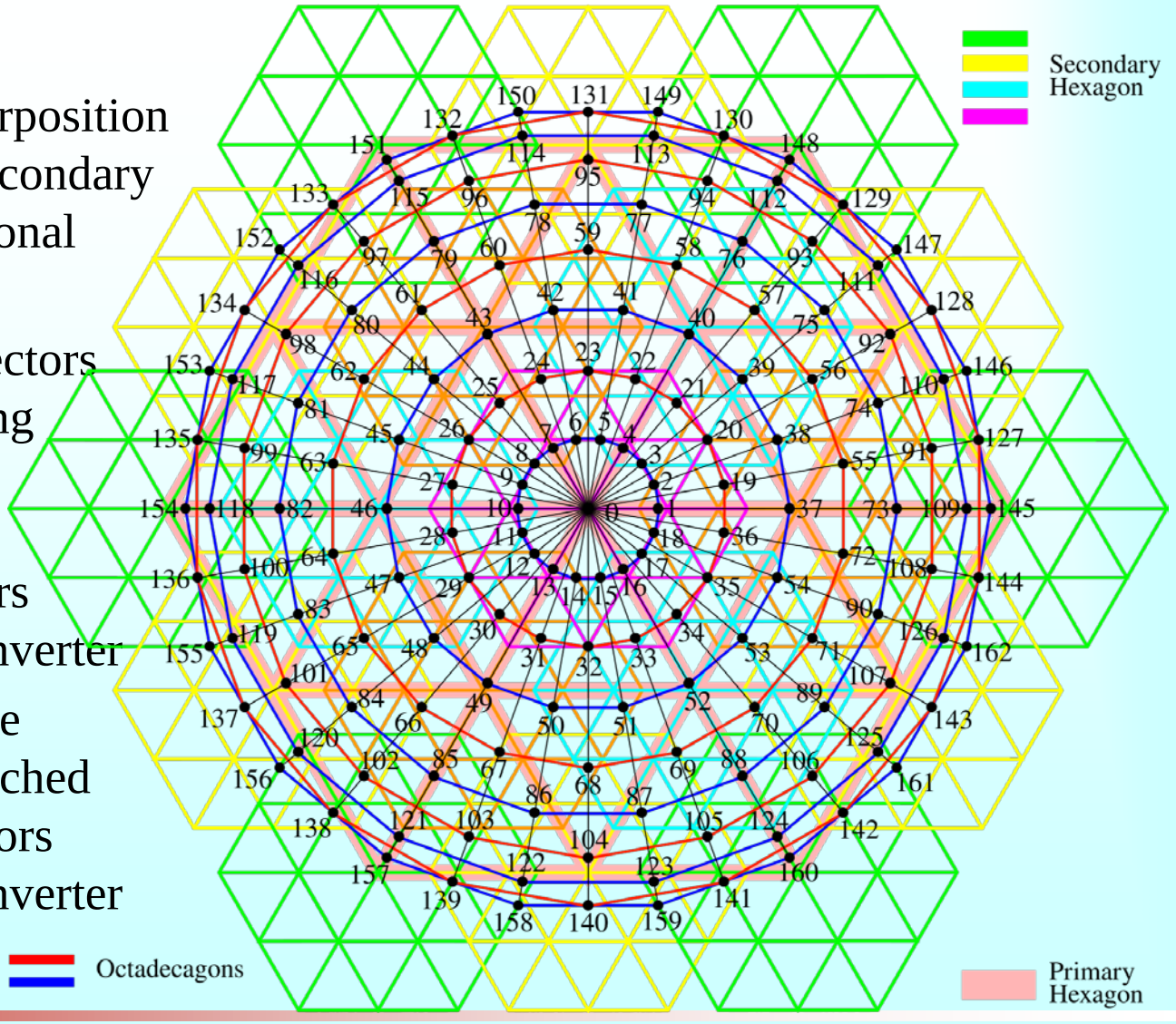


Fig: VSVS obtained by superposition of primary and secondary hexagons

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Pseudo vectors:
  - Many k-value sets are obtained because of formation of new pseudo vectors

Octadecagonal Vectors	k-values $[k_0, k_1, k_2]$
1, 4, 7, 10, 13, 16, 38, 39, 41, 42, 44, 45, 47, 48, 50, 51, 53, 54, 73, 76, 79, 82, 85, 88	[0.759, 0, 0.241]
2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	[0.653, 0, 0.347]
19, 21, 22, 24, 25, 27, 28, 30, 31, 33, 34, 36, 55, 57, 58, 60, 61, 63, 64, 66, 67, 69, 70, 72	[0.653, 0.106, 0.241]
20, 23, 26, 29, 32, 35	[1, 0, 0]
37, 40, 43, 46, 49, 52	[0.894, 0, 0.106]
56, 59, 62, 65, 68, 71, 91, 93, 94, 96, 97, 99, 100, 102, 103, 105, 106, 108, 128, 131, 134, 137, 140, 143	[0.518, 0.241, 0.241]
74, 75, 77, 78, 80, 81, 83, 84, 86, 87, 89, 90, 110, 111, 113, 114, 116, 117, 119, 120, 122, 123, 125, 126	[0.759, 0.106, 0.135]
92, 95, 98, 101, 104, 107	[0.788, 0.106, 0.106]
127, 129, 130, 132, 133, 135, 136, 138, 139, 141, 142, 144,	[0.73, 0.135, 0.135]
145, 148, 151, 154, 157, 160	[0.788, 0, 0.212]
109, 112, 115, 118, 121, 124, 146, 147, 149, 150, 152, 153, 155, 156, 158, 159, 161, 162	[0.518, 0, 0.482]

Table: k-value sets for secondary inverter vector switching

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Superposition requires 2 octadecagons
  - Two 2-level hexagons generates one octadecagon
  - Two sets of two 2-level hexagons can generate two octadecagons
  - The 2-level hexagons get superposed to form 3-level hexagons
  - Hence two 3-level hexagons can generate a 9-concentric octadecagonal structure
    - Primary 3-level hexagon has vector length of Vdc
    - Secondary 3-level hexagon has vector length of 0.379Vdc

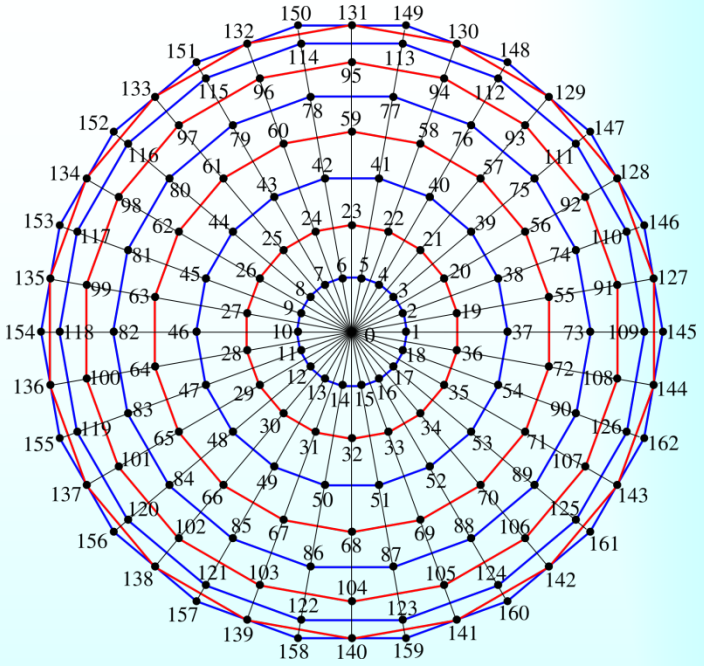


Fig: Superposition of two 2-level octadecagons

- The inverter topology is realized by cascading a 3-level Flying Capacitor (FC) inverter with an H-bridge (CHB)

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Inverter Topology
  - Single DC source
  - Two 3-level inverters:
    - FC inverter
    - CHB inverter
  - FC capacitor at Vdc/2
  - CHB capacitor at 0.1895Vdc
  - FC inverter generates 3-level space vector structure of vector length Vdc
  - CHB inverter generates 3-level space vector structure of vector length 0.379Vdc
  - Sx1 and $\overline{Sx1}$ are complementary; x = a, b, c indicates phase
  - 8 switches and 2 capacitors per phase

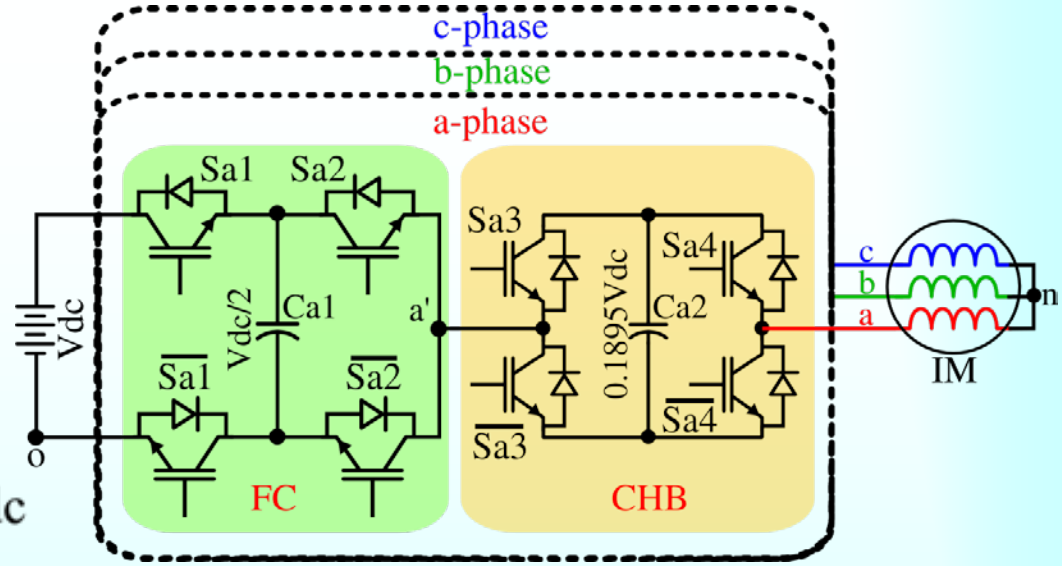


Fig: Inverter Topology

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- PWM Scheme:
  - Timing calculation involves finding vectors $[V_0, V_1, V_2]$ and timings $[T_0, T_1, T_2]$ satisfying the volt-second balance:
    - $V_{ref} T_s = V_0 T_0 + V_1 T_1 + V_2 T_2$
    - $T_s = T_0 + T_1 + T_2$
    - Similar to steps in [1] [2]
  - PWM scheme
    - $V_1 \rightarrow V_0 \rightarrow V_2$ sequence
    - Reduced switchings
    - Quasi-square output from FC inverter
  - Example

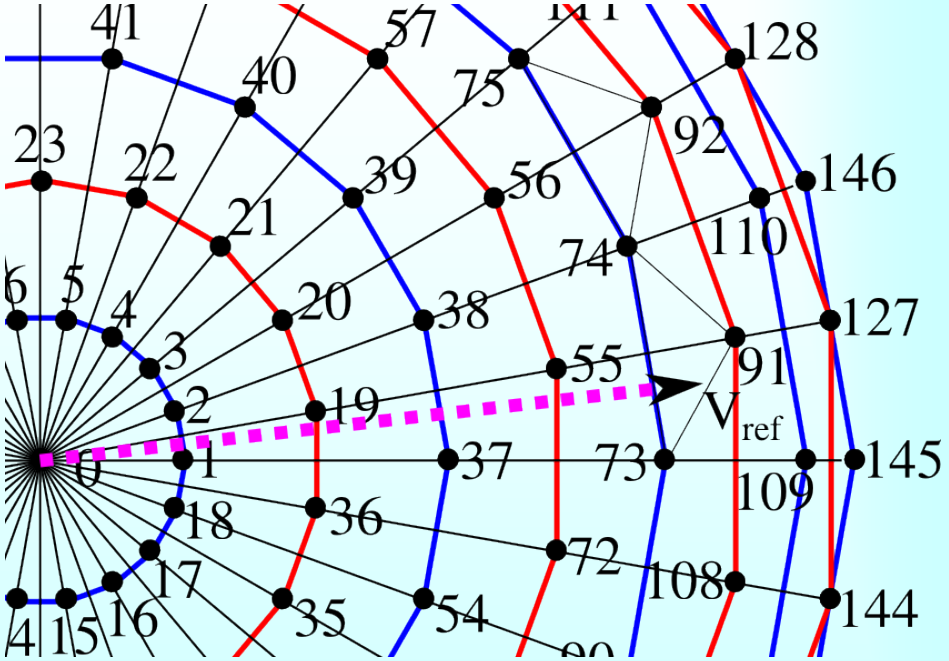


Fig: PWM Switching sequence

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

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    - Similar to steps in [1] [2]
  - PWM scheme
    - $V_1 \rightarrow V_0 \rightarrow V_2$ sequence
    - Reduced switchings
    - Quasi-square output from FC inverter
  - Example
    - $73 \rightarrow 91 \rightarrow 74$

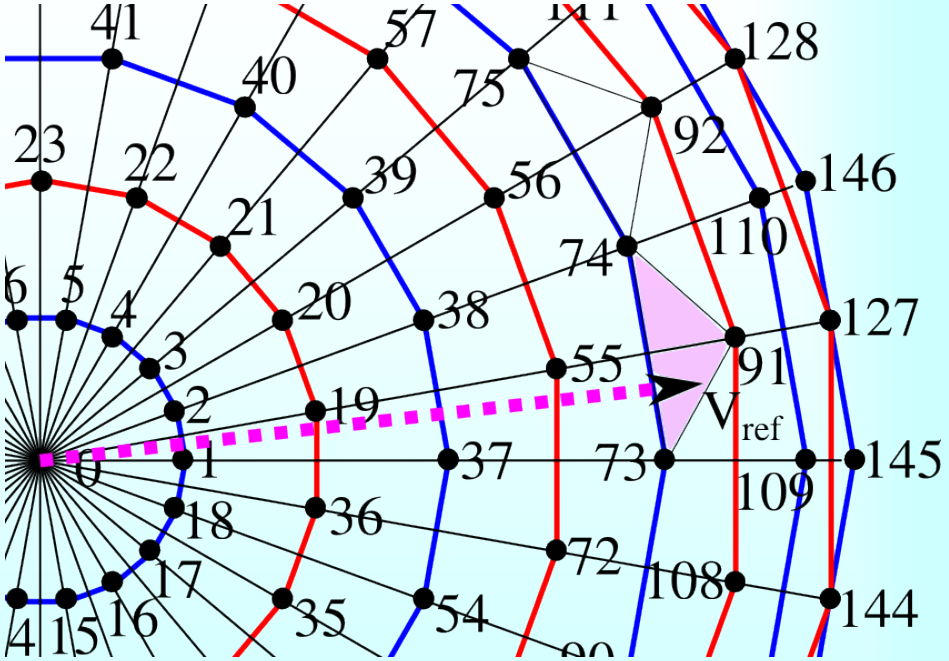

Fig: PWM Switching sequence

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

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    - Similar to steps in [1] [2]
  - PWM scheme
    - $V_1 \rightarrow V_0 \rightarrow V_2$ sequence
    - Reduced switchings
    - Quasi-square output from FC inverter
  - Example
    - $73 \rightarrow 91 \rightarrow 74 \rightarrow 74 \rightarrow 92 \rightarrow 75 \rightarrow$

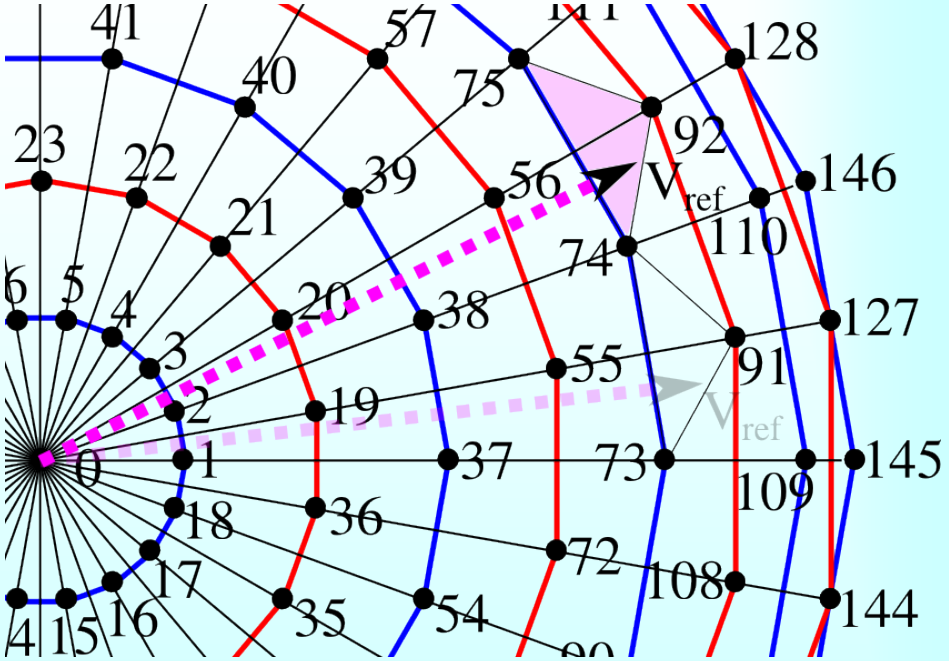


Fig: PWM Switching sequence

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Capacitor Balancing
  - FC capacitor balancing is same as explained before
  - CHB capacitors have to be balanced individually
  - A modification is brought in the capacitor balancing scheme:
  - Consider octadecagonal vector 18
  - CHB inverter vectors used are:
    - $[V_0, V_1, V_2] = [100, 000, 101]$, with $[k_0, k_1, k_2] = [0.653, 0, 0.347]$.
    - Since $V_1 = 000$, is the zero vector, the space vector redundancies could also be used and therefore $V_1 = 111$ can also be used
    - The possibilities for capacitor balancing are:
      - 1) A-phase capacitor voltage could be modified by modifying k_0 & k_1 values, keeping k_2 constant
      - 2) B-phase capacitor voltage could be modified by modifying k_1 & k_2 values, keeping k_0 constant (using $V_1 = 111$)
      - 3) C-phase capacitor voltage could be modified by modifying k_0 & k_2 values, keeping k_1 constant.

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Capacitor Balancing
  - All such possibilities as considered and LUTs are created. LUTs contain:
    - k-values to be modified
    - Capacitor that could be controlled
    - Control sense
  - If an octadecagonal vector can control multiple capacitors, choice could be made according to:
    - Maximum deviated capacitor
    - Phase with maximum current
  - In this work, phase with maximum current is chosen
    - Allows fast correction of capacitor voltages
  - A “phase selection logic” does this job

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Capacitor Balancing
  - Capacitor voltage errors are obtained and checked whether they are within a band
  - Polarity of error, direction of current and control sense are used to generate polarity of Δk
  - LUT gives the k values, phases and the control sense
  - Phase selection logic selects the capacitor to be controlled

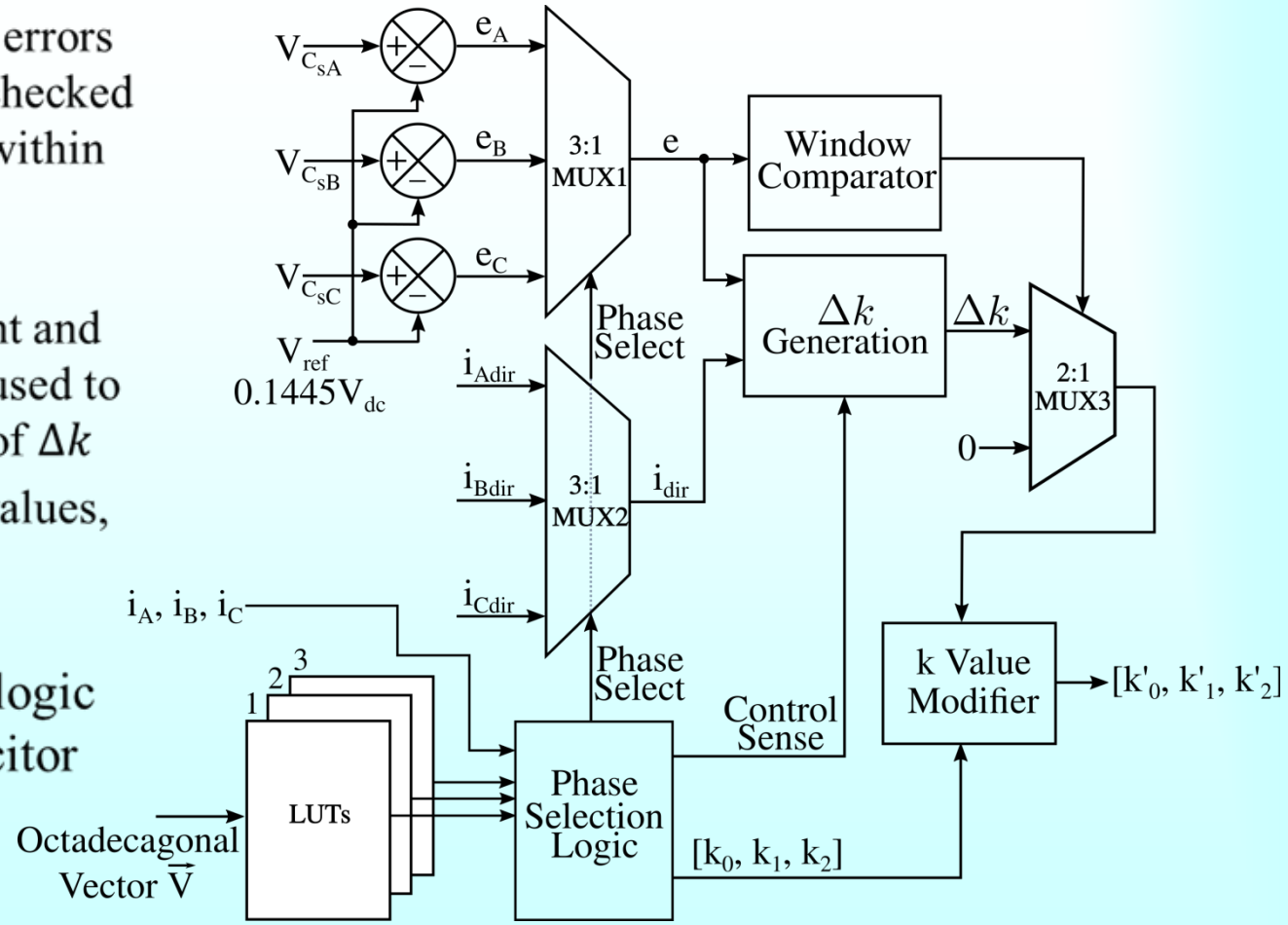


Fig: Secondary inverter DC-link controller

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Implementation

  - Rotor filed oriented vector control
  - Open loop V/f control
  - A shaft encoder is used to get rotor position

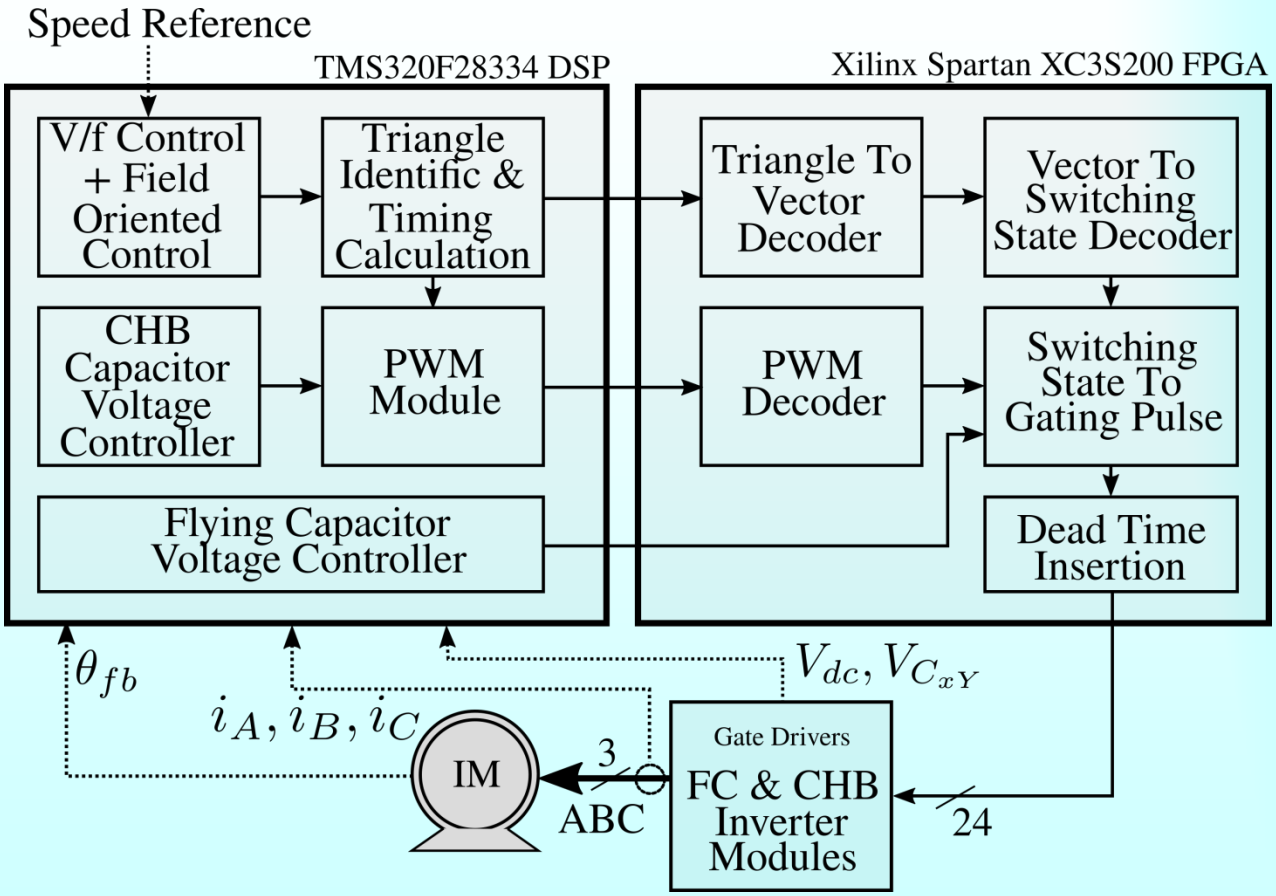


Fig: Implementation block diagram for multilevel octadecagonal IMD

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Implementation
  - Rotor filed oriented vector control lock diagram

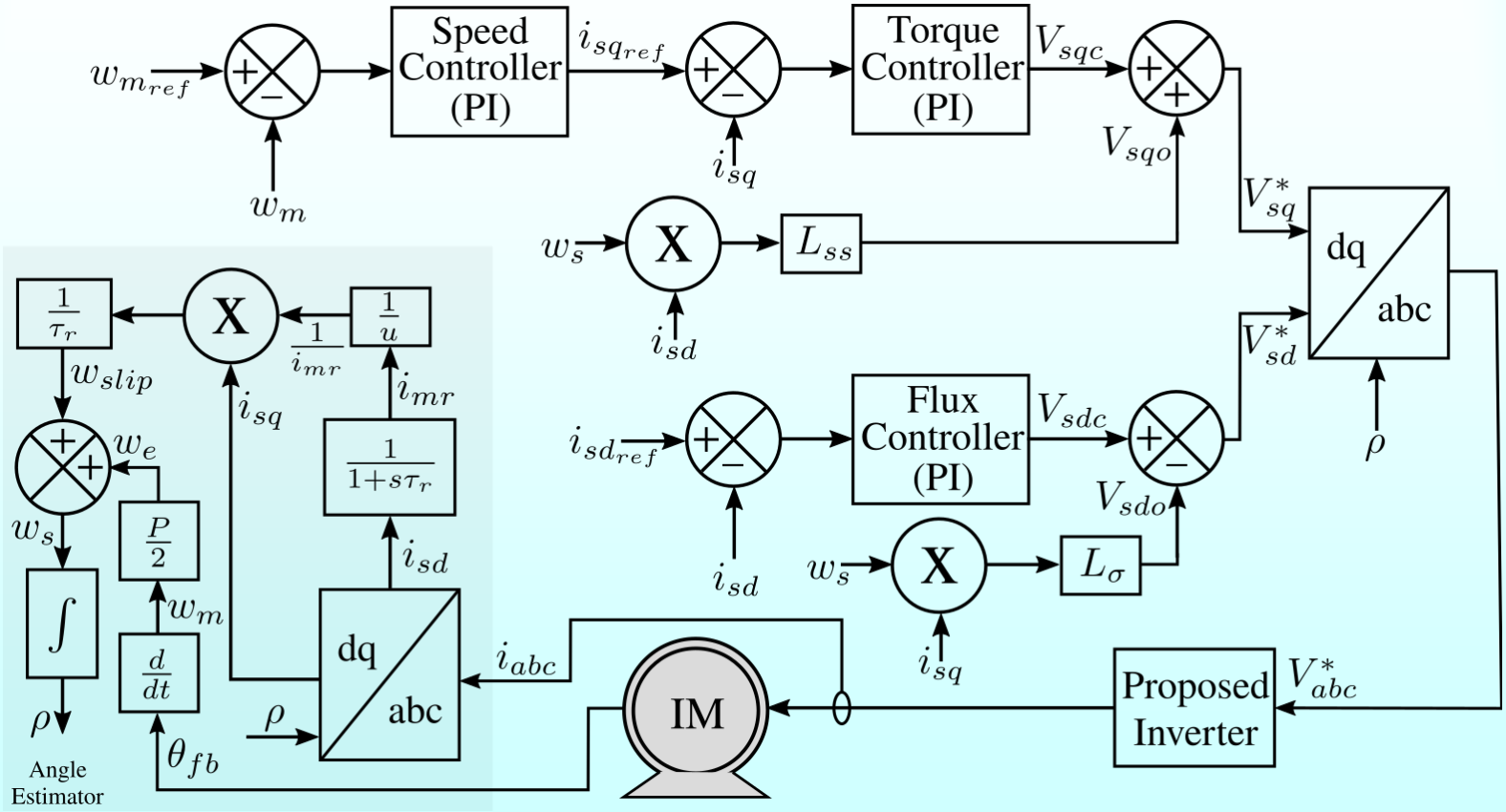
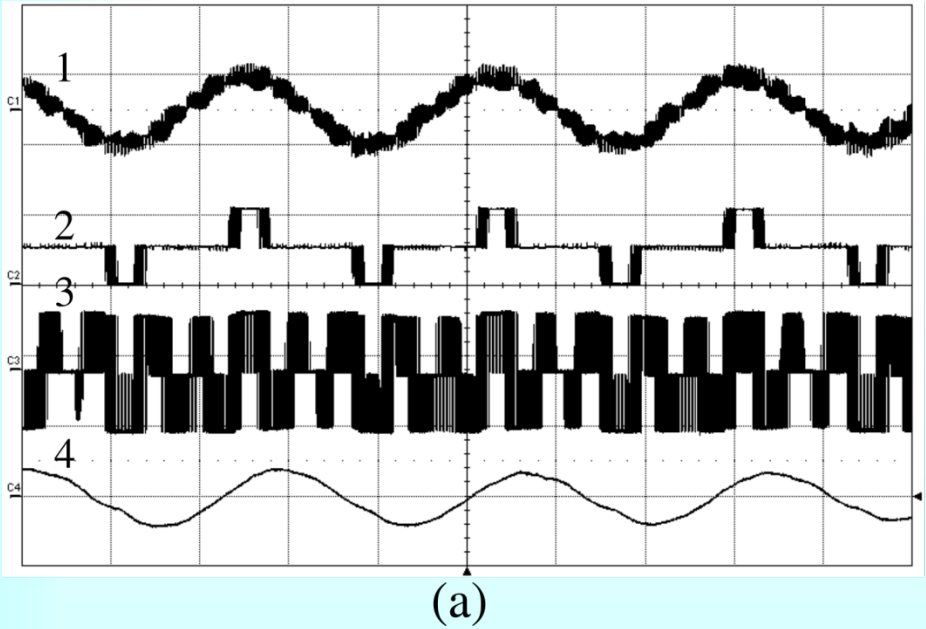


Fig: FOC implementation block diagram

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Steady state results:

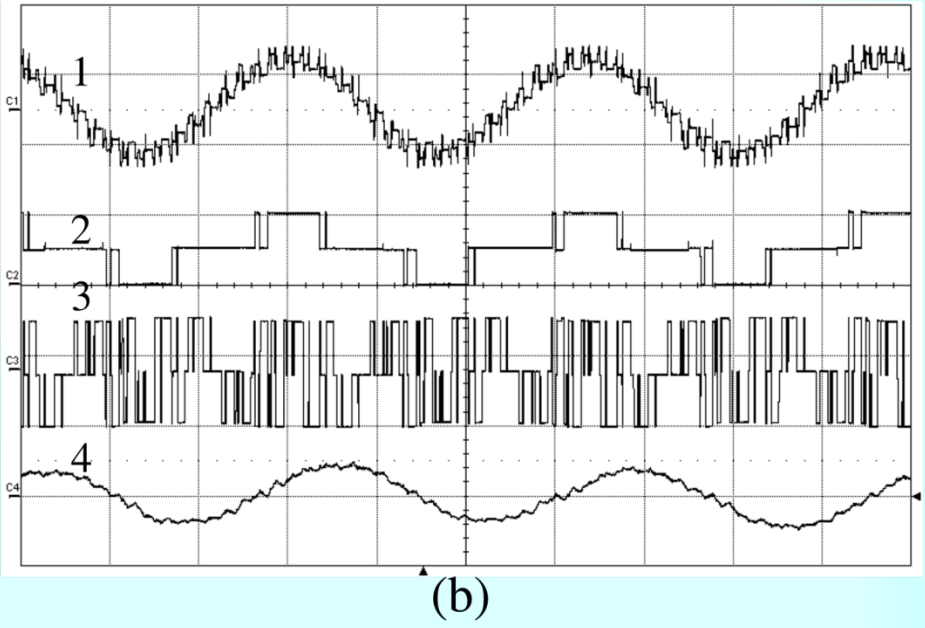
18Hz (M=0.36)Operation – 72spc – PWM1



(a)

Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 50V/div, (4) Current, 1A/div; X-axis: 20mS/div

30Hz (M=0.6) Operation – 36spc – PWM1



(b)

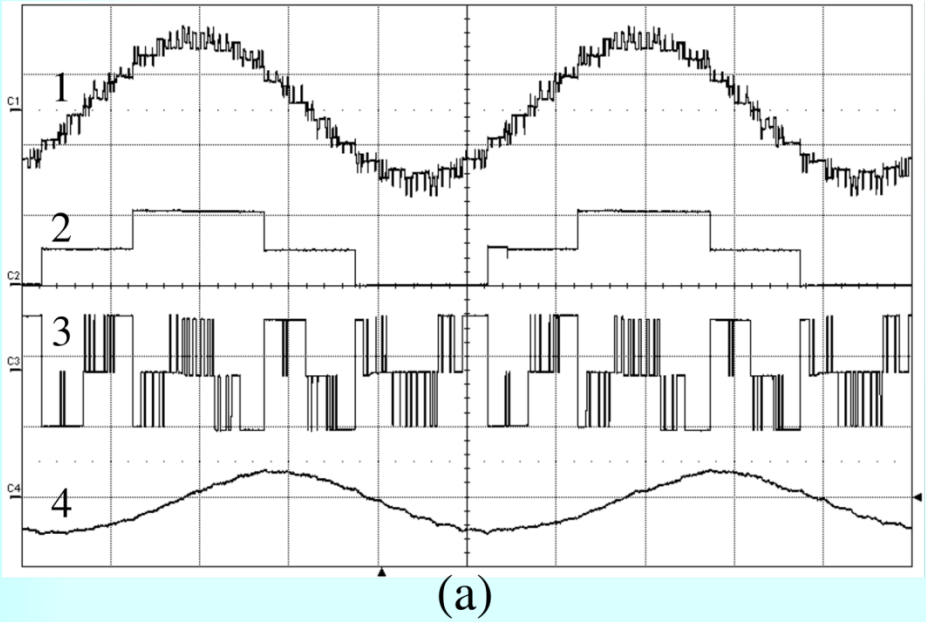
Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 50V/div, (4) Current, 1A/div; X-axis: 10mS/div

- Higher frequency switching happens in secondary inverter at low voltage

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Steady state results:

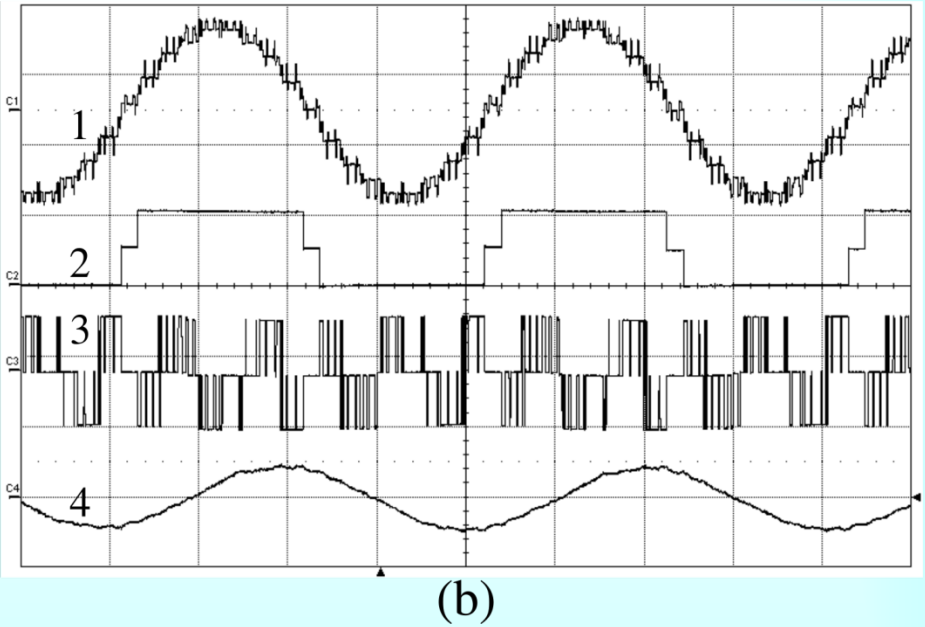
40Hz (M=0.8) Operation – 18spc – PWM2



(a)

Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 50V/div, (4) Current, 1A/div; X-axis: 5mS/div

49Hz (M=0.98)Operation – 18spc – PWM2



(b)

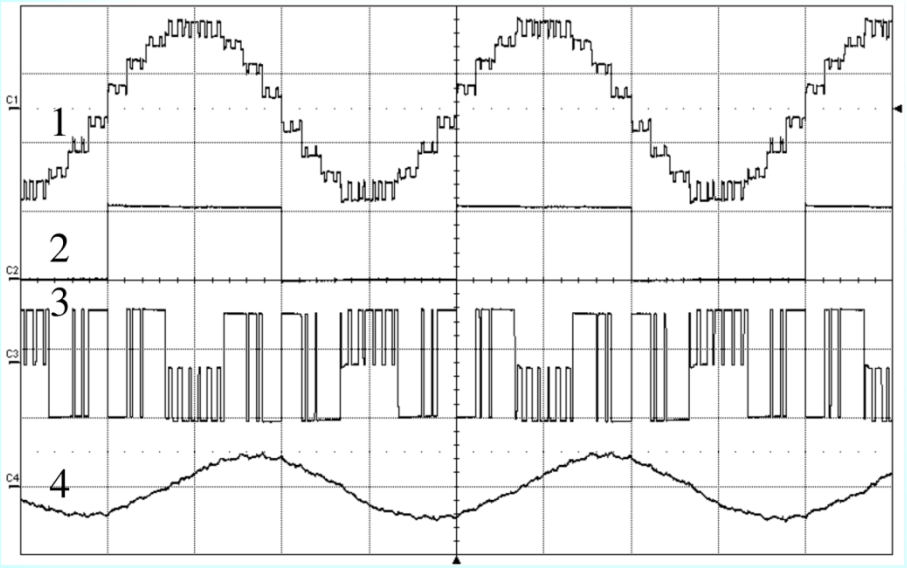
Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 50V/div, (4) Current, 1A/div; X-axis: 5mS/div

- Primary inverter switches in quasi-square mode, switching losses are reduced

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

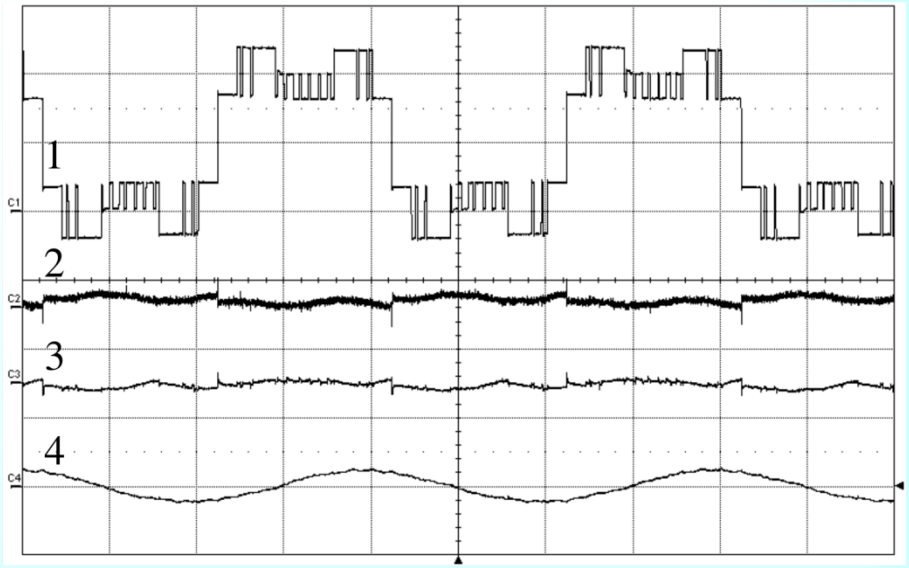
- Steady state results:

50Hz (M=1), 18 step mode – 18spc – PWM2



(a)

Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 50V/div, (4) Current, 1A/div; X-axis: 5mS/div



(b)

Fig: Vdc=200V (1) Pole voltage, 100V/div, (2) FC inverter capacitor ripple, 1V/div, (3) CHB inverter capacitor ripple, 5V/div, (4) Current, 2A/div; X-axis: 5mS/div

- Primary inverter switches in square wave mode

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Steady state results: FFT at 50Hz (M=1)
- FC inverter generates square wave output
- FFT of FC inverter shows $5^{th}, 7^{th}, 11^{th}, 13^{th}$ ... order harmonics in the pole voltage
- CHB generates $5^{th}, 7^{th}, 11^{th}, 13^{th}$ ... harmonics of same amplitude
- FFT of phase voltage shows the absence of $5^{th}, 7^{th}, 11^{th}, 13^{th}$ ... harmonics
- CHB generates zero fundamental voltage output
- CHB functions as a harmonic filter

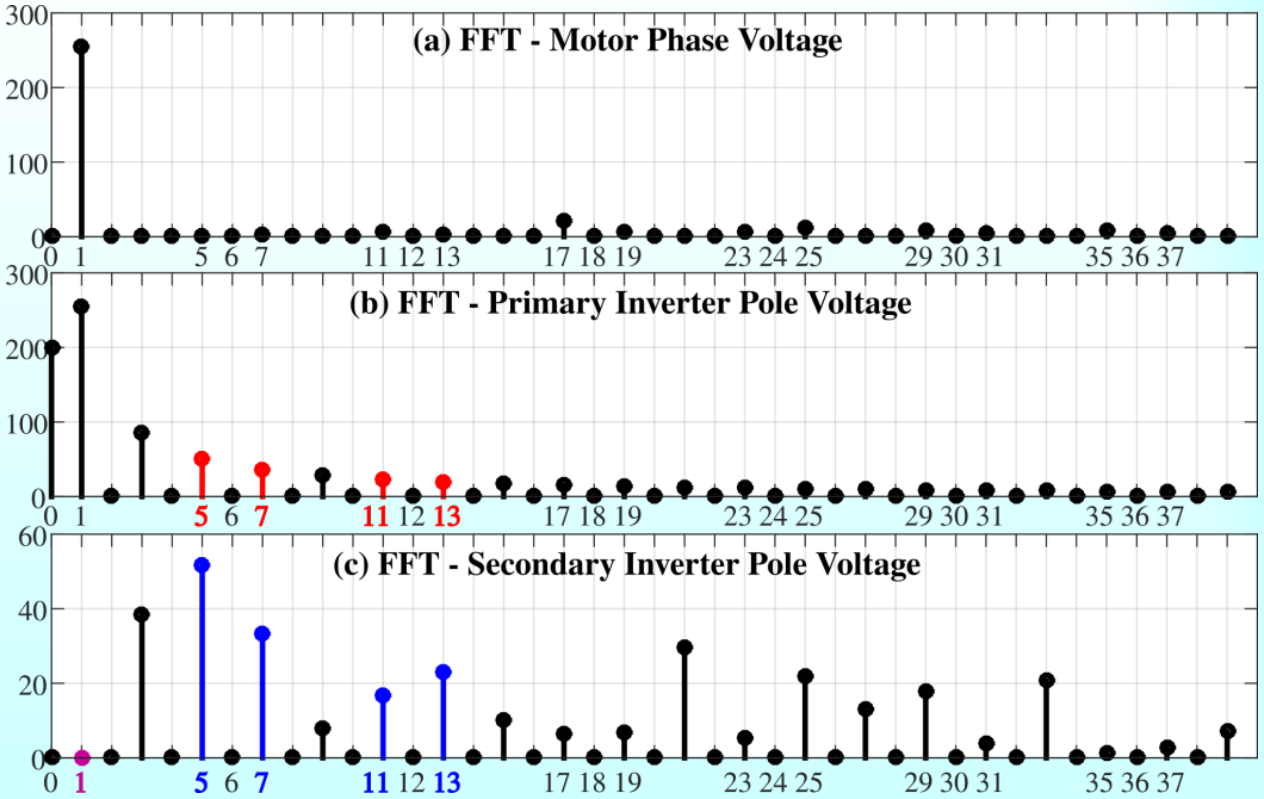


Fig: Harmonic spectrum of inverter voltages for 18 step operation

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Transient operations:

Startup from Vdc = 0 to 200V

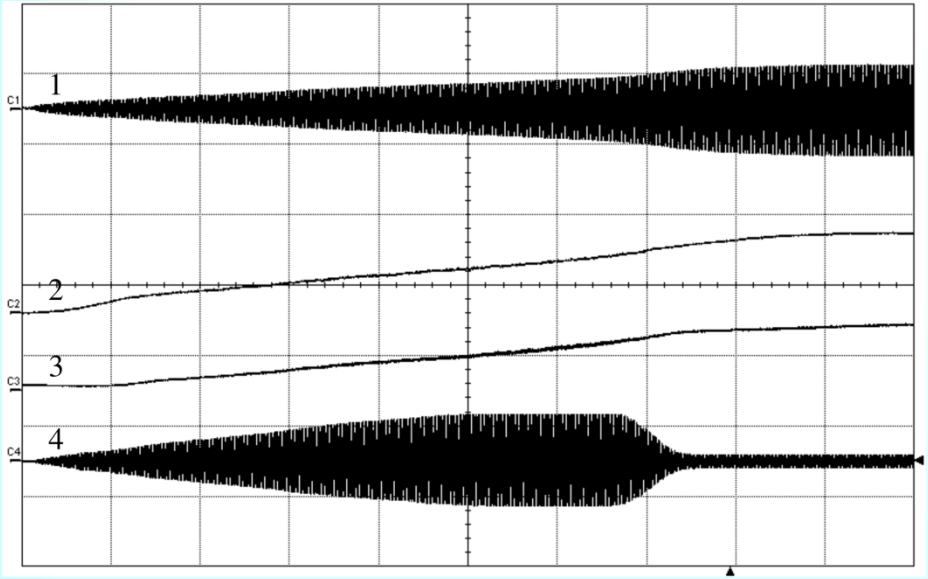


Fig: (1) Phase voltage, 200V/div, (2) FC inverter capacitor voltage, 100V/div, (3) CHB inverter capacitor voltage, 50V/div, (4) Current, 5A/div; X-axis: 1s/div

Speed Reversal using FOC

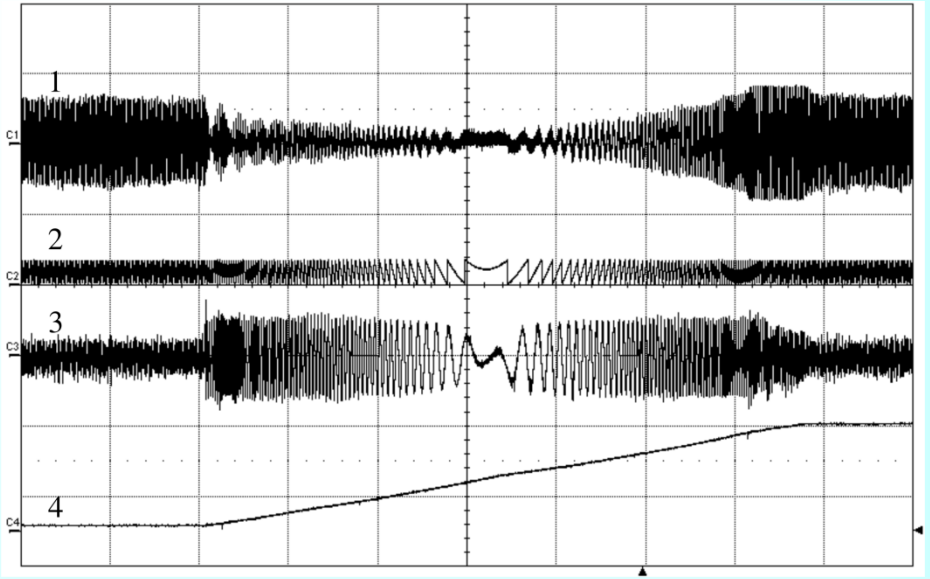


Fig: (1) Phase voltage, 200V/div, (2) Rotor flux angle, (3) Phase current, 5A/div, (4) Rotor speed, -47Hz to +47Hz; X-axis: 1s/div

- Capacitor voltages settle and stay at nominal values at end of startup

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- Transient operations:

Speed Reversal using FOC

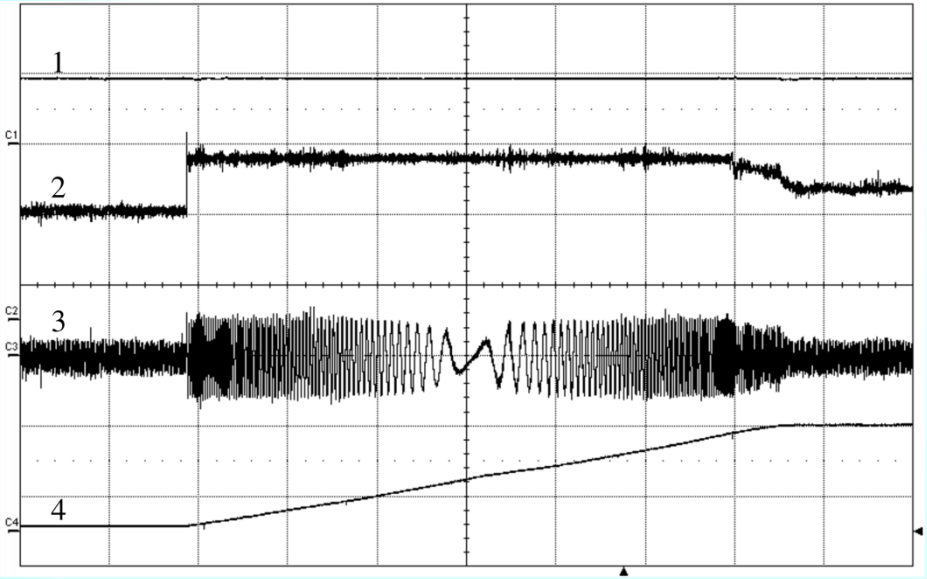


Fig: (1) Rotor mag current, 0.75A, (2) Isq, 1.5A step, (3) Phase current, 5A/div, (4) Rotor speed, -47Hz to +47Hz; X-axis: 1s/div

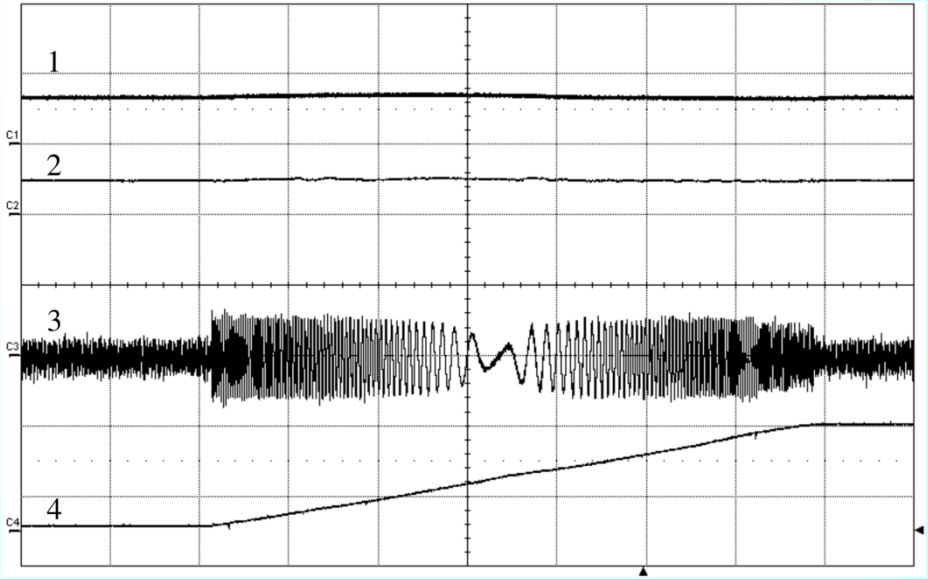


Fig: (1) FC inverter capacitor, 200V/div(2) CHB inverter capacitor, 200V/div, (3) Phase current, 5A/div, (4) Rotor speed, -47Hz to +47Hz; X-axis: 1s/div

- Capacitor voltages stay at nominal values

Multilevel Oct-VSVS Using a Single DC Source for a Star Connected IMD

- An IMD scheme with following advantages are proposed:
  - Single DC source requirement
    - Reduces system cost
    - Permits easy four-quadrant operation
  - 9-concentric multilevel octadecagonal space vector structure
    - Low order harmonics of orders: $5^{th}, 7^{th}, 11^{th}$ & 13^{th} are eliminated from phase voltage and hence current
    - Absence of low order torque ripple
    - Low THD phase voltage due to multilevel operation
    - Low dv/dt output
    - Linear modulation range extended till 49.5Hz (M=0.99)
  - Capacitors in the circuit are inherently balanced with the PWM operation
  - Controlled switching losses
    - Quasi-square waveform switching from FC inverter
    - Low voltage switching for CHB inverter

Conclusion

- IMD schemes with six-concentric-dodecagonal & nine-concentric octadecagonal voltage space vector structures are proposed
- Following are the features
  - Single DC source requirement
    - Reduces system cost & permits easy four-quadrant operation
  - Low order harmonics are eliminated
    - Low order torque ripple is avoided
    - Requirement of filters are avoided or relaxed
  - Multilevel operation brings:
    - Low THD phase voltage due to multilevel operation
    - Low dv/dt output
  - A secondary inverter operating at low voltage functions as a harmonic filter
  - Quasi-square waveform switching from primary inverter controls losses

Publications

- M. Boby, S. Pramanick, R. S. Kaarthik, S. A. Rahul, K. Gopakumar, and L. Umanand, **Multilevel dodecagonal voltage space vector structure generation for open-end winding IM using a single DC source**, IEEE Trans. Ind. Electron., vol. 63, no. 5, pp. 27572765, May 2016.
- M. Boby, S. Pramanick, R. S. Kaarthik, A. R. S, K. Gopakumar, and L. Umanand, **Fifth- and seventh-order harmonic elimination with multilevel dodecagonal voltage space vector structure for IM drive using a single DC source for the full speed range**, IEEE Trans. Power Electron., vol. 32, no. 1, pp. 6068, Jan 2017.
- M. Boby, Arun Rahul S, K. Gopakumar, L. Umanand, Frede Blaabjerg, and Subhashish Bhattacharya, **A Low Order Harmonic Elimination Scheme For Induction Motor Drives Using a Multilevel Octadecagonal Space Vector Structure With a Single DC Source**, IEEE Trans. Power Electron., accepted for publication.
- M. Boby, S. Pramanick, S. A. Rahul, K. Gopakumar, and L. Umanand, **A multilevel inverter fed IM drive with dodecagonal voltage space vector structure using a single DC source with linear modulation range near to base speed**, 18th EPE'16 ECCE Europe, Sept 2016, pp. 110.
- Mathews Boby, Sumit Pramanick, Arun Rahul S, K. Gopakumar, and L. Umanand, **A multilevel nine concentric octadecagonal space vector structure for induction motor drives using a single DC source**, IEEE-PEDES, 2016, Trivandrum, India.

THANK YOU!