

Multilevel Dodecagonal and Octadecagonal Voltage Space Vector Structures With a Single DC Supply Using Basic Inverter Cells

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Outline



Introduction

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- 2-level 3-phase voltage source inverter (VSI)
- Hexagonal voltage space vector structure (Hex-VSVS)
- Multilevel VSI
- Harmonics
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 - Features & advantages
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 - Features & advantages
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- Motivation for research

Outline...



- Six-Concentric-Dodecagonal Voltage Space Vector Structure for Open-End Winding IMDs Using a Single DC Source
 - Dod-VSVS using single DC source
 - Topology
 - PWM scheme
 - Capacitor balancing & design
 - Implementation
 - Results
- Six-Concentric-Dodecagonal Voltage Space Vector Structure for Star Connected IMDs Using a Single DC Source
 - Topology
 - PWM scheme
 - Capacitor balancing & design
 - Implementation
 - Results

Outline...



- Nine-Concentric-Octadecagonal Voltage Space Vector Structure for IMDs Using a Single DC Source
 - Oct-VSVS using single DC source
 - Two-level
 - Extension to multilevel
 - Topology
 - PWM scheme
 - Capacitor balancing & design
 - Implementation
 - Results
- Conclusion

Induction Motor Drive Systems



- Induction motors are widely used in industrial applications, reasons being
 - Simple construction / low cost
 - Rugged / maintenance free / long life
- Variable speed induction motor drive (IMD) system:



Fig: IMD System

- Focus is on the power converter, to make the system
 - Lower cost, smaller size, lower weight
 - Reliable, efficient

2-Level 3-Phase Voltage Source Inverter



Power circuit topology:

• 6 switches / 3 half-bridges

•
$$V_{XO} = \left[-\frac{V_{dc}}{2}, +\frac{V_{dc}}{2}\right]; X = A, B, C$$

- State '1':
 - Top switch ON
 - Bottom switch OFF
- $2^3 = 8$ switching states in total



 Table 1: 2-level Inverter Switching States

State	V _{AO}	V _{BO}	V _{co}
100	$+\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$
110	$+\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$
010	$-\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$
011	$-\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$
001	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$
101	$+\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$
000	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$
111	$+\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$	$+\frac{V_{dc}}{2}$

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Hexagonal Voltage Space Vector Structure



V1(100)

 α -axis a-axis

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V2(110)

76(101)

VSVS from 2-level VSI:

• Obtained by plotting V_A , V_B , V_C in a 2D plane ($\alpha\beta$ plane) using:

$$\begin{bmatrix} V_{\alpha} \\ V_{\beta} \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{A} \\ V_{B} \\ V_{C} \end{bmatrix}$$

 Reference vector inside the hexagon can be synthesized as:

$$V_{ref}T_{s} = V_{0}T_{0} + V_{6}T_{1} + V_{5}T_{2}$$

$$T_{s} = T_{0} + T_{1} + T_{2}$$

• Radius of the in-circle: $\frac{\sqrt{3}}{2}V_{dc} = 0.866V_{dc}$





b-axis

2.800 Vdc

60°

V3(010)

 β -axis

V0(000)

V7(111)

Vrèf

- Peak phase fundamental output
 - Linear modulation range: $\frac{2}{3} * 0.866V_{dc} = 0.577V_{dc}$
 - 6 step mode (M=1): 0.637*V*_{dc}

Multilevel VSI



Commonly used multilevel VSI topologies & VSVS:



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Hexagonal Voltage Space Vector Structure...



- In six-step mode / M=1:
 - Peak phase fundamental output is: $V_1 = 0.637 V_{dc}$
 - Harmonic content of V_{XN} :

•
$$V_n = \frac{1}{n} V_1; n = 5,7,11,13...$$

- Creates harmonic currents
- Problems with harmonics:
 - Creates torque pulsations
 - 6th, 12th, ... order torque ripple
 - Affects closed loop current control
 - Requires filtering
 - Power loss due to harmonic currents



Fig: Waveforms during extreme overmodulation



Harmonic Elimination & Suppression

Harmonic current suppression:

- Use high frequency PWM
 - Higher switching losses
 - EMI issues
 - Good only in linear modulation range
- Selective Harmonic Elimination PWM
 - Limited modulation range
 - Requires offline computations
- Use passive filters
 - Efficiency degradation
 - Bulky, good for high frequency harmonics
 - Unsuitable for variable frequency operation
 - DC-link utilization is poor
- Voltage space vector structures with more number of sides (12, 18, ...)

Dodecagonal VSVS

- Dodecagonal Structure:
 - Boundary is a 12 sided polygon
 - 12 active vectors separated at 30^o angle
 - Vectors of magnitude V_d
- Projection of vectors on α-axis and scaling by 2/3 gives A-phase voltage





vector structure

$$V_{0} = 0$$

$$V_{1} = 2/3V_{d}cos(60^{o})$$

$$V_{2} = 2/3V_{d}cos(30^{o})$$

$$V_{3} = 2/3V_{d}$$

Dodecagonal VSVS - Harmonics



Harmonics spectrum:



Fig: Harmonic spectrum of phase voltage from dodecagonal structure

- $6n \pm 1$; n = odd order harmonics are absent
 - 5th, 7th, 17th, 19th ... harmonics are eliminated form the phase voltage
- $12n \pm 1$; n = 1, 2, 3 ... order harmonics are present
- Peak phase fundamental output is:
 - 50Hz operation, 12-step mode, M = 1: $V_{ppf-dod} = 0.659V_d$

Linear modulation range is
$$V_{\text{lin}} = \frac{2}{3}V_{\text{d}}\cos(15^{\circ}) = 0.644V_{\text{d}}$$

Dodecagonal VSVS - Advantages



- Complete elimination of $6n \pm 1$; n = odd order harmonics from the phase voltage over entire modulation range:
 - Absence of 6th order torque ripple, smooth torque generation
 - Output filtering requirements could be avoided or relaxed
 - Easy current control loop design
- Linear modulation range is extended till 97.7% of base speed compared to 90.58% in a hexagonal structure
 - Hexagonal structure: $\frac{0.577V_{dc}}{0.637V_{dc}} = 90.58\% \equiv 45.3Hz \text{ (M=0.906)}$
 - Dodecagonal structure: $\frac{0.644V_d}{0.659V_d} = 97.7\% \equiv 48.86Hz$ (M=0.977) (For base speed of 50Hz)

Octadecagonal VSVS

- Octadecagonal Structure:
 - Boundary is an 18 sided polygon
 - 18 active vectors separated at 20^o angle
 - Vectors of magnitude Voct
- Projection of vectors on α-axis and scaling by 2/3 gives A-phase voltage







Octadecagonal VSVS - Harmonics



Harmonics spectrum:



- $6n \pm 1$; $n = 1, 2, 4, 5, \dots$ order harmonics are absent
 - 5th, 7th, 11th, 13th ... harmonics are eliminated form the phase voltage
- $18n \pm 1$; n = 1, 2, 3 ... order harmonics are present
- Peak phase fundamental output is:
 - 50Hz / 18 step operation / M=1: $V_{ppf-oct} = 0.663V_{oct}$
 - Linear modulation range is $V_{\text{lin}} = \frac{2}{3}V_{\text{oct}}\cos(10^{\circ}) = 0.656V_{oct}$

Octadecagonal VSVS - Advantages



- Complete elimination of $6n \pm 1$; n = 1, 2, 4, 5, ... order harmonics from the phase voltage over entire modulation range:
 - Absence of 6th, 12th order torque ripple, smooth torque generation
 - Output filtering requirements could be avoided or relaxed
 - Easy current control loop design
- Linear modulation range is extended till 99% of base speed
 - Hexagonal structure: $\frac{0.577V_{dc}}{0.637V_{dc}} = 90.58\% \equiv 45.3Hz \text{ (M=0.906)}$
 - Dodecagonal structure: $\frac{0.644V_d}{0.659V_d} = 97.7\% \equiv 48.86Hz (M=0.977)$
 - Octadecagonal structure: $\frac{0.656V_{oct}}{0.663V_{oct}} = 99\% \equiv 49.5Hz (M=0.99)$ (For base speed of 50Hz)

Dodecagonal VSVS – Prior Works



 2-level dodecagonal space vector structure for open-end winding IM



[1] K. Mohapatra, K. Gopakumar, V. Somasekhar, and L. Umanand, "A harmonic elimination and suppression scheme for an open-end winding induction motor drive," IEEE Trans. Ind. Electron., vol. 50, pp. 1187–1198, Dec 2003.

Dodecagonal VSVS – Prior Works



Multilevel dodecagonal space vector structure for open-end winding IM



Fig: Topology for multilevel Dod-VSVS

- Requires 2 DC sources delivering active power
- DC links: $V_{dc} \& 0.366 V_{dc}$



- 6 concentric dodecagons giving a multilevel structure
- [2] A. Das and K. Gopakumar, "A voltage space vector diagram formed by six concentric dodecagons for induction motor drives," IEEE Trans. Power Electron., vol. 25, pp. 1480–1487, June 2010.

Dodecagonal VSVS – Prior Works

- HICATU LA DELLA DE
- 2-level dodecagonal space vector structure for open-end winding IM using single DC source



Fig: Topology for 2-level Dod-VSVS using single DC source

- Requires only one DC source delivering active power
- DC links: V_{dc} & 0.289 V_{dc} (capacitor fed)
- Only 2-level operation
- [3] S. Pramanick, N. Azeez, R. Sudharshan Kaarthik, K. Gopakumar, and C. Cecati, "Low-order harmonic suppression for open-end winding im with dodecagonal space vector using a single dc-link supply," IEEE Trans. Ind. Electron., vol. 62, pp. 5340–5347, Sept 2015.





- 2-Level octadecagonal SVS first proposed in:
 - [4] S. Lakshminarayanan, G. Mondal, P. Tekwani, K. Mohapatra, and K. Gopakumar, "Twelve-sided polygonal voltage space vector based multilevel inverter for an induction motor drive with common-mode voltage elimination," IEEE Trans. Ind. Electron., vol. 54, DOI 10.1109/TIE.2007.899929, no. 5, pp. 2761–2768, Oct. 2007.
 - Requires **3 DC sources** delivering active power
 - Only 2-level operation
- A 3-concentric multilevel octadecagonal SVS proposed in:
 - [5] K. Mathew, K. Gopakumar, J. Mathew, N. A. Azeez, A. Dey, and L. Umanand, "Medium voltage drive for induction motors using multilevel octadecagonal voltage space vectors," IEEE Transactions on Power Electronics, vol. 28, pp. 3573–3580, July 2013
 - Requires 4 DC source

Motivation For Research



- Is it possible to generate multilevel dodecagonal & octadecagonal voltage space vector structures using a single DC source?
 - Single DC source:
 - Permits easy 4-quadrant operation
 - Reduces cost and size of the system
 - Multilevel operation brings:
 - Lower switching frequency operation
 - Improved voltage and current THD
 - Lower EMI concerns
 - Reduced filtering requirements
 - Dodecagonal & Octadecagonal structure brings:
 - Absence of low order harmonics in phase voltage
 - Improved linear modulation range



- A drive scheme for an open-end winding IM to generate a multilevel Dod-VSVS using a single DC source is proposed.
 - Obtaining a 2-level Dod-VSVS[1]
 - Obtaining a 2-level Dod-VSVS using a single DC source[2]
 - Obtaining a multilevel Dod-VSVS[3] using a single DC source
 - Power circuit topology
 - Dod-VSVS features
 - PWM scheme
 - Capacitor balancing
 - Implementation
 - Results

- Obtaining a 2L Dod-VSVS[1]:
 - (a) Method 1
 - INV2 DC-link is 0.366V_{dc}
 - Resultant vector is of $1.225V_{dc}$
 - INV2 sources power
 - (b) Method 2
 - INV2 DC-link is $0.268V_{dc}$
 - Resultant vector is of 0.896V_{dc}
 - INV2 sinks power
- If we make fundamental voltage output of resultant Dod-VSVS same as that of INV1, average power delivered by INV2 equals zero. $K_{d} = 0.896 Vec$ $V_{dc} = 0.896 Vec$ $V_{dc} = 0.268 Vec$ (b) Method 2S'(b) Method 2S'(b) Method 2S'(b) Method 2S'







- Obtaining a 2-level Dod-VSVS using a single DC source[3]:
 - Fundamental output from resultant dodecagon = output from hexagon (INV1)
 - $0.659V_d = 0.637V_{dc}$; $V_d = 0.966V_{dc}$
 - Zero power delivered by INV2, replace DC source in INV2 by a capacitor

•
$$V_{pseudo} = O'R' = 0.259V_{dc} \angle 75^{o}$$



- O'P' is applied for k * T duration
 O'Q' is applied for (1 k) * T duration,
 T is the duration for which OR' is applied
- Nominal k = 0.732, adjust k to balance INV2 capacitor voltage
 - k > 0.732 charges & k < 0.732 discharges INV2 DC-link capacitor

Obtaining a multilevel Dod-VSVS using a single DC source:

- A 6-concentric Dod-VSVS is obtained from superposition of two 2L Dod-VSVS
- DOD1:[0,1,2,...,11,12]
- DOD2:[0',1',2',...,11',12']
- Superposition example:
 - B1 = DOD1[1]+DOD2[0']
 - D2 = DOD1[1]+DOD2[3']
 - F1 = DOD1[1]+DOD2[1']
 - and so on...



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HEX1 PRI

- DOD2 is generated using HEX2_PRI & switched averaged vectors from HEX2_SEC
- 6-conc Dod-VSVS is obtained as superposition of DOD1 & DOD2
- A 3L Hex-VSVS is a superposition of two 2L Hex-VSVS
- Hence, 6-conc Dod-VSVS is obtained from HEX_3L_PRI and Fig: 6-concentric switched averaged vectors from HEX_3L_SEC



HEX2 PRI



HEX 3L PRI

Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

6-con Dod-VSVS as superposition of hexagons:

 DOD1 is generated using HEX1_PRI & switched averaged vectors from HEX1_SEC

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Fig: 6-concentric Dod-VSVS as superposition hexagons



- Power Circuit Topology:
- DC-links:
 - $V_{prim} = V_{dc}$
 - $V_{sec} = 0.289 V_{dc}$
- Device counts:
 - 12 half bridges
 - 7 capacitors
- Device voltage ratings:
 - INV1: $V_{dc}/2$
 - INV2: 0.1445*V*_{dc}
- Capacitor ratings:
 - INV1: $V_{dc}/2$
 - INV2:
 - FCs: 0.1445*V*_{dc}
 - DC-link: 0.289*V*_{dc}



Fig: Power circuit topology for 6-con Dod-VSVS for open-end winding IMD

- Topology:
 - Open-end winding IM permits superposition of two VSVS
 - HEX_3L_PRI from INV1 & HEX_3L_SEC from INV2
 - Flying capacitor topology is used
 - INV1:
 - $OX = V_{dc}/2$; $OY = V_{dc}$
 - States: $2' \rightarrow V_{dc}$; $1' \rightarrow V_{dc}/2$; $0' \rightarrow 0$
 - INV2:
 - $OX = 0.1445V_{dc}; OY = 0.289V_{dc}$
 - States: $2' \rightarrow 0.289V_{dc}$; $1' \rightarrow 0.1445V_{dc}$; $0' \rightarrow 0$ Fig: VSVS of 3L inverters



Fig: Topology for 6-con Dod-VSVS for open-end winding IM drive







Raw VSVS: Obtained by superposition of primary and secondary three-level hexagonal structures Dodecagonal vectors are generated using vectors from primary inverter and pseudo vectors from secondary inverter⁶ Pseudo vectors are generated by switched averaging of two vectors from secondary inverter 105800 69_{210} Dodecagons Fig: VSVS obtained by superposition of primary and Primary Inverter secondary hexagons Secondary Inverter

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- Example of dodecagonal vector generation using pseudo vectors (dotted lines):
 - Space vector structures are subtracted because of open-end winding connection
 - Vector 13 generated by averaging 101 and 112 with k = 0.732
 - Vector 61 generated by averaging 202 and 102 with k' = 2k - 1 = 0.464
 - k' = 0.464 used for vectors 49, 51, 53, 55, 57 & 59 in E and all vectors (61 to 72) in F
 - Prevents exceeding machine phase voltage rating & reduces INV2 dv/dt





- Space vector structure:
 - 6 concentric dodecagons: A-F
 - 73 vectors including zero vector
 - Two types of dodecagons:
 - Type1: **B**, **D**, **F**
 - Type2: A, C, E
 - $R_A: R_B: R_C: R_D: R_E: R_F = \cos(75^o):\cos(60^o): \cos(45^o):\cos(30^o): \cos(15^o):\cos(0^o)$
 - $R_F = 0.966 V_{dc}$
 - Density increases at higher modulation range
 - Dodecagons are formed in a switched average sense





• PWM Scheme:

Sampled reference based SVPWM timing calculation is implemented

$$V_{ref}T_s = V_0T_0 + V_1T_1 + V_2T_2$$

 $T_s = T_0 + T_1 + T_2$

- $[V_0, V_1, V_2]$ are the adjacent vectors to V_{ref} forming a triangular boundary
- T_s is the sampling duration
- $[T_0, T_1, T_2]$ are durations for which $[V_0, V_1, V_2]$ are applied
- Aim is to find $[V_0, V_1, V_2] \& [T_0, T_1, T_2]$
- Involves:
 - Sector identification
 - Dodecagon identification
 - Triangle identification
 - Vector selection from a LUT





- PWM Scheme1:
 - Conventional SVPWM sequence
 - $\begin{array}{ccc} V_0 \rightarrow V_1 \rightarrow V_2 \rightarrow V_0 \\ \rightarrow V_2 \rightarrow V_1 \rightarrow V_0 \\ \hline \\ \frac{T_0}{4} \rightarrow \frac{T_1}{2} \rightarrow \frac{T_2}{2} \rightarrow \frac{T_0}{2} \\ \rightarrow \frac{T_2}{2} \rightarrow \frac{T_1}{2} \rightarrow \frac{T_0}{4} \end{array}$
 - *k* = 0.732 (0.464) at SS
 - When a vector V_x is applied from INV1, $V_x^i \& V_x^o$ is applied from INV2
 - Scheme1 is used for lower modulation ranges





PWM Scheme2:

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- Capacitor Balancing:
 - Flying capacitor balancing:
 - Utilizing pole voltage redundancy available in generating $\frac{V_{dc}}{2}$ pole voltage (switching state 1).







- Capacitor Balancing:
 - Secondary DC-link capacitor balancing:
 - Is naturally balanced
 - Forced balancing used for startup and to meet non-idealities
 - A simple control loop adjusting value of k
 - k > 0.732 (k' > 0.464) increases capacitor voltage (INV2 sinks power)
 - k < 0.732 (k' < 0.464) decreases capacitor voltage (INV2 sources power)
 - Vector check logic selects k or k' depending on vector to be applied



Fig: Secondary DC-link capacitor balancing


- Capacitor Design: Primary side flying capacitors
 - Nominal operating voltage = $V_{dc}/2$
 - Capacitors are bypassed during states `0' & `2', balancing has to be done whenever state `1' is applied
 - Design:
 - Peak current through capacitor (phase current) = I_p (A)
 - Sampling time duration (duration for which state 1' is applied) = T_s (s)
 - Nominal capacitor voltage = V_c (V)
 - Allowable capacitor voltage ripple = r (%)
 - Capacitor value, $C = \frac{100*I_p*T_s}{r*V_c}$
 - Example: For 50*Hz* operation at 12*spc*, $V_c = 100V$, $I_p = 10A$ and target

$$r = 5\%$$
: $C = \frac{100*10*\left(\frac{1}{50*12}\right)}{5*100} = 3333uF$



- Capacitor Design: Secondary side flying capacitors
 - Nominal operating voltage = $0.1445V_{dc}$
 - Capacitors are bypassed during states `0' & `2', balancing has to be done whenever state `1' is applied
 - Design:
 - Peak current through capacitor (phase current) = I_p (A)
 - Sampling time duration (duration for which state 1' is applied) = T_s (s)
 - Nominal capacitor voltage = V_c (V)
 - Allowable capacitor voltage ripple = r (%)
 - Capacitor value, $C = \frac{100*I_p*T_s}{r*V_c}$
 - Example: For 50*Hz* operation at 12*spc*, $V_c = 28.9V$, $I_p = 10A$ and target r = 5%: $C = \frac{100 \times 10 \times \left(\frac{1}{600}\right)}{5 \times 28.9} = 11534 uF$

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Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD

- Capacitor Design: Secondary side DC-link capacitor
 - Nominal operating voltage = $0.289V_{dc}$
 - $I_{C_s} = sgn(S_A 1) + sgn(S_B 1) + sgn(S_C 1)$
 - Example: 210
 - $I_{C_S} = I_A + I_B + I_C$
 - $I_{C_s} = -2I_C$
 - Worst case capacitor current is $2I_p$
 - Capacitor value, $C = \frac{100*2*I_p*T_s}{r*V_c}$
 - Example: For 50*Hz* operation at 12*spc*, $V_c = 57.8V$, $I_p = 10A$ and target r = 5%: $C = \frac{100 * 2 * 10 * (\frac{1}{600})}{5 * 57.8} = 1154uF$



Secondary Inverter



मारतीय विज्ञान संस्थान



Implementation:

- $V_{dc} = 200V$
- $V_{sec} = 57.8V$
- SKM75GB12T4 (75A, 1200V)
 IGBT half-bridge based inverters
- 3phase currents, capacitor voltages,
 V_{dc} & V_{sec} are sensed
- Capacitors:
 - INV1 FC: 2200uF
 - INV2 FC: 2200uF
 - INV2 DC-link: 2200uF



Fig: Hardware implementation block diagram



Implementation:



Fig: Hardware implementation



Fig: Vdc=200V (1) Phase voltage, 50V/div, (2) Primary inverter pole voltage, 100V/div, (3) Secondary inverter pole voltage, 50V/div, (4) Current, 2A/div; X-axis: 20mS/div

Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) Primary inverter pole voltage, 100V/div, (3) Secondary inverter pole voltage, 50V/div, (4) Current, 2A/div; X-axis: 10mS/div

• Higher frequency switching happens in secondary inverter at low voltage



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Steady state results:



Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) Primary inverter pole voltage, 100V/div, (3) Secondary inverter pole voltage, 50V/div, (4) Current, 2A/div; X-axis: 10mS/div

Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) Primary inverter pole voltage, 100V/div, (3) Secondary inverter pole voltage, 50V/div, (4) Current, 2A/div; X-axis: 5mS/div

Primary inverter switches in quasi-square mode, switching losses are reduced



Steady state results:



Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) Primary inverter pole voltage, 100V/div, (3) Secondary inverter pole voltage, 50V/div, (4) Current, 2A/div; X-axis: 10mS/div



^{10mS/div} Prim inverter pole voltage is square waveform in extreme overmodulation

No fundamental voltage contribution form secondary inverter



Multilevel Dod-VSVS Using a Single DC

Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) Sec flying cap, 50V/div, (3) Secondary DC-link, 50V/div, (4) Current, 2A/div; X-axis: 1S/div

Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) Sec flying cap, 50V/div, (3) Secondary DC-link, 50V/div, (4) Current, 2A/div; X-axis: 1S/div

• Capacitor voltages reaches steady-state without the need of any pre-charging circuitry, voltage balancing happens inherently with the PWM





Transient results:



Capacitor unbalance, Y : (1) 100V/div (2) 20V/div (3) 50V/div (4) 1A/div X : 2S/div

Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) Sec flying cap, 20V/div, (3) Secondary DC-link, 50V/div, (4) Current, 1A/div; X-axis: 2S/div



Capacitor unbalance, Y : (1) 100V/div (2) 20V/div (3) 20V/div (4) 2A/div X : 200mS/div

Fig: (1) Phase voltage, 100V/div, (2) Pri flying cap, 20V/div, (3) Sec flying cap, 20V/div, (4) Current, 2A/div; X-axis: 200mS/div

• Controllers are disabled at point A and then re-enabled at point B



- Conclusion:
 - A multilevel dodecagonal space vector structure using a single DC source for an open-end winding IM is obtained
 - Four quadrant operation is easier since only one DC source is required
 - $6n \pm 1, n = odd$ order harmonics in the phase voltage are eliminated over the entire modulation range
 - Dominant 6th order harmonic torque generation avoided
 - Switching losses are less both in primary and secondary inverters
 - Multilevel structure brings advantages like lesser dv/dt and better THD
 - No capacitor pre-charging circuitry is required, voltage buildup & balancing happens inherently with PWM
 - Linear modulation till $48.83Hz (0.622V_{dc})$
 - Machine phase voltage rating never exceeded
 - Suitable for high performance medium voltage IM drive applications



- A drive scheme for a star connected IM to generate a multilevel Dod-VSVS using a single DC source is proposed.
 - Power circuit topology
 - Dod-VSVS
 - Capacitor balancing
 - PWM Scheme
 - Implementation
 - Results

- Power Circuit Topology
 - FC inverter followed by a cascaded H-Bridge (CHB)
 - 12 half bridges:
 - 6 rated for $V_{dc}/2$
 - 6 rated for $0.1445V_{dc}$
 - 6 capacitors:
 - 3 rated for $V_{dc}/2$
 - 3 rated for $0.1445V_{dc}$
 - Pole voltages:
 - $\bullet \quad V_{AO} = V_{A'O} + V_{AA'}$
 - $V_{A'O} \in [0, \frac{V_{dc}}{2}, V_{dc}]$
 - $V_{AA'} \in [-0.1445V_{dc}, 0 \& + 0.1445V_{dc}]$



Fig: Power circuit topology for 6-con Dod-VSVS for star connected IMD





- Space Vector Structure
 - Obtained by superposition of VSVS of FC and CHB
 - For FC inverter:

•
$$OX = \frac{V_{dc}}{2}; OY = V_{dc}$$

- Pole voltage $(V_{A'O})$ for switching state
 - `2': V_{dc} • `1': $\frac{V_{dc}}{2}$ • `0': 0
- For CHB inverter:
 - $OX = 0.1445V_{dc}; OY = 0.289V_{dc}$
 - Pole voltage $(V_{AA'})$ for switching state
 - $2': +0.1445V_{dc}$
 - `1': 0
 - `0': $-0.1445V_{dc}$







Raw VSVS: Obtained by superposition of primary and secondary three-level hexagonal structures Dodecagonal vectors are generated using vectors from primary inverter **019** and pseudo vectors from secondary inverter⁶/ Pseudo vectors are generated by switched averaging of vectors FC Inverter from secondary inverter CHB Inverter Fig: VSVS obtained by superposition of primary and Dodecagon secondary hexagons



- Example of dodecagonal vector generation using pseudo vectors (dotted lines):
 - Space vector structures are added together instead of subtracting as in the case of open-end winding
 - Vector 13 generated by averaging 101 and 112 with k = 0.732
 - Vector 61 generated by averaging 202 and 102 with k' = 2k - 1 = 0.464
 - k' = 0.464 used for odd-numbered vectors in E and all vectors in F
 - Prevents exceeding machine phase voltage rating & reduces INV2 dv/dt





- Three vector switching:
 - Some of the dodecagonal vectors lie inside a triangle of secondary hexagon
 - Switching the vectors forming the triangular boundary results in reduced dv/dt in the phase voltage
 - For example, dodecagonal vector 48:
 - Could use vectors 120 and 210
 - k = 0.732 is used
 - But vectors [120, 220, 110] are used
 - $[k_0, k_1, k_2] = [0.464, 0.268, 0.268]$
 - Dodecagonal vectors having three vector switching are: 26, 28, 30, 32, 34, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 50, 52, 54, 56, 58, 60
 vector generation using 3 vector switching
 - []; $k_0 + k_1 + k_2 = 1$



0.289V.dc

120

Fig: Dodecagonal

- Set of k values used:
 - Denoted as $[k_0, k_1, k_2]; k_0 + k_1 + k_2 = 1$

Dodecagonal Vectors	k values
0, 2, 4, 6, 8, 10, 12	[1, 0, 0]
1, 3, 5, 7, 9, 11, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 27, 29, 31, 33, 35	[0.732, 0, 0.268]
26, 28, 30, 32, 34, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 50, 52, 54, 56, 58, 60	[0.464, 0.268, 0.268]
49, 51, 53, 55, 57, 59, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72	[0.464, 0, 0.536]

Table: k-value sets used for secondary inverter vector switching

• An LUT stores this information inside the digital controller





- Space vector structure:
 - 6 concentric dodecagons: A-F
 - 73 vectors including zero vector
 - Two types of dodecagons:
 - Type1: **B**, **D**, **F**
 - Type2: A, C, E
 - $R_A: R_B: R_C: R_D: R_E: R_F = \cos(75^o):\cos(60^o): \cos(45^o):\cos(30^o): \cos(15^o):\cos(0^o)$
 - $R_F = 0.966 V_{dc}$
 - Density increases at higher modulation range
 - Dodecagons are formed in a switched average sense





- Capacitor Balancing:
 - FC capacitor balancing (C_{a1}, C_{b1}, C_{c1}) is same as explained before
 - CHB capacitors (C_{a2}, C_{b2}, C_{c2}) have to be balanced individually
 - Adjusting k value
 - Capacitor voltage ripple depends on applied state and phase current direction



(a) State 2; iA +ive; Cap discharges



(e) State 1; iA +ive; Cap bypassed



(b) State 2; iA -ive; Cap charges



(f) State 1; iA -ive; Cap bypassed Fig: CHB inverter switching states, currents and effect on capacitor





(c) State 1; iA +ive; Cap bypassed (d) State 1; iA -ive; Cap bypassed



(g) State 0; iA +ive; Cap charges



(h) State 0; iA -ive; Cap discharges



- CHB Capacitor Balancing:
 - State `2' discharges & `0' charges cap for a positive current
 - State `2' charges & `0' discharges cap for a negative current
 - CHB capacitors are naturally balanced, forced balancing is required during startup and to meet non-idealities
 - CHB capacitors (C_{a2}, C_{b2}, C_{c2}) have to be balanced individually
 - Adjusting k value
 - Forced balancing depends on the vectors applied from CHB inverter to generate the pseudo vectors. Example:
 - 020 & 120 (to generate vector 61)
 - Modifying k affects A-phase cap only
 - 102 & 201 (to generate vector 37)
 - Modifying k affects A & C-phase caps
 - 200 & 201 (to generate vector 69)
 - Modifying k affects C-phase cap only



- CHB Cap Balancing:
 - Consider CHB vector pair 200 & 201(to generate vector 69)
 - Assume 200 & 201 are switched averaged over time duration T_x
 - 200 applied for kT_x duration & 201 applied for $(1 k)T_x$ duration
 - A-phase: State 2 applied for entire T_x duration
 - B-phase: State 0 applied for entire T_x duration
 - C-phase:
 - State 0 applied for $k * T_{\chi}$ duration
 - State 1 applied for $(1 k) * T_x$ duration
 - Changing the value of k affects only C-phase capacitor
 - For positive C-phase current:
 - Applying state 0 for longer duration charges C-phase cap
 - Applying state 1 for longer duration discharges C-phase cap
 - For negative C-phase current:
 - Applying state 0 for longer duration discharges C-phase cap
 - Applying state 1 for longer duration charges C-phase cap



• CHB Cap Balancing:

- Dodecagonal vectors

 7, 13, 18, 19, 24, 25, 30, 31, 36, 37, 42, 43, 48, 49, 55, 60, 61, 66, 67 & 72 are used for balancing A-phase cap (C_{a2})
- Vectors shifted 120° & 240° ⁶⁶ to above vectors are used for balancing B-phase & C-phase caps (C_{b2} &C_{c2}) respectively
- SVL in RED used for A-phase cap
- SVL in GREEN used for B-phase cap
- SVL in **BLUE** used for C-phase cap
- Stored in an LUT



Multilevel Dod-VSVS Using a Single DC

Source for a Star Connected IMD

- CHB Cap Balancing:
 - Capacitor voltage errors are obtained and checked whether they are within a band
 - Polarity of error, direction of current and control sense are used to generate polarity of Δk
 - LUT gives the k values and the control sense
 - Control sense:
 - Which k values to modify
 - In what direction to modify (increase or decrease)







- Capacitor Design:
 - Flying capacitors design is same as before
 - CHB capacitor design:
 - Nominal voltage = $0.1445V_{dc}$
 - CHB capacitor charges when state `0' is applied
 - CHB capacitor discharges when state `2' is applied
 - CHB capacitor is unaffected when state `1' is applied
 - Design CHB capacitors for longest duration for which state 0' or 2' is applied (T_{st02}) with peak current flowing through them

•
$$C = \frac{(100*I_p*T_{st02})}{r*V_c}$$
; $T_{st02} = \frac{1}{spc*f_m}$

• Example: For 50*Hz* operation at 12*spc*, $V_c = 28.9V$, $I_p = 10A$ and target r = 5%: $C = \frac{100*10}{12*50*5*28.9} = 11534uF$

- PWM Schemes:
- Scheme1
- 0-1-2-0-2-1-0 seq
- Timing values T_0, T_1, T_2 and vectors V_0, V_1, V_2 obtained as before
- Scheme1 is used at lower modulation indices



- PWM Schemes:
- Scheme2
- 1-0-2 sequence
- Scheme2 is used at higher modulation indices
- Results in quasi-square switching of primary inverter



- Implementation:
 - $V_{dc} = 200V$
 - SKM75GB12T4 (75A, 1200V)
 IGBT half-bridge based inverters
 - 3phase currents, capacitor voltages & V_{dc} are sensed



- Capacitors:
 - INV1 FC: 2200uF
 - INV2 CHB: 2200uF

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Implementation:



Fig: Hardware implementation

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Steady state results:



Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 100V/div, (4) Current, 1A/div; X-axis: 20mS/div Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 100V/div, (4) Current, 1A/div; X-axis: 10mS/div

Higher frequency switching happens in secondary inverter at low voltage



Steady state results:



Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 100V/div, (4) Current, 1A/div; X-axis: 5mS/div

Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 100V/div, (4) Current, 2A/div; X-axis: 5mS/div

Primary inverter switches in quasi-square mode, switching losses are reduced



17 18 19

Steady state results:



Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 100V/div, (3) CHB inverter pole voltage, 100V/div, (4) Current, 2A/div;

Fig: FFT of (a) FC inverter pole voltage; (b) CHB inverter pole voltage; (c) motor phase voltage;

- Primary inverter switches in square wave mode
- No fundamental voltage contribution form INV2/CHB inverter



2A/div: X-axis: 1S/div

flying cap, 100V/div, (3) CHB inverter floating cap, 50V/div, (4) Current, 5A/div; X-axis: 1S/div

 Capacitor voltages reaches steady-state without the need of any pre-charging circuitry, voltage balancing happens inherently with the PWM





Transient results:



Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter flying cap, 50V/div, (3) CHB inverter floating cap, 20V/div, (4) Current, 1A/div; X-axis: 1S/div

• Controllers are disabled at point t1 and then re-enabled at point t2



- Conclusion:
 - A multilevel dodecagonal space vector structure using a single DC source for a star connected IM is obtained
 - Four quadrant operation is easier since only one DC source is required
 - $6n \pm 1, n = odd$ order harmonics in the phase voltage are eliminated over the entire modulation range
 - Dominant 6th order harmonic torque generation avoided
 - Switching losses are less both in primary and secondary inverters
 - Multilevel structure brings advantages like lesser dv/dt and better THD
 - No capacitor pre-charging circuitry is required, voltage buildup & balancing happens inherently with PWM
 - Linear modulation till $48.83Hz (0.622V_{dc})$
 - Machine phase voltage rating never exceeded
 - Suitable for high performance medium voltage IM drive applications





Oct-VSVS using single DC source

- Two-level
- Extension to multilevel
- Topology
- PWM scheme
- Capacitor balancing & design
- Implementation
- Results


- Octadecagon Using Single DC Source:
- Octadecagonal vectors generated in a switched-averaged sense
 - Two inverters, primary and secondary; two hexagons, primary and secondary
 - Pseudo vectors are generated from secondary hexagon to form octadecagonal vectors
- Example



- Octadecagon Using Single DC Source:
- Octadecagonal vectors generated in a switched-averaged sense
 - Two inverters, primary and secondary; two hexagons, primary and secondary
 - Pseudo vectors are generated from secondary hexagon to form octadecagonal vectors
- Example
 - Primary inverter applies vector OA
 - Secondary inverter generates pseudo vectors Vp18, Vp1, Vp2
 - V18 = OA + Vp18 V1 = OA + Vp1V2 = OA + Vp2





- Octadecagon Using Single DC Source:
- If the resultant octadecagon generates fundamental voltage output equal to the fundamental voltage output from primary inverter:
 - Secondary inverter delivers zero average power
- The condition is given by:
 - Voct = |V18| = |V1| = |V2|
 - 0.637Vdc = 0.6637Voct
 - Voct = 0.9598Vdc
 - Values of Vp18, Vp1, Vp2 found using vector algebra
- Single DC source operation
 - DC source of Vdc for primary inverter
 - Secondary inverter DC-link maintained using capacitor



Fig: Octadecagonal Vector Generation





- Octadecagon Using Single DC Source:
- Values of Vp18, Vp1 & Vp2 (pseudo vectors) are:
 - $Vp18 = 0.3426Vdc \angle -106.63^{\circ}$
 - $Vp1 = 0.0402Vdc \angle 180^{\circ}$
 - $Vp2 = 0.3426Vdc \ge 106.63^{\circ}$
- Secondary inverter DC-link voltage Vsec = 0.379Vdc
- Pseudo vectors are generated in a switched-averaged sense:
 - $Vp2 * T_s = [AR * T_s * k] + [AS * T_s * (1 k)]$
 - T_s is the duration for which V2 has to be applied & $0 \le k \le 1$
 - $\mathbf{k} = 0.7587$ is obtained
- Similarly other pseudo vector values and 'k' values are obtained









Octadecagon Using Single DC Source: Requires two 2-level inverters The structure is only V5 V6a 2-level octadecagon V4V3 • How to get a multilevel structure using single **V**1 V10 DC source? V18 V1 Generate two **V17** independent V16 V13 V14 V15 octadecagons & take superposition of all vectors 162 active vectors forming a 9-concentric octadecagonal structure is obtained Fig: 2-level Octadecagon Generation

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Superposition:



Fig: Superposition of two 2-level octadecagons

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Superposition:



Fig: Superposition of two 2-level octadecagons

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Superposition:



Fig: Superposition of two 2-level octadecagons

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Fig: Superposition of two 2-level octadecagons

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Superposition:

Fig: Superposition of two 2-level octadecagons

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Multilevel Dod-VSVS Using a Single DC Source for an Open-End Winding IMD



Raw VSVS: Secondary Hexagon 131 50 Obtained by superposition of primary and secondary three-level hexagonal structures 128Octadecagonal vectors are generated using vectors from primary inverter and pseudo vectors from secondary inverter 155 Pseudo vectors are 137 generated by switched 156 averaging of vectors from secondary inverter 140 58 Fig: VSVS obtained by superposition Octadecagons Primary of primary and secondary hexagons Hexagon



- Pseudo vectors:
 - Many k-value sets are obtained because of formation of new pseudo vectors

Octadecagonal Vectors	k-values $[k_0, k_1, k_2]$
1, 4, 7, 10, 13, 16, 38, 39, 41, 42, 44, 45, 47, 48, 50, 51, 53, 54, 73, 76, 79, 82, 85, 88	[0.759, 0, 0.241]
2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	[0.653, 0, 0.347]
19, 21, 22, 24, 25, 27, 28, 30, 31, 33, 34, 36, 55, 57, 58, 60, 61, 63, 64, 66, 67, 69, 70, 72	[0.653, 0.106, 0.241]
20, 23, 26, 29, 32, 35	[1, 0, 0]
37, 40, 43, 46, 49, 52	[0.894, 0, 0.106]
56, 59, 62, 65, 68, 71, 91, 93, 94, 96, 97, 99, 100, 102, 103, 105, 106, 108, 128, 131, 134, 137, 140, 143	[0.518, 0.241, 0.241]
74, 75, 77, 78, 80, 81, 83, 84, 86, 87, 89, 90, 110, 111, 113, 114, 116, 117, 119, 120, 122, 123, 125, 126	[0.759, 0.106, 0.135]
92, 95, 98, 101, 104, 107	[0.788, 0.106, 0.106]
127, 129, 130, 132, 133, 135, 136, 138, 139, 141, 142, 144,	[0.73, 0.135, 0.135]
145, 148, 151, 154, 157, 160	[0.788, 0, 0.212]
109, 112, 115, 118, 121, 124, 146, 147, 149, 150, 152, 153, 155, 156, 158, 159, 161, 162	[0.518, 0, 0.482]
Table: k-value sets for secondary inverter vector switching	

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- Superposition requires 2 octadecagons
 - Two 2-level hexagons generates one octadecagon
 - Two sets of two 2-level hexagons can generate two octadecagons
 - The 2-level hexagons get superposed to form 3-level hexagons
 - Hence two 3-level hexagons can generate a 9-concentric octadecagonal structure
 - Primary 3-level hexagon has vector length of Vdc



Fig: Superposition of two 2-level octadecagons

- Secondary 3-level hexagon has vector length of 0.379Vdc
- The inverter topology is realized by cascading a 3-level Flying Capacitor (FC) inverter with an H-bridge (CHB)



- Inverter Topology
 - Single DC source
 - Two 3-level inverters:
 - FC inverter
 - CHB inverter
 - FC capacitor at Vdc/2
 - CHB capacitor at 0.1895Vdc
 - FC inverter generates
 3-level space vector structure of vector length Vdc



Fig: Inverter Topology

- CHB inverter generates 3-level space vector structure of vector length 0.379Vdc
- Sx1 and $\overline{Sx1}$ are complementary; x = a, b, c indicates phase
- 8 switches and 2 capacitors per phase



PWM Scheme:

- Timing calculation involves finding vectors [V₀, V₁, V₂] and timings [T₀, T₁, T₂] satisfying the volt-second balance:
 - $V_{ref}T_s = V_0T_0 + V_1T_1 + V_2T_2$
 - $T_s = T_0 + T_1 + T_2$
 - Similar to steps in [1] [2]
- PWM scheme
 - $V_1 \rightarrow V_0 \rightarrow V_2$ sequence
 - Reduced switchings
 - Quasi-square output from FC inverter
- Example



Fig: PWM Switching sequence



PWM Scheme:

- Timing calculation involves finding vectors [V₀, V₁, V₂] and timings [T₀, T₁, T₂] satisfying the volt-second balance:
 - $V_{ref}T_s = V_0T_0 + V_1T_1 + V_2T_2$
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- PWM scheme
 - $V_1 \rightarrow V_0 \rightarrow V_2$ sequence
 - Reduced switchings
 - Quasi-square output from FC inverter
- Example
 - $73 \rightarrow 91 \rightarrow 74$



Fig: PWM Switching sequence



PWM Scheme:

- Timing calculation involves finding vectors [V₀, V₁, V₂] and timings [T₀, T₁, T₂] satisfying the volt-second balance:
 - $V_{ref}T_s = V_0T_0 + V_1T_1 + V_2T_2$
 - $T_s = T_0 + T_1 + T_2$
 - Similar to steps in [1] [2]
- PWM scheme
 - $V_1 \rightarrow V_0 \rightarrow V_2$ sequence
 - Reduced switchings
 - Quasi-square output from FC inverter
- Example
 - $73 \rightarrow 91 \rightarrow 74 \rightarrow 74 \rightarrow 92 \rightarrow 75 \rightarrow$



Fig: PWM Switching sequence



- Capacitor Balancing
 - FC capacitor balancing is same as explained before
 - CHB capacitors have to be balanced individually
 - A modification is brought in the capacitor balancing scheme:
 - Consider octadecagonal vector 18
 - CHB inverter vectors used are:
 - $[V_0, V_1, V_2] = [100, 000, 101]$, with $[k_0, k_1, k_2] = [0.653, 0, 0.347]$.
 - Since $V_1 = 000$, is the zero vector, the space vector redundancies could also be used and therefore $V_1 = 111$ can also be used
 - The possibilities for capacitor balancing are:
 - 1) A-phase capacitor voltage could be modified by modifying k₀ & k₁ values, keeping k₂ constant
 - 2) B-phase capacitor voltage could be modified by modifying $k_1 \& k_2$ values, keeping k_0 constant (using $V_1 = 111$)
 - 3) C-phase capacitor voltage could be modified by modifying k₀ & k₂ values, keeping k₁ constant.



- Capacitor Balancing
 - All such possibilities as considered and LUTs are created. LUTs contain:
 - k-values to be modified
 - Capacitor that could be controlled
 - Control sense
 - If an octadecagonal vector can control multiple capacitors, choice could be made according to:
 - Maximum deviated capacitor
 - Phase with maximum current
 - In this work, phase with maximum current is chosen
 - Allows fast correction of capacitor voltages
 - A "phase selection logic" does this job



Capacitor Balancing

- Capacitor voltage errors are obtained and checked whether they are within a band
- Polarity of error, direction of current and control sense are used to generate polarity of Δk
- LUT gives the k values, phases and the control sense
- Phase selection logic selects the capacitor to be controlled Octadecagonal



Fig: Secondary inverter DC-link controller



Implementation



 A shaft encoder is used to get rotor position



Fig: Implementation block diagram for multilevel octadecagonal IMD



Implementation

Rotor filed oriented vector control lock diagram



Fig: FOC implementation block diagram





Steady state results:

18Hz (M=0.36)Operation – 72spc – PWM1



Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 50V/div, (4) Current, 1A/div; X-axis: 20mS/div

Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 50V/div, (4) Current, 1A/div; X-axis: 10mS/div

30Hz (M=0.6) Operation – 36spc – PWM1

• Higher frequency switching happens in secondary inverter at low voltage





Steady state results:

40Hz (M=0.8) Operation – 18spc – PWM2



Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 50V/div, (4) Current, 1A/div; X-axis: 5mS/div

Fig: Vdc=200V (1) Phase voltage, 100V/div, (2) FC inverter pole voltage, 200V/div, (3) CHB inverter pole voltage, 50V/div, (4) Current, 1A/div; X-axis: 5mS/div

49Hz (M=0.98)Operation – 18spc – PWM2

Primary inverter switches in quasi-square mode, switching losses are reduced



Steady state results:





Primary inverter switches in square wave mode



- Steady state results: FFT at 50Hz (M=1)
- FC inverter generates square wave output
- FFT of FC inverter shows 5th, 7th, 11th, 13th ... order harmonics in the pole voltage
- CHB generates
 5th, 7th, 11th, 13th ...
 harmonics of same amplitude
- FFT of phase voltage shows the absence of 5th, 7th, 11th, 13th ... harmonics
- CHB generates zero fundamental voltage output
- CHB functions as a harmonic filter







Transient operations:



Fig: (1) Phase voltage, 200V/div, (2) FC inverter capacitor voltage, 100V/div, (3) CHB inverter capacitor voltage, 50V/div, (4) Current, 5A/div; X-axis: 1s/div

2 4

Fig: (1) Phase voltage, 200V/div, (2) Rotor flux angle, (3) Phase current, 5A/div, (4) Rotor speed, -47Hz to +47Hz; X-axis: 1s/div

Capacitor voltages settle and stay at nominal values at end of startup

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Transient operations:

Speed Reversal using FOC

2

4



Fig: (1) Rotor mag current, 0.75A, (2) Isq, 1.5A step, (3) Phase current, 5A/div, (4) Rotor speed, -47Hz to +47Hz; X-axis: 1s/div

Fig: (1) FC inverter capacitor, 200V/div(2) CHB inverter capacitor, 200V/div, (3) Phase current, 5A/div, (4) Rotor speed, -47Hz to +47Hz; X-axis: 1s/div

• Capacitor voltages stay at nominal values



- An IMD scheme with following advantages are proposed:
 - Single DC source requirement
 - Reduces system cost
 - Permits easy four-quadrant operation
 - 9-concentric multilevel octadecagonal space vector structure
 - Low order harmonics of orders: 5th, 7th, 11th & 13th are eliminated from phase voltage and hence current
 - Absence of low order torque ripple
 - Low THD phase voltage due to multilevel operation
 - Low dv/dt output
 - Linear modulation range extended till 49.5Hz (M=0.99)
 - Capacitors in the circuit are inherently balanced with the PWM operation
 - Controlled switching losses
 - Quasi-square waveform switching from FC inverter
 - Low voltage switching for CHB inverter

Conclusion



- IMD schemes with six-concentric-dodecagonal & nine-concentric octadecagonal voltage space vector structures are proposed
- Following are the features
 - Single DC source requirement
 - Reduces system cost & permits easy four-quadrant operation
 - Low order harmonics are eliminated
 - Low order torque ripple is avoided
 - Requirement of filters are avoided or relaxed
 - Multilevel operation brings:
 - Low THD phase voltage due to multilevel operation
 - Low dv/dt output
 - A secondary inverter operating at low voltage functions as a harmonic filter
 - Quasi-square waveform switching from primary inverter controls losses





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THANK YOU!

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