Unique Rise Time Sensitivity Leading to Air Discharge System-Level ESD Failures in Bidirectional High Voltage SCRs

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***Abstract*— This article discloses a unique failure mode in high-voltage bidirectional (Bi-Di) silicon-controlled rectifier (BDSCR) cells during International Electrotechnical Commission (IEC) air discharge electrostatic discharge (ESD) events. Failure was found to be sensitive to IEC measurement conditions or variabilities such as the speed of IEC gun and angle of approach, which causes different stress rise times. Hence, observed failure was a peculiar function of the rise times of the discharge current waveform. Remarkably, failure in high-voltage BDSCR was observed only for a window of current rise times. A new approach is presented using 3-D TCAD simulations of multifinger BDSCR to study and probe the failure mechanism dependent on these system-level stress parameters and variabilities. By emulating the experimental conditions in a 3-D TCAD environment, physical insights are developed to probe the root cause of the observed air discharge failures. Furthermore, a device engineering approach has been proposed, with the help of 3-D TCAD simulations of multifinger BDSCR, which computationally demonstrated improved robustness of BDSCR multifinger cells against IEC air discharge failures. The proposed design mitigates the nonuniform turn-on and failure due to IEC stress or rise time variability at the cost of a negligibly small area overhead.**

***Index Terms*— Bidirectional (Bi-Di) silicon-controlled rectifiers (BDSCRs), current filaments, electrostatic discharge (ESD), multifinger turn-on.**

I. Introduction

HIGH-voltage input–output (I/O) pads in system-on-chips (SOCs), power SoCs, and automotive products often experience electrostatic discharge (ESD) failures, particularly during their end-use in systems [1]. The ESD problem at high-voltage I/O pins becomes pertinent, particularly in uncontrolled environments, say automotive. Uncontrolled ESD environments like these can induce very high current levels into the electronic system. For system-level International Electrotechnical Commission (IEC) standards, such as IEC-61000-4-2, the first peak current can go up to a few tens of amperes (in a shorter time), compared with 1–2 A for an human body model (HBM) event in an ESD-controlled environment [2]. In some applications, it is desired that the products be capable of surviving these system-level ESD events without the assistance of off-chip ESD protection (e.g., transient voltage suppression (TVS) diodes). Therefore, developing on-chip ESD protection for different IEC standards is a new challenge. On the other hand, it can reduce the system cost by significantly avoiding off-chip protection elements, but at the cost of chip area penalty. This trade-off is required to be addressed.

Developing high-voltage ESD protection elements is, however, challenging, mainly because of lower well dopings that result in conductivity modulation and associated consequences during high current injection [3]. The laterally double-diffused MOS (LDMOS) and drain extended MOS (DeMOS) devices, which are frequently used in high-voltage I/O drivers, have been established to be vulnerable against ESD stress [4]. One reason for this vulnerability is an early space charge modulation (SCM) in the n-well, which causes device failure at the onset of voltage snap-back with electrothermal filament formation [5]. Several modified designs for the basic LDMOS construct were proposed in the literature to improve the overall ESD robustness by delaying the onset of SCM to higher current levels [6], [7]. However, the approaches proposed earlier are often technology node/process-dependent and only provide a limited improvement in ESD robustness. The limited It2 improvements and significantly high current protection requirements under system-level ESD stress conditions hinder the development of a self-protected driver, which demands a high-voltage ESD solution for these high-voltage I/Os in automotive and power SoC products.

The high-voltage SCR is a desirable solution for achieving a compact ESD solution due to its high current-carrying ability [8], relative to other ESD protection device types. High-voltage SCRs are often developed in an LDMOS process [9] to

Manuscript received September 13, 2021; revised January 4, 2022 and February 11, 2022; accepted March 8, 2022. Date of publication March 28, 2022; date of current version April 22, 2022. The review of this article was arranged by Editor C. Duvvury. *(Corresponding author: N. K. Kranthi.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2022.3159281.

Digital Object Identifier 10.1109/TED.2022.3159281

be used as unidirectional ESD protection elements. However, signal excursions on various I/Os can drop below ground voltage, necessitating ESD protection elements that can block high voltage for both polarities [10]. Bidirectional (Bi-Di) ESD elements can be made with back-to-back connection of unidirectional LDMOS/DeNMOS SCRs or can be developed in a single device with intrinsic SCR action for both stress polarities [10], [11].

However, studies in the past highlighted the challenges associated with the use of such SCRs as a high-voltage ESD protection element. System-level ESD pulses can last longer than typical HBM time scale [12]. It was found that although high-voltage SCRs can pass HBM qualification tests, they can fail in the products for long-duration pulse discharges because of power scalability problems [12], [13]. Various design solutions are proposed to safely conduct low currents for longer duration [14]. Window failures associated with the presence of a common-mode choke in the stress path were also studied in the past [15], [16] for back-to-back connected SCR cells.

System-level ESD qualification may require an on-chip SCR to pass multiple qualification tests including the human–metal model (HMM), ISO cable discharge tests, and other IEC tests. IEC tests can be conducted in two configurations: direct contact and indirect air gap. Direct contact tests were considered rather stringent in the past because of the higher current levels involved. It is assumed that if the cell passes IEC direct contact test, air gap qualification is guaranteed. However, recent works have shown this to be untrue. In [17], a missing correlation between HMM and air gap discharge stress is shown. This article investigates another instance where air discharge results were not predicted by contact discharge. Specifically, allowed variation in the ESD gun speed and angle of approach during air discharge stress produce a variation in current waveforms; a subset of these caused failures. By examining different current waveforms, a sensitivity to pulse rise times is identified. This work presents a detailed, physics-based analysis and explanation for the observed failure. Besides, a proposal to improve the ESD robustness of these HV SCRs under these unique IEC conditions is given.

The article is arranged as follows. Section II presents the working of the high-voltage Bi-Di SCR under test. Besides, experimental details of the air discharge ESD failure are presented. Section III discloses the TCAD simulation setup details, including various physical models and stimulus shape definition for emulating air discharge events. The root cause of device failure is explored in Section IV. Besides, detailed physical insights are presented to explain the same. In Section V, a modified design to improve Bi-Di SCR's robustness against air discharge stress is proposed. Finally, the findings are concluded in Section VI.

II. Device Under Test and Air Discharge Problem

A. Device Under Test

The high-voltage Bi-Di SCR protecting the I/O circuits against the system-level ESD surges is as depicted in Fig. 1.

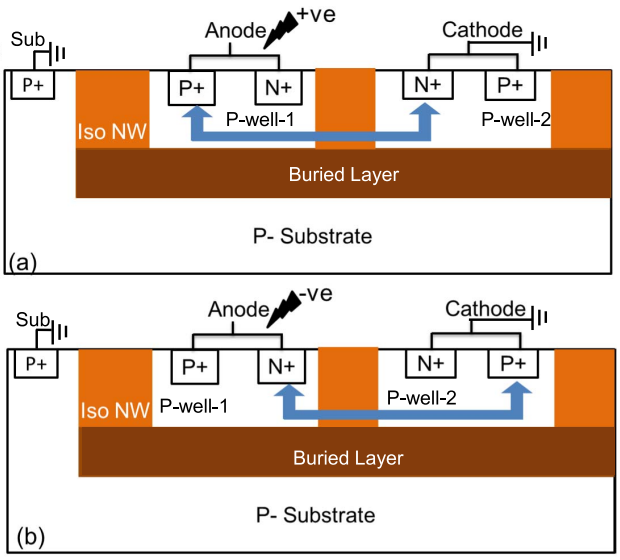

Fig. 1. 2-D cross-sectional view of a single-finger Bi-Di SCR depicting the current path for (a) positive stress on anode and (b) negative stress on anode.

In general, the back-to-back connection of two uni-directional SCRs can also be used to form a Bi-Di ESD cell. This requires two DeNMOS/LDMOS SCR devices, leading to a large area footprint. Another approach is to design an SCR that has inherent Bi-Di high-voltage blocking capability, as shown in Fig. 1. In this SCR, the iso n-well and buried layer are left floating to take both positive and negative potentials for different ESD strikes (positive and negative). Each finger of Bi-Di SCR contains two p-wells as depicted in Fig. 1. Furthermore, each p-well has P+ and N+ diffusions connected together. The N-buried layer shields the p-wells from the global substrate. Two well junctions are formed in each finger. Junction J1 is between the first p-well and n-well. The second junction J2 is between p-well-2 and n-well. One of the junctions mentioned above blocks the high voltage depending on the type of stress. The operation of Bi-Di SCR under positive and negative strikes is explained below. Although the anode and cathode names can be used interchangeably in this device, the terminal connected to the pad is named anode to avoid further confusion.

1) Positive Stress: During a positive ESD strike at the pad, the P+ pickup in p-well-1 together with p-well-1 acts as the anode. The voltage on the anode terminal increases with increasing injected current. The n-well (Iso + buried well) takes positive potential through p-well-1. An increasing potential difference between the n-well and p-well-2 junction causes impact ionization and avalanche action. Subsequent junction breakdown occurs between p-well-2 and n-well at the critical electric field. The generated electrons are accumulated in the n-well, whereas holes are collected at the p-well-2 pickup. Hole conduction in p-well-2 raises the local potential and forward biases the N+ cathode/p-well diode, which injects additional electrons into the n-well region, and complete SCR turn-on is achieved. The SCR current path is between P+ in p-well-1 and N+ contact in p-well-2, as depicted in Fig. 1(a). In the Bi-Di SCR, the peak electric field continues to be at p-well-2 and n-well junction even after the SCR turns on.

2) Negative Stress: When there is a negative ESD strike at the pad, n-well gets the negative potential. In this stress combination, junction breakdown occurs at p-well-1 and buried n-well junction. The generated holes get collected at the most negative potential, i.e., P+ pickup in p-well-1. Excess holes in the p-well raise the potential near the N+ contact, turning on the N+/p-well-1 diode. The P+ pickup in p-well-2 along with p-well-2 acts as an anode. The avalanche-generated electrons and holes trigger the SCR, with a current path shown in Fig. 1(b).

B. IEC Measurement Results and Rise Time Sensitivity

The qualification of system-level IEC requires two test configurations: direct and indirect IEC tests. In the direct test, the sharp tip of the ESD gun lands directly on the printed circuit board (PCB) discharge tip connected to the IC pin under test. After locking the position, the ESD generator is set to the desired stress level, and N number of pulses of different polarities is applied. The voltage and current through the device are measured. In general, direct contact discharges have high first current peak with rise time in the range of 1–3 ns. In the case of indirect IEC system-level ESD qualification, discharge is done through air. In general, air discharge IEC qualification is considered to be a less challenging requirement. Peak current levels of air discharges are much lower than those of contact discharges at the same precharge stress levels. However, the air discharge pulse shape is a function of several factors, such as humidity, temperature, and speed and angle of approach of the ESD gun. Fig. 2(a) depicts the technique for characterizing possible current waveform during the air discharge test used for the measurements presented in this work. The trigger is pulled to a precharge tip, and the gun is moved toward the PCB pin tip. The discharge occurs when a spark forms between the gun tip and the PCB pin tip. Fig. 2(b) shows several pulse current waveforms measured at the device under test (DUT) for an air discharge test at the precharge level of −6 kV. These waveforms are captured at different speeds of approaches of the ESD gun at the same temperature and humidity levels. The measurement can produce significant fluctuations in the pulse rise time and peak current with variations in the trigger pull, air temperature, and humidity levels. For a precharge voltage of −6 kV, product failures are seen in cases where the pulse rise time is approximately 10 ns (moderate gun speed). When the discharge is very fast (1–5 ns rise time) and very slow (40–50 ns), the device is found to pass the air gap test. However, product failures are observed for critical rise times around 10–20 ns. It is also observed that peak current also varies with pulse rise time. With a longer rise time, the observed peak current is smaller. Table I summarizes the IEC measurement results for both contact and air discharge. The ESD cell passes all the contact discharges up to −15 kV. However, sporadic failures in air discharge measurements are seen at −6 kV and higher stress levels. The DUT was also found to pass all the positive stress polarity air discharge IEC tests till 15 KV. It should be noted that the observed rise time sensitivity in the IEC air discharge waveforms was not observed in the Transmission Line Pulse (TLP) measurements with varying pulse rise time (data not shown). This is possibly due to the load line effect and dependence of injected current on the system/load (DUT) parasitic, including the parasitic in series contributed by the air gap.

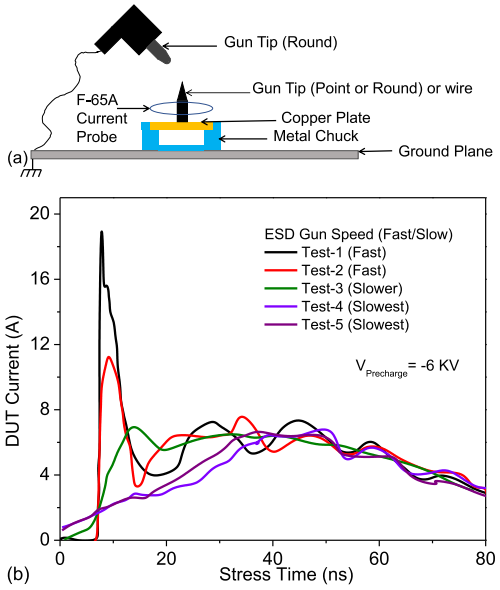

Fig. 2. (a) Experimental setup for air discharge IEC measurements. A precharged IEC gun is bought close to the target (DUT) and the trigger is pulled manually. (b) Current pulse waveforms recorded at the DUT for different test conditions stressed at the same precharge level of −6 KV.

TABLE I
IEC RESULTS SUMMARIZING PASS/FAIL INFORMATION AT DIFFERENT STRESS LEVELS FOR BOTH CONTACT AND AIR DISCHARGE. THE ESD CELL IS FOUND TO PASS THE CONTACT STRESS UP TO −15 KV (DATA NOT SHOWN) BUT FAILS AT −6 KV DURING AIR DISCHARGE. THE FAILURE IS SPORADIC AND SENSITIVE TO THE MEASUREMENT CONDITIONS

IEC Stress Level (KV)	Contact Discharge (P/F)	Air Discharge(P/F)
-1	Pass	Pass
-2	Pass	Pass
-3	Pass	Pass
-4	Pass	Pass
-5	Pass	Pass
-6	Pass	Fail

III. UNIQUE APPROACH USING 3-D TCAD FOR AIR DISCHARGE FAILURES

A. 3-D TCAD Framework

The three-finger Bi-Di SCR structure depicted in Fig. 3 is simulated using TCAD. The simulated device was kept significantly smaller in terms of the number of fingers than the physical device to aid in convergence of 3-D TCAD simulations. The ESD cell is sized according to IEC contact qualification requirements. However, simulation trends and physical insights gained from three-finger structures can be used to understand the air discharge problem in detail. Also, simulating an IEC-sized cell is not practically possible due to the computational complexity. Electrical and thermal boundary conditions are defined with proper mesh to perform electrothermal simulation. Drift diffusion equations are solved,

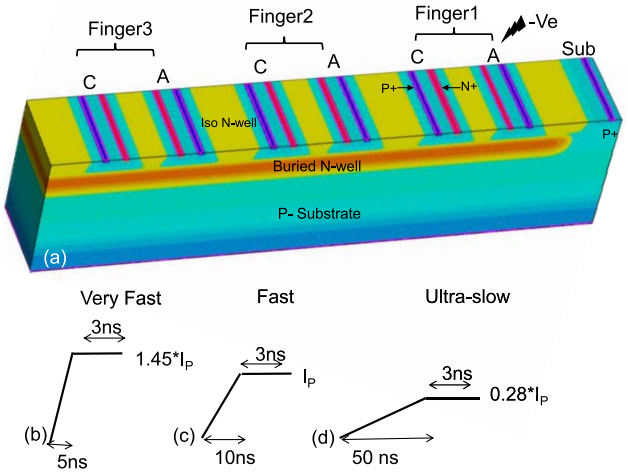

Fig. 3. (a) 3-D view of multifinger Bi-Di SCR structure used for TCAD simulations. Anode and cathode in each finger are marked. Negative stress is applied to the anode of the SCR during simulations. (b) Different stimulus shapes used in this work for studying air discharge in Bi-Di SCRs.

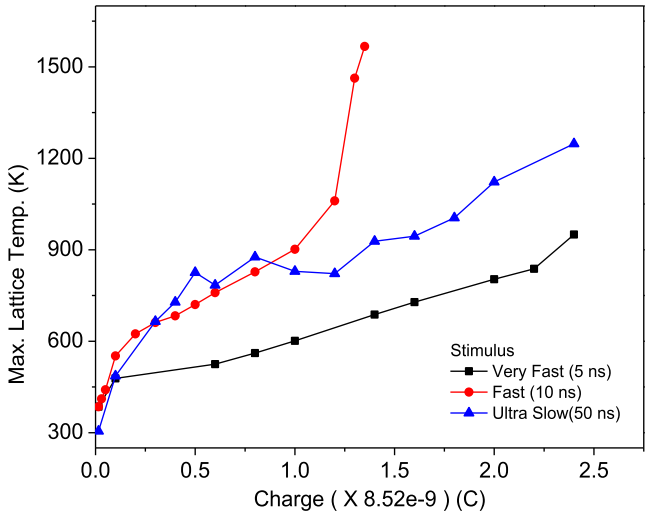

Fig. 4. Simulated (3-D) maximum lattice temperature in Bi-Di SCR (three fingers) as a function of charge under different stimulus shapes. Under very fast and ultraslow stimuli, the device survives high charge levels. However, the SCR fails under fast stimulus, as indicated by a rapid increase in lattice temperature.

coupled with the temperature equations. Various physical models are incorporated in device simulations to account for high current and field effects. Effects such as impact ionization, high-field mobility degradation, carrier recombination, and band gap narrowing are captured with the models used for the simulations presented in this work.

B. Definition of Stimulus in TCAD for Mimicking the Air Gap Failure

Simulating the on-chip system-level IEC failures using TCAD is complicated by the uncertainty in determining the proper stimulus shape. Generally used square pulse shapes with specific pulse rise time (TLP-like) cannot emulate specific stress conditions during IEC tests. For example, DeNMOS-SCR failures under IEC stress through a common-mode choke cannot be replicated using TLP-like pulse shapes. A double-pulse shape stimulus is used to demonstrate and understand the root cause in [16].

The air discharge failure observed in the Bi-Di SCR investigated in this work is not replicated in TLP testing with varying pulse rise times. As mentioned in Section II, the measured current waveforms for different air discharges at the same precharge stress level vary in peak current and pulse shape via rise time. A new approach is proposed to study device failure under such peculiar cases based on the constant charge stimulus method for TCAD simulations. Fig. 3(b) depicts different pulse shapes used to demonstrate the observed rise time sensitivity of device failure in TCAD. The Bi-Di SCR is stressed with three different pulse shapes: 1) very fast pulse (rise time = 5 ns); 2) fast pulse (rise time = 10 ns); and 3) ultraslow pulse (rise time = 50 ns). The duration of the peak in each pulse is kept constant (3 ns in this case). However, to compare the device response with different pulse shapes, there should be one constant parameter (similar to precharge voltage in experiments). Here, device responses to different pulse shapes are compared at a constant charge value, Q. At a fixed charge value, each of the three stimulus types has a different peak current (I_P). Note that the charge is the area under the stimulus current pulse shape. For the charge to remain constant, the peak current should vary with rise time. For example, if the current peak value is (I_P) for a fast pulse at charge level Q, then for the same charge level, the very fast stimulus has $1.45\times$ (I_P) higher peak current. Similarly, the ultraslow pulse should have approximately 70% smaller current peak than (I_P) for the same charge level Q. In summary, the simulation approach uses charge as equivalent to precharge voltage during actual IEC measurements. This helps obtain different pulse shapes with varying rise time and peak current, as measured in air discharge IEC stress. This approach helps capture the rise time sensitivity in simulations, as was observed in measurements.

C. Demonstration of the Problem Using TCAD

The three-finger structure, as depicted in Fig. 3(a), is stressed with the three aforementioned pulse shapes at different charge levels. Maximum lattice temperature inside the silicon volume is extracted at various stress levels for each stimulus shape, as depicted in Fig. 4. Under the very fast stimulus, the lattice temperature is limited below critical temperature (1600 K) limits until high stress (charge) levels. During ultraslow pulse conditions, though the lattice temperature is higher than that of very fast stimulus stress, it does not exceed the critical temperature, and the device continues to survive higher charge levels. Under fast pulse stress, lattice temperature first gradually increases, followed by an abrupt increase in temperature. The maximum temperature inside the silicon under fast stimulus reaches a critical temperature, indicating early device failure under fast stimulus stress conditions. In summary, the simulated device was found to survive very fast and ultraslow pulse shapes until high charge levels but was observed to suffer early failure for fast pulse stress.

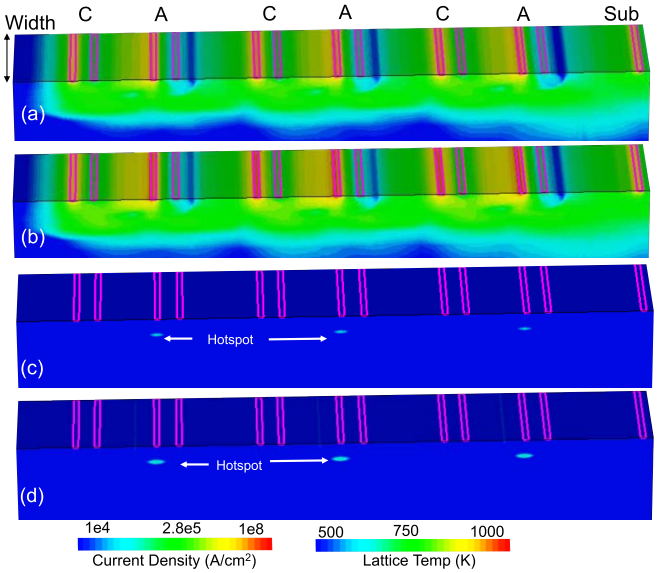

Fig. 5. (a) and (b) Conduction current density (A/cm^2) and (c) and (d) lattice temperature (K) extracted at the end of very fast (RT = 5 ns) stimulus for (a) and (c) lower stress level ($Q = 0.8 \times$ 8.52e-9 C) and (b) and (d) higher stress levels ($Q = 1.4 \times$ 8.52e-9 C). Uniform turn-on of all the fingers is observed for very fast stimulus.

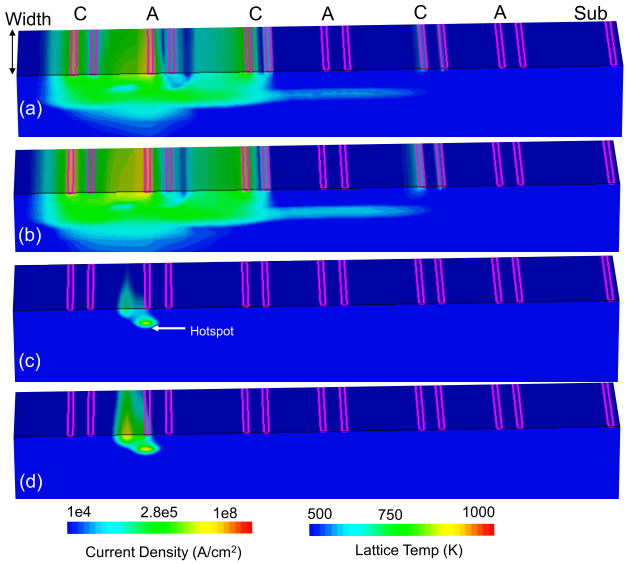

Fig. 7. (a) and (b) Conduction current density (A/cm^2) and (c) and (d) lattice temperature (K) extracted at the end of the ultraslow (RT = 50 ns) stimulus for (a) and (c) lower stress level ($Q = 0.8 \times$ 8.52e-9 C) and (b) and (d) higher stress levels ($Q = 1.4 \times$ 8.52e-9 C).

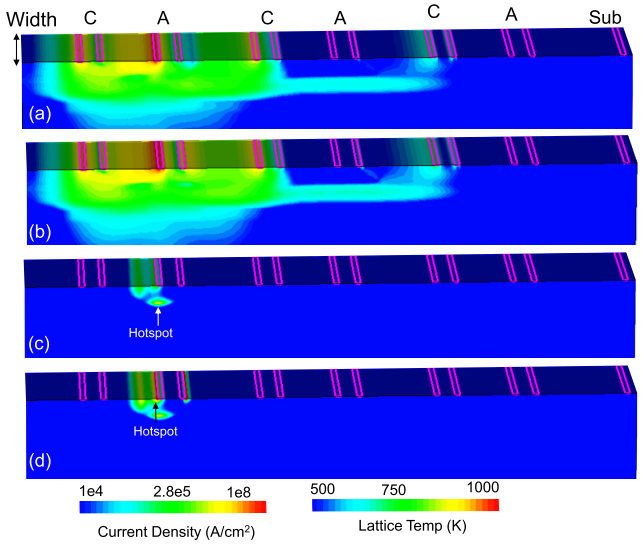

Fig. 6. (a) and (b) Conduction current density (A/cm^2) and (c) and (d) lattice temperature (K) extracted at the end of fast (RT = 10 ns) stimulus for (a) and (c) lower stress level ($Q1 = 0.8 \times$ 8.52e-9 C) and (b) and (d) higher stress levels ($Q2 = 1.2 \times$ 8.52e-9 C). Nonuniform turn-on can be seen across fingers.

IV. Root Cause and Physical Insights

A detailed analysis is presented to understand the root cause of air discharge failures for rise times in the range of 10 ns. Current density and lattice heating are analyzed with stress (charge) levels for different pulse shapes. Fig. 5 depicts the conduction current density and lattice temperature in a three-finger structure extracted at two different charge levels (Q1 and Q2) under a very fast stimulus. It is observed that all the fingers are found to participate in the current conduction under very fast stimulus. The uniform turn-on of all the fingers at lower charge levels (Q1) results in minimal lattice heating inside the device. Even at higher charge levels (Q2), the current density is found to be still limited in each finger. Therefore, the hot spot continues to exist at each of these junctions as shown in Fig. 5(d). As the current density increases, these hot spots become stronger. The uniform turn-on of different fingers under the very fast stimulus condition is attributed to a large dV/dt resulting from the high slew rate of the stimulus current (di/dt) pulse. Note that the peak current in a very fast stimulus is approximately 1.5× higher than that of the fast pulse, resulting in larger di/dt for the same charge. The displacement current along with avalanche current at the high electric field helps in uniform turn-on of different fingers in Bi-Di SCR. During the voltage ramp-up, all the fingers have impact ionization at the p-well/n-well junction. Under the very fast stimulus, as the voltage does not drop (overshoot) even after one early finger turn-on [18], it allows other fingers to turn on as well. Fig. 6 depicts the conduction current density and lattice temperature for fast stimulus (RT = 10 ns) at two different stress levels. Stress levels (Q1 and Q2) are chosen so that the lower charge level (Q1) represents device conduction prior to an increase in temperature (see Fig. 4). The second stress level (Q2) represents conduction during rapid temperature rise. It is observed that under both stress levels, only one of the fingers conduct [see Fig. 6(a) and (b)]. The turn-on of a few fingers for slower rise times is already well-established in the literature [18]. Due to process variations, some nonuniformity in the structure always allows a few fingers to turn on first, followed by others. The physics of sequential turn-on is explained in detail in [18] in SCR devices. When one of the fingers triggers, the terminal voltage reduces, which lowers the impact ionization-generated carriers; as a result, the other fingers fail to turn on. Therefore, the turn-on of the remaining fingers depends on the minority carrier diffusion from the conducting finger to the neighboring fingers. This makes the

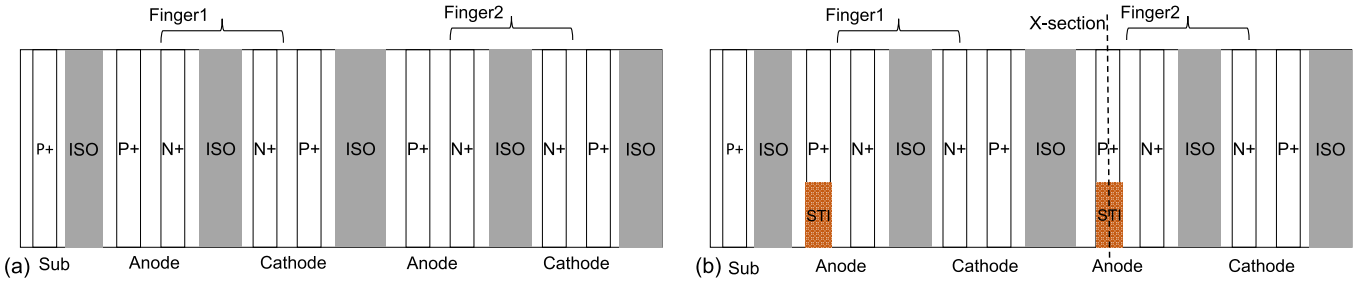

Fig. 8. Top view of multifinger. (a) Reference Bi-Di SCR. (b) Proposed well-tapped Bi-Di SCR. Only a two-finger structure is shown here for simplicity.

multifinger turn-on a sequential event. The hotspot is formed at the p-well and N-buried junction at lower stress levels in the SCR under test. However, with an increase in localized current density in the SCR finger, conductivity modulation was found to occur in the p-well, which led to a strong lateral SCR conduction at the surface. At a specific current density in the finger, the hotspot undergoes a shift from the well junction to the N+ cathode, causing an abrupt increase in temperature and strong hotspot formation, as depicted in Fig. 6(d). This results in early failure of the Bi-Di SCR under the fast stimulus in one of the fingers. The shift in the hotspot is due to the presence of more substantial lateral SCR conduction at the surface and not due to the Kirk effect.

The Bi-Di SCR survives a high charge level when stressed with an ultraslow stimulus (RT = 50 ns). Current density and lattice temperature for different stress values (Q1 and Q2) are as depicted in Fig. 7. As seen from Fig. 7(a) and (b), similar to the fast stimulus, only one of the three fingers begins conducting current under ultraslow stimulus stress conditions. The hotspot is formed at the p-well and N-buried junction during low stress levels (Q1), as shown in Fig. 7(c). At a higher stress level (Q2), though only one of the fingers conducts, the lower current density associated with the ultraslow pulse does not induce a shift in hotspot to the N+ cathode [see Fig. 7(d)]. The lateral SCR current density at the surface does not exceed the critical limit. The hotspot continues to be present at the junction region. This will ensure that lattice temperature does not dramatically increase at low stress levels, and the device can sustain higher stress under ultraslow pulse conditions.

In summary, under a very fast stimulus, most fingers participate in conduction. Uniform current distribution across fingers enables the device to survive higher stress levels. However, under an immediate/fast stimulus, the nonuniform turn-on of a small number of fingers in the device causes increased current density and nonuniform heating across the fingers. Device failure takes place after strong hotspot formation. However, though only a few fingers turn on for the ultraslow stimulus because of the reduction in displacement current, the smaller current in the pulse makes it safely conduct until high stress levels, despite having fewer fingers conducting the discharge current.

V. Well-Tap Engineering

From the previous discussion, it can be concluded that nonuniform turn-on across a large number of fingers and associated higher current density for the fast stimulus is the primary reason for air discharge damage. The mutual ballasting technique presented in [15] to improve multifinger turn-on for slower rise times cannot be implemented in the Bi-Di SCR structure. The mutual ballasting technique is a way to connect the middle node of the two metals when a Bi-Di protection cell is formed with back-to-back connection of two single-ended SCRs. However, the Bi-Di SCR under test does not involve such metal connections of single-ended SCRs. The well-tap engineering approach is presented to address rise time sensitivity-induced air discharge failures; this approach is intended to improve turn-on uniformity across multiple fingers.

Fig. 8 depicts the top view of the reference structure and well-tap engineered device. A two-finger structure layout is shown for simplicity, though all TCAD simulations in this work were conducted with three-finger 3-D structures. The engineered structure in Fig. 8(b) has p-well taps blocked at the edges of its anode fingers using shallow trench isolation (STI). The simulated TCAD structure has a well-tap blocking length of 3 μm for a 15-μm-wide device. The n-well in the Bi-Di SCR is floating and does not have an n-well pickup. P+ is blocked only on the anode diffusion to improve negative mode triggering uniformity. A cross-sectional view of the well-tap engineered structure along the finger width is depicted in Fig. 9. The cross section is extracted at the well-tap blocking STI as shown in Fig. 8. Extracted maximum lattice temperature for the reference structure and the well-tap engineered structure is plotted in Fig. 10. The maximum temperature is extracted at different charge levels for the fast stimulus. As discussed in Section IV, the reference device shows an abrupt rise in lattice temperature at lower charge levels. However, the well-tap engineered structure does not significantly increase the lattice temperature until high charge levels. This result demonstrates the robustness of the well-tap engineered devices against rise time sensitivity-induced air gap failures.

The physical reasons for the robustness of the engineered structure can be seen from Fig. 11. Current density and lattice temperature are extracted at different charge levels for a well-tap engineered device. Uniform conduction across fingers in a well-tap engineered device can be seen in Fig. 11(a) and (b). By selectively blocking the well tap at the finger edges, high-resistance p-well regions are created in every finger, encouraging strong triggering of the SCR at the edges of the device, independent of the pulse rise time. The higher resistance part of the p-well region for engineered SCR

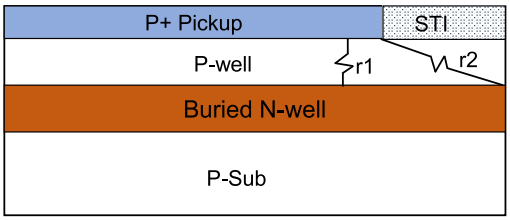

Fig. 9. Cross-sectional view of the well-tap engineered SCR depicting the different body resistances experienced by the generated holes near the buried n-well and p-well junction.

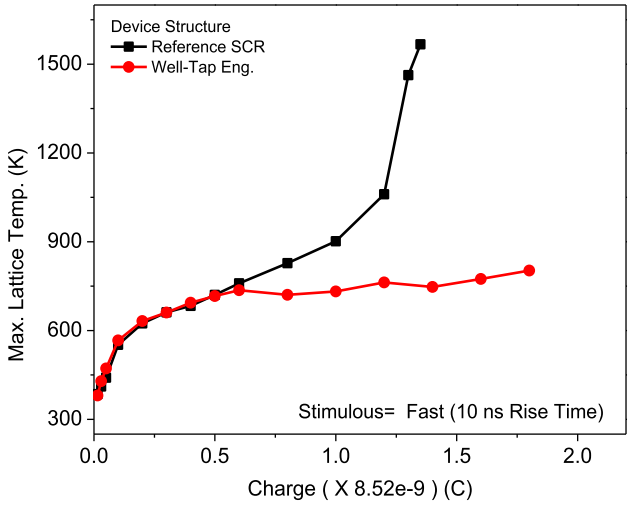

Fig. 10. Simulated (3-D) maximum lattice temperature (K) of reference and well-tap engineered Bi-Di SCR plotted as a function of charge, stressed with fast stimulus. The well-tapped structure does not show increases in the lattice temperature at low stress levels.

is depicted in Fig. 9 as r2. Avalanche-generated holes experience a higher resistance (r2) at the finger well-tap blocked region than the unblocked region (r1). Higher p-well resistance at the finger edges requires a lower current to trigger the SCR. The reduction in trigger current with well-tap blocking is first observed in experiments in [19]. The displacement current is no longer needed for uniformly turning on the SCR. This makes the engineered SCR turn-on insensitive to the pulse rise time variations. This improves the overall uniformity in the SCR turn-on across different fingers and causes lower lattice heating in the device as depicted in Fig. 11(c) and (d). It should be noted that the difference in the current through the substrate contact in the reference and well-tap engineered structures (see Figs. 6 and 11) is due to the presence of SCR turn-on in the finger next to the P-sub contact. The P-sub forms a weak SCR with an N+ anode in the finger next to it. If this finger turns on, it shares current with P-sub contact. This is also evident from the very fast pulse response depicted in Fig. 5.

The well-tap blocking at the edges in the engineered structure reduces the effective anode area for positive stress combination. The P-tap that is being blocked acts as an anode for positive stress. This will require additional fingers to be added to the engineered structure to accommodate the current in positive stress combination. If the well-tap blocking is 3 μm for a 50-μm-wide finger, 6% of the additional anode area has

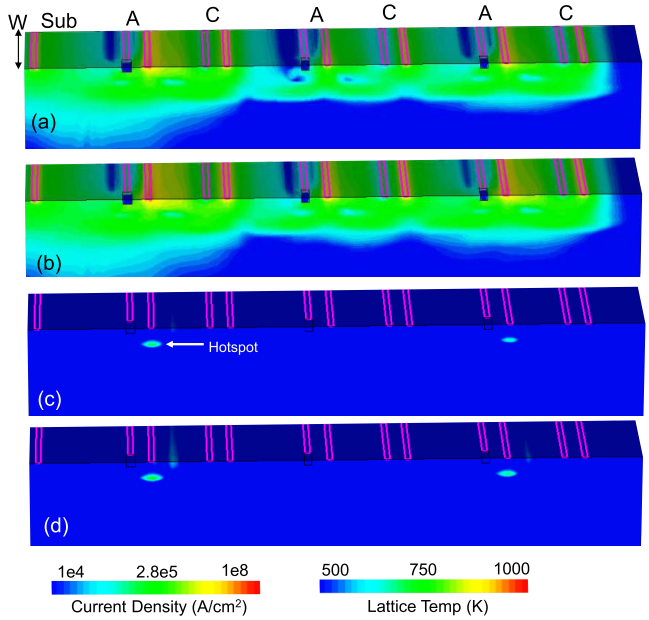

Fig. 11. (a) and (b) Conduction current density (A/cm^2) and (c) and (d) lattice temperature (K) extracted at the end of fast (RT = 10 ns) stimulus in well-tap engineered structure for (a) and (c) lower stress level (Q = 0.8 × 8.52e-9 C) and (b) and (d) higher stress level (Q = 1.4 × 8.52e-9 C). Well-tap engineering improves the turn-on uniformity. It should be noted that the substrate contact is here shown on the left side of the contour to previous contours depicted. This is to highlight the STI and hotspot from the front view.

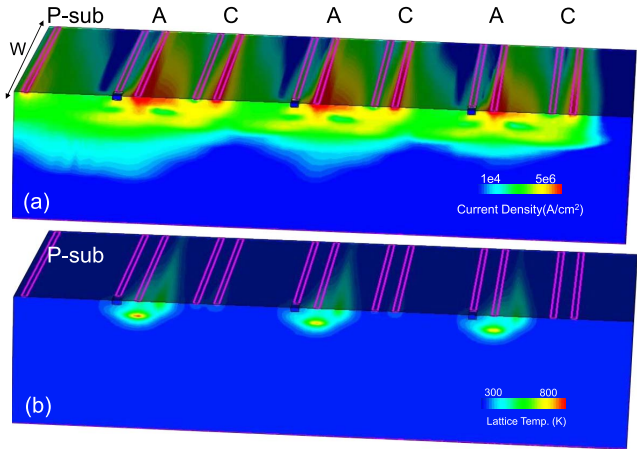

Fig. 12. (a) Conduction current density (A/cm^2) and (b) lattice temperature (K) extracted at the end of fast (RT = 10 ns) stimulus for 50-μm-wide finger structure.

to be added for the positive stress. It is worth highlighting that the increasing finger width to 50 μm does not require a larger well-tap blocking area to obtain uniform finger turn-on. Fig. 12 shows the conduction current density and lattice temperature for 50-μm-wide structure with 3-μm well-tap blocking under fast pulse stimulus. All the fingers can be seen carrying uniform current despite increasing finger width using the same well-tap blocking length. In other words, multifinger turn-on uniformity does not depend on the finger length.

VI. Conclusion

Air-discharge-related failures during system-level IEC stress conditions in Bi-Di silicon controlled rectifiers (BDSCRs) are found to be highly sensitive to stress rise time. The BDSCR device was found to pass ultrafast (RT = 5 ns) and ultraslow (RT = 50 ns) stress pulses. However, BDSCR surprisingly failed during fast stress pulses with a rise time of around 10 ns. 3-D TCAD simulations show that a uniform turn-on of all fingers was achieved under very fast stimulus, which is due to high di/dt. Larger ramp rate in the case of very fast stimulus results in a higher displacement current across different fingers. The displacement current and avalanche-induced current help trigger the fingers rather uniformly and avoid early filamentation or hotspot formation causing failure. However, for the fast pulse stimulus with rise time around 10 ns, only a few fingers could trigger, causing higher current density in those fingers leading to early device failure. The process variation across different fingers forces only a few fingers to trigger in the absence of enough/required displacement current. The same was also true for the ultraslow stress pulses; however, a smaller stress current (i.e., injected displacement current) allowed the BDSCR to survive nonuniform turn-on. Finally, we have shown from 3-D TCAD simulations of a large multifinger BDSCR cell that by selective blocking of p-well tap at the finger edges, uniform BDSCR turn-on of all the fingers can be achieved independent of pulse/stress rise time. Well-tap blocking at the edges increases the resistivity of the p-well tap, forcing BDSCR to trigger faster in case of a lower displacement current, allowing the BDSCR fingers to trigger uniformly.

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