Design Insights to Address Low Current ESD Failure and Power Scalability Issues in High Voltage LDMOS-SCR Devices

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Abstract— **Power-scalability issues for longer pulse duration discharges (PW>100ns) in high voltage LDMOS-SCR devices is evaluated. The severity of the problem with increasing LDMOS voltage classes is highlighted with a need for newer design strategies. A systematic design approach is presented to evaluate the effect of different design parameters on LDMOS filament and SCR turn-on near the snapback region. Finally design guidelines are presented to improve the power scalability without compromising on its ON-state DC (functional) and Safe Operating Area (SOA) characteristics.**

Index Terms—Electrostatic Discharge, Laterally Double Diffused MOS (LDMOS), Silicon Controlled rectifier (SCR).

I. Introduction

LDMOS devices used in System on Chips are prone to early ESD damages [1-3]. The self-protection concept can be implemented in high voltage I/Os by forming a parasitic SCR within the LDMOS device (LDMOS-SCR) [4-6]. LDMOS-SCR device should be able to operate in LDMOS mode during functional operation of the I/O, and in HV-SCR mode during ESD events [4]. In automotive environment, LDMOS-SCR devices can experience discharge pulses that are longer (>500 ns typically) than the on-chip level qualified pulse widths [7]. These long discharges at IC pins can be a result of system RC lines. Hence, the on-chip LDMOS-SCR devices need to survive pulse widths longer than 100ns and should provide non zero failure current. However, recently it is found that LDMOS-SCR designs are susceptible to low current failures, for pulse widths beyond 100 ns [7-8]. The physical insight into such a failure is presented in [8] along with design techniques to overcome such a failure [9]. However, as the LDMOS operating voltage is pushed to higher and higher voltage, the power scalability problem can become a big bottleneck to implement SCR in LDMOS process. As the voltage class increases (e.g. from 40V to 80V, as explored in this work) design approaches proposed in [9] was found to be insufficient and HV LDMOS-SCR do not follow the wunsch-Bell characteristics [10]. In this work we have tried to bridge this gap and develop deeper design insights to improve power scalability independent of voltage class.

II. The Power Scalability Problem

Two different LDMOS-SCR (Fig. 1a) with voltage class of 40V & 80V are studied to understand the severity of the power scalability problem as function of voltage class. The

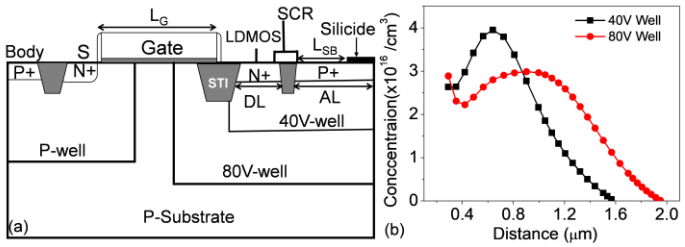

Fig. 1: (a) Cross-sectional view of LDMOS-SCR. To extract intrinsic LDMOS characteristics of LDMOS-SCR design, P+ (in N-Well) terminal was left floating. (b) Doping profiles of two different wells used in this work for obtaining 40 and 80 Voltage classes.

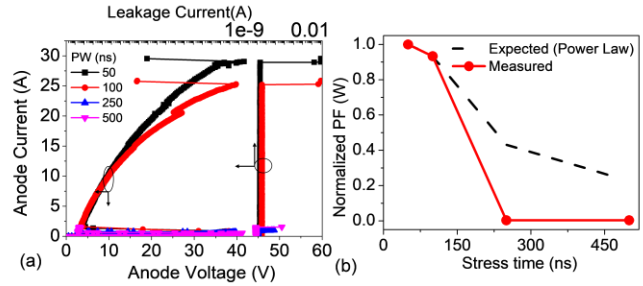

Fig. 2: (a) Measured TLP I-V characteristics LDMOS-SCR device for different stress pulse widths along with leakage data. (b) Normalized power to failure as a function TLP Stress time. Device stressed beyond 100ns duration are observed to fail during the snapback. Note that these TLP measurements are performed with the high impedance Setup that causes the SCR to experience the current values near snapback.

40V well has higher N-well doping than the 80V well (Fig. 1b). 80V LDMOS also consists of 40V well underneath the N+ drain for improved DC on-state performance. LDMOS-SCR devices were found to survive sub 100ns pulses (Fig. 2a), however were found to fail during the snapback for PW>100ns, causing abrupt collapse in power handling capability (Fig. 2b). 3D TCAD characteristics (Fig. 3a) shows temperature near snapback exceeds the critical temperature at larger pulse stress time. The transient temperature (Fig. 4) reveals that filament formation in the intrinsic LDMOS results in abrupt increase in lattice temperature causing early device failure for current values near the device snapback (Fig. 5b & 5c). However, when stressed at higher current

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levels, the

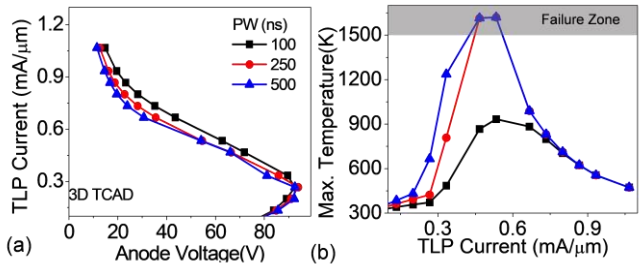

Fig. 3: Simulated 3D TCAD simulated (a) TLP I-V (b) Maximum temperature plotted as a function of current for different pulse widths. Temperature near snapback increases beyond critical temp for PW>100ns.

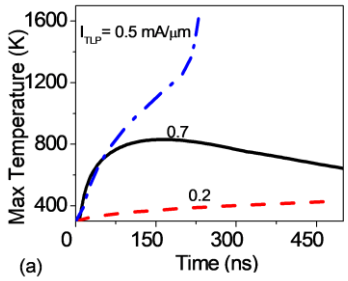

Fig. 4: Simulated transient temperature plotted as a function of stress time for different injected current near the snapback. Lower current values temperature increases linearly with time. For moderate current values near snapback, the lattice temperature abruptly increase and reaches the critical temperature for device failure, however device is found to survive the higher current levels with reduction in temperature beyond a peak value.

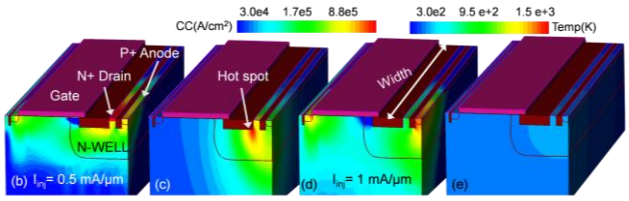

Fig. 5: Conduction current density (b & d), Lattice temperature (c & e) for ITLP of 0.5 and 1 respectively. The temperature shoots up attributed the LDMOS filament for current of 0.5 (b & c). However, for larger current SCR turn-on (d & e) and filament spreading causes safe conduction.

peak temperature falls significantly, attributed to SCR turn on (Fig. 5d & 5e), making the device to survive high current stress. At much higher stress levels the SCR current spreading was seen in the full device width and device is not vulnerable for filament formation until the eventual it2 point. It is worth highlighting that the TLP measurements with 50-ohm load line cannot capture this failure at low currents, as the snapback current is much higher and such measurement bypasses the currents where SCR is vulnerable for device failure [8]. The physical events that are responsible for LDMOS_SCR low current failure near snapback region are summarized in the flow chart in fig.5.

III. Design Issues in Higher Voltages classes

From physical events summarized in Fig. 5, it is evident that, the key design goals should be (i) stronger SCR and (ii) Weaker intrinsic LDMOS. It is worth mentioning that the term strong SCR action refers to increase in N-P-N and/or P-N-P strength and their efficiency, weaker LDMOS refers to the reduction in LDMOS efficiency to collect carriers from N-well.

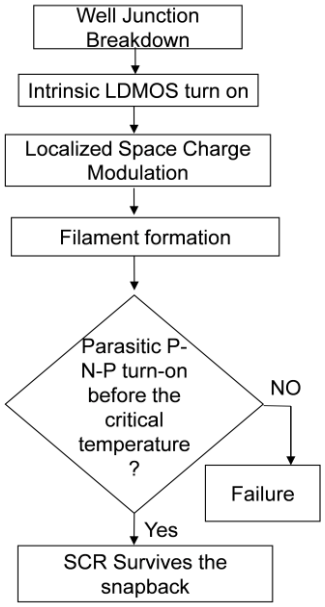

Fig. 6: Flow chart summarizing the Series of physical events that occur in LDMOS-SCR, that are critical for understanding the Power Scalability problem.

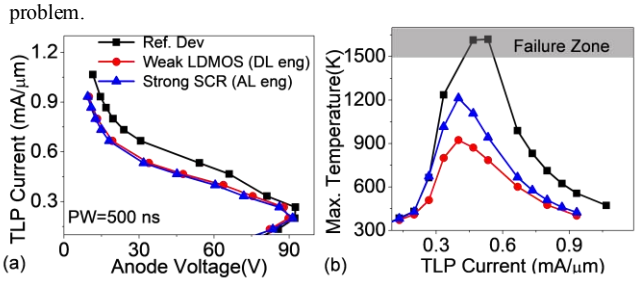

Fig. 7: simulated (a) TLP I-V (b) Maximum temperature plotted as a function of current for 40V LDMOS_SCR devices with AL and DL engineering. Increasing AL (emitter of P-N-P) improves SCR action and reducing DL Weakens the LDMOS action. Peak temperature can be safely limited below Critical value and hence power scalability is achieved.

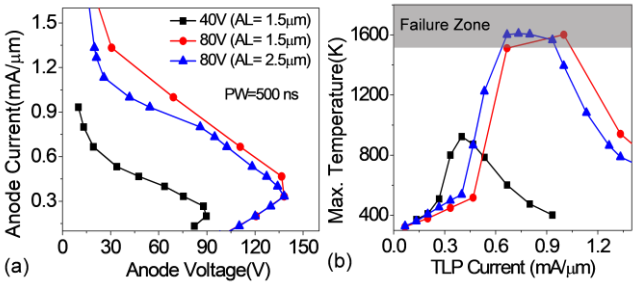

Fig. 8: (a) TLP I-V characteristics of 40V and 80V LDMOS-SCR devices (b) Max Lattice temp plotted as a function of injected current. Minimum DL (0.5 μm) is being used. The 80V LDMOS-SCR has severe power scalability problems compare to 40V designs and Increasing AL (5X) will not be enough for the safe snapback at higher PW.

1)P+ anode (AL) and N+ Drain (DL) engineering: length of P+ region (AL) in N-well defines the emitter area for inherent P-N-P. Increase in AL, increases emitter efficiency of parasitic P-N-P, this inturn boosts the P-N-P strength and the

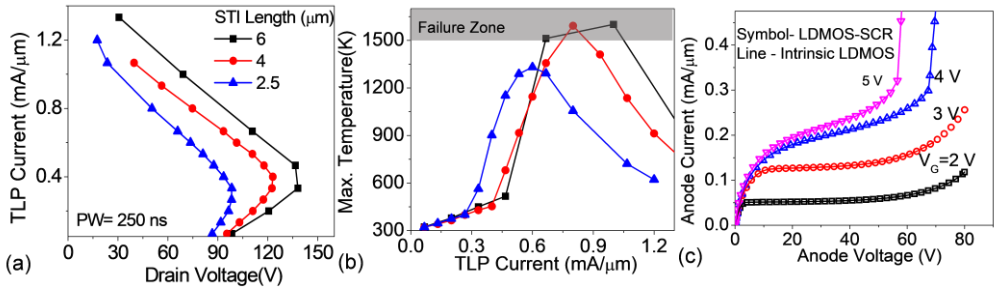

Fig. 9: TLP I-V characteristics LDMOS-SCR for different STI lengths (b) Lattice temperature plotted a function injected current. Reduction in STI length reduces It1, Vt1 and causes early filament formation. However, the smaller operating voltage attributed to reduced anode cathode distance, ensures that self-heating in filament do not reach critical temperature. However, reducing STI length for increasing power scalability has negative implications on on-state performance (Reduction in on-state breakdown voltage).

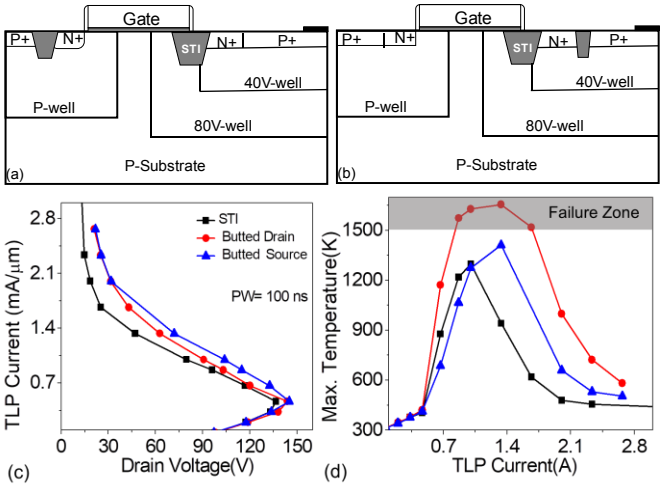

Fig. 10: device Cross-sections for Butted (a) Drain (b) Source. (c) Simulated (3D) TLP I-V characteristics LDMOS-SCR with STI isolation, butted configurations at source and drain. (d) Lattice temperature plotted a function injected current. Butted configuration at drain degrades P-N-P turn on, and at source slows down N-P-N, causes severe power scalability problems. The lattice temperature reaches to critical temp. Even with 100 ns Stress.

SCR action, causing device to survive snapback (Fig. 7b). the device with AL engineeering in 40V LDMOS-SCR found to limit the lattice temperature below the crictical value and hence device surives the failure, power scalability can be achived. On the other hand, reduction in DL weakens the efficiency of LDMOS in collecting electrons from N-well. The accumulation of electons in the N-well helps in turning the P+ and N-well diode earlier and makes SCR to trigger faster; This will result in SCR taking over the conduction before the temeprature in filament reaches critical value , resulting in improved power scalability in 40V deigns (Fig. 7b).

2)Why to revisit the design approch for higher voltage classes?: Implementing fast SCR in higher voltage classes is challenging attributed to longer drift lengths. The long drift length implies that longer Anode-cathode distance. The power scalability for higher voltage LDMOS-SCR designs becomes an issue due to reduced SCR strength attributed to larger drift length. It is observed that AL and DL engineering appraoches, though reduces low-current failure current window in 80V designs, but do not gauranty safe snapback. By using minimum DL (to ensure on-state breakdown is intact), Increasing AL even by 5× in 80V devices (opposed to 3× increase in 40V LDMOS-SCR), found to have limited improvement as depcited in figure 8. Hence, it is required

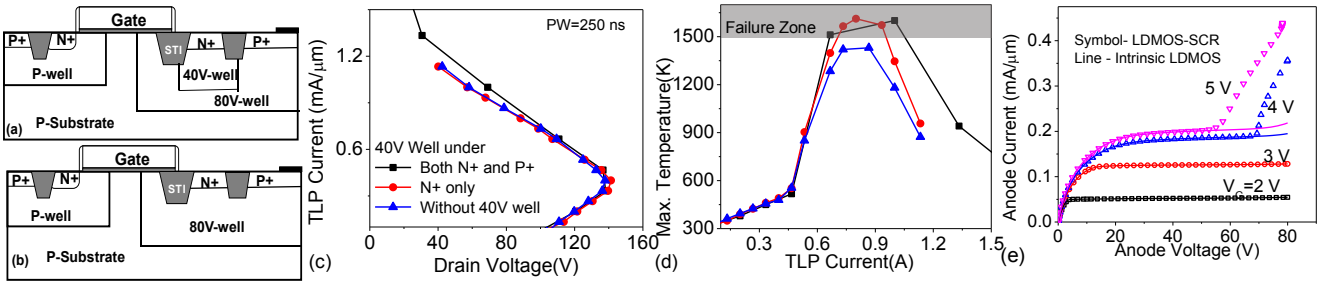

Fig. 11: Device cross-section of 40V Well profile changes (a) Underneath only N+ (b) W/0 40V well (c) LDMOS-SCR TLP I-V characteristics and (d) Maximum Lattice temperature vs injection current for different 40V well placements inside 80V well. 40V well increases the doping near the surface in the 80V well. If it is under both N+ & P+, yields worst case condition with larger failure window. 40V well under only N+ though reduces the failure window; cannot improve the power scalability. If 40V well is not implanted the failure window disappears for 250 ns PW, improved Power scalability but causes strong SCR action in the on-state (e)

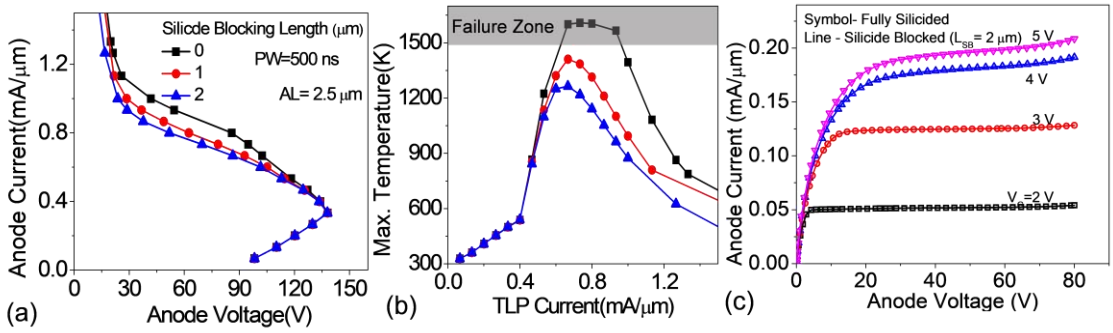

Fig. 12: (a) TLP I-V Characteristics of LDMOS-SCR (b) Maximum Lattice temperature plotted as function Silicide blocking length. Increasing Silicide Blocking on P+ found to reduce the lattice temperature, during snapback. Improvement in power scalability with silicide blocking is purely a 3D phenomenon, the peak lattice temperature from 2D Simulations do not change (data not shown). (C) DC I-V characteristics showing no influence on on-state characteristics.

to develop unified design insights independent of voltage class. Following are the key learnings:

(a) STI length: larger STI length requirements in higher voltage classes weaken the parasitic P-N-P. Reducing STI length (Fig. 9) reduces device operating voltage after breakdown (reduced Vt1, It1) which mitigates the self-heating inside the LDMOS filament. Reduction in STI length implies smaller base length for parasitic P-N-P and stronger P-N-P action ensures SCR turn-on before LDMOS filament causes stronger hotspot. This improves the power scalability; however there will be tradeoff with on-state device breakdown (Fig. 9c).

(b) Source/Drain side butting: Butted contacts in HV LDMOS-SCR is found to cause severe power scalability problems (Fig. 10). Though, butted contacts do not significantly influence intrinsic LDMOS filament nature, carrier recombination in the butted region near anode slows down P-N-P and hence weak SCR action. This will cause intrinsic LDMOS failure even for 100ns pulse width. Source side butting though slows down N-P-N turn on, its influence on power scalability found to be very limited. In general, body of the LDMOS is butted to the source to reduce weaken the N-P-N action in LDMOS, hence the higher ESD robustness is achived. But this can be killer for LDMOS-SCR devices. As the weaker N-P-N action implies that, reduced supply of electrons for the P-N-P to turn on and hence device conducts in the filament mode and eventual fail. Same applies to butting at the drain side.

(c) 40V well implant: 40V (high doping) N-well when implanted in (low-doping) 80V N-well, under anode/drain region, was found to have negative impact on the power scalability (Fig. 11). Presence of highly doped well beneath anode reduces base resistance of P-N-P, causing increased hole recombination in the base of P-N-P. This results into week SCR action. Improved power scalability is observed without the 40V well (Fig. 11). If implanted only under N+, the failure window gets narrowed; however the low current failure cannot be avoided. On the other hand, removing 40V well, causes SCR turn on in the functional region (Fig. 11 c).

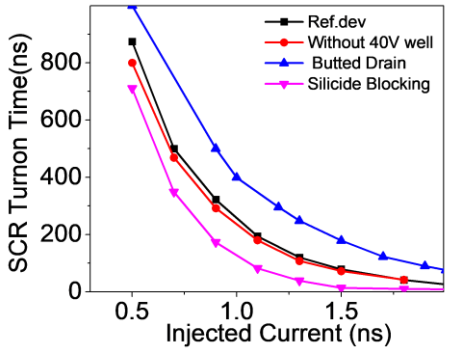

Fig. 13: SCR Turn-on time a function of injected current, for different designs under Investigation. Drain side butted configuration shows slowest SCR turn on and worst power scalability behavior. Whereas Silicide Blocked on AL shows fastest SCR turn on and best power scalability trends.

(d) Anode Length (AL) Engineering with Silicide Blocking: Increasing AL found to improve emitter efficiency of PNP, however it saturates soon as only a portion of anode region next to STI conducts the current. Hence, AL engineering do not reduce the failure current window in 80V design. However, silicide blocking over anode was found to improve the power scalability (Fig. 12). Lattice temperature near snapback region gets reduced with increasing silicide blocking length. Silicide blocking on P+ anode causes improved SCR turn-on inside the filament region. As a result the entire anode region conducts, which accelerates the current spreading outside the filament before failure. The mitigation of heat with silicide blocking is purely 3D in nature and cannot be observed in 2D simulations. The silicide blocking together with AL engineering found to provide best possible solution for power scalability problems for higher voltage classes, which also do not cause SCR turn-on during MOS operation (Fig. 12c). Fig. 13 shows butted drain device has the slowest SCR and provide worst power scalability trends. However, AL engineering plus silicide blocks results in fastest SCR turn-on and robust power scalability behavior (Fig. 14). Influence of various design parameters on power scalability and DC operation as well as SOA behavior are summarized in table-I

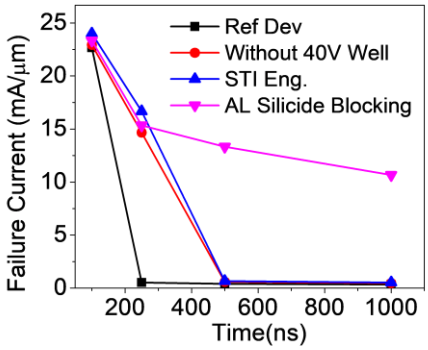

Fig. 14: Final Power Scalability trends for different designs Investigated.

Design Parameter	Effect on Power scalability	SOA/SCR turn on in DC functional region
P+ Anode Length ↑	☺☺	☺
N+ Anode Length ↓	☺☺	☺
STI Length ↓	☺	☹☹
Butted at Drain	☹☹	☺
Butted at Source	☹	☺
40V well under Anode	☺	☹
Silicide Blocking on AL	☺☺☺	☺☺☺

Table-I: Summary of Design guidelines.

IV. Conclusion

Anode length engineering and drain length engineering techniques that solve the power scalability issues in lower voltage classes (40V SCR), won't be enough for safe snapback at higher voltage classes (80V). The severity of the problem attributed to longer drift lengths in high voltage classes, that weakens the P-N-P and hence SCR turn-on. Increasing AL for higher emitter efficiency also have limitation as only a portion of AL conducts the SCR current. Reducing STI length found to improve the power scalability but on-state breakdown voltage is impacted. Butted configurations at drain yields worst power scalability trends as the SCR weakens attributed to carrier recombination in the butted region. Silicide Blocking with AL engineering was found to give the best possible power scalability trends without impacting the MOS functional and SOA characteristics.

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