First Insights into Electro-Thermal Stress Driven Time-Dependent Permanent Degradation Failure of CVD Monolayer MoS_2 Channel

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***Abstract*—This work reports, for the first time, time dependent degradation and failure of CVD monolayer MoS_2 based field-effect transistor channel under DC voltage stress, which seem to have originated from its unique molecular description. Degradation was found to be permanent, which takes place at fields lower than critical field for breakdown and have been discovered to be a strong function of channel temperature and e-field. Strong dependence of channel current on self-heating across the channel has also been observed, which resulted in significant drop in channel current under stress, which however recovers when stress was removed. Reversal in degradation trends and permanent channel failure was observed at lower (77–150K) channel temperatures. Unique localized low resistance regions as well as field assisted physical damage result in overall (ON and OFF state) performance degradation of MoS_2 transistors. Micro-Raman and Photoluminescence investigations, as a function of stress time, are performed to investigate the micro-origin of permanent degradation and failure.**

***Index Terms*—Transition Metal Dichalcogenides (TMDs), CVD MoS_2.**

I. Introduction

ALONG with the remarkable properties of 2D materials, especially MoS_2, improved material growth and process techniques have fueled the demand for replacing Silicon with 2D Transition Metal-Dichalcogenides (TMDCs) for future logic applications. Extensive research on contact engineering and doping techniques [1], [2] have significantly brought down the contact resistance (R_C) of TMDC based FETs (a major bottleneck in the 2D FET technology), however, R_C as low as that in case of Si MOSFETs is yet to be achieved. Moreover, device circuit design techniques driven by reliability investigations on 2D material based transistors is imperative for technology development. Apart from Graphene [3], electrical stress-dependent 2D transistor reliability has not been extensively considered so far. In this work, we present a systematic investigation on temporal response of CVD monolayer MoS_2 FETs to a constant voltage stress at different ambient temperatures. Moreover, effect of voltage stress on device performance and on the material configuration has been elucidated.

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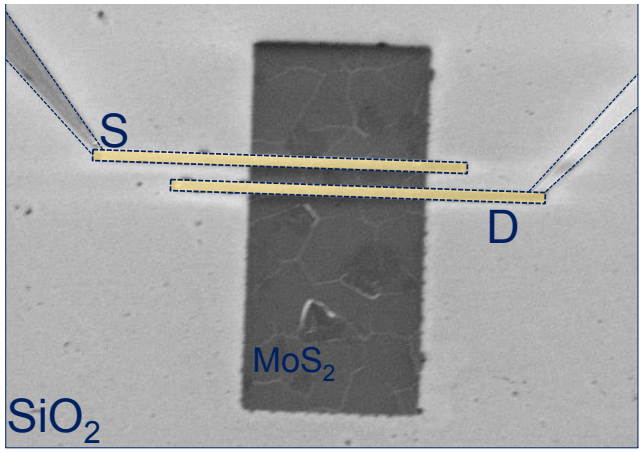

Fig. 1. SEM image of back-gated transistor fabricated on 90nm SiO_2 substrate

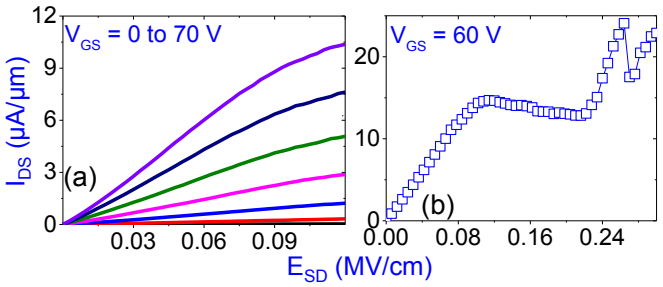

Fig. 2. (a) Current saturation observed at V_{DS}=12 V and V_{GS}=70 V. (b) In order to run time-dependent measurements, 0.2 MV/cm is taken as the upper limit for stressing the devices. L_{ch} = 1μm. EOT = 90 nm.

II. Experimental Details

For the explorations presented in this work CVD monolayer MoS_2 based back-gated FETs (Effective oxide thickness, E_{OT} = 90nm) were realized using the following process flow: transfer of CVD monolayer MoS_2 on 90nm thick thermally grown SiO_2 on highly doped Si substrate; channel definition using etching of MoS_2 by Oxygen plasma; Lithography for source/drain contact patterning; metal deposition inside E-beam evaporator; metal lift-off; vacuum annealing at 520 K. All measurements were performed in vacuum. It is observed that the drain current in realized MoS_2 FETs saturate around E_{SD} = 0.09 MV/cm for V_{GS} = 70 V (Fig. 2a). Further, no change in current is observed till E_{SD} = 0.2 MV/cm, whereas a sharp increase in drain current can be seen at E_{SD}

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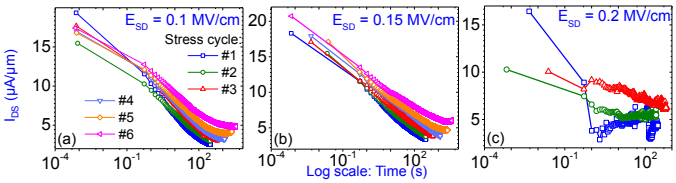

Fig. 3. Time-dependent current decay for different Sfield stress at T=300K, V_{GS} = 60 V. (a, b) decay in current with time due to electron-phonon scattering. Current at the end of every stress is higher than that after previous stress. This implies the dependence of channel current on stress time. (c) Abrupt variation in current at higher field.

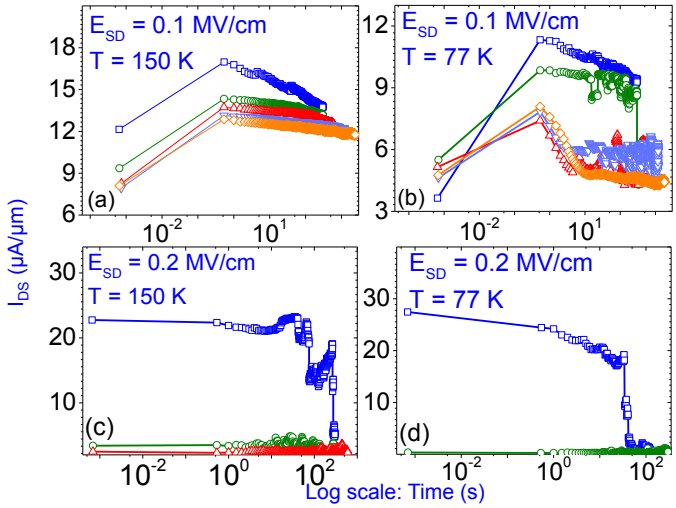

Fig. 4. (a,b) at lower temperature, Current rises initially and then falls. This is attributed to increased thermionic emission of carriers at the contacts due to heat propagation towards the channel. (c,d) At higher field and lower temperature, less number of scattering events occur due to which electron elastically collides with the lattice thereby inducing more damage to the lattice.

= 0.24 MV/cm at V_{GS} = 60 V (Fig. 2b). Keeping this limit in mind, the devices were stressed at E_{SD} 0.2 MV/cm as a function of time for temperature ranging from 77K–300K. After every stress cycle, I-V (at low voltages), Raman and PL characteristics of the devices are extracted.

III. Results Discussion

A. Electro-thermal transport

It is observed that, after an initial abrupt fall, the current monotonically decays with time and saturates at 100s, when stressed at E_{SD} = 0.1 MV/cm (Fig. 3a). Similar temporal behavior is observed when the stress field is increased to E_{SD} = 0.15 MV/cm (Fig. 3b). However, at sufficiently high E_{SD} (= 0.2 MV/cm), observed current decay is highly abrupt unlike for lower E_{SD} values. An initial abrupt fall followed by a monotonic decay leading to saturation is attributed inelastic scattering of electrons with lattice, which increases the phonon population and in turn degrades channel current. This process eventually saturates when a thermal equilibrium is established between the lattice and the electrons where the rate of scattering equals the rate of heat transfer across the lattice. At higher E_{SD}, electrons gain relatively higher energies before electron scatters elastically with the lattice, which results into

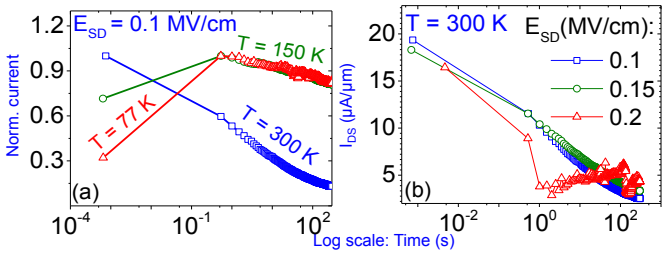

Fig. 5. Comparison of current decay curve at various temperatures (a) and E_{SD} (b).

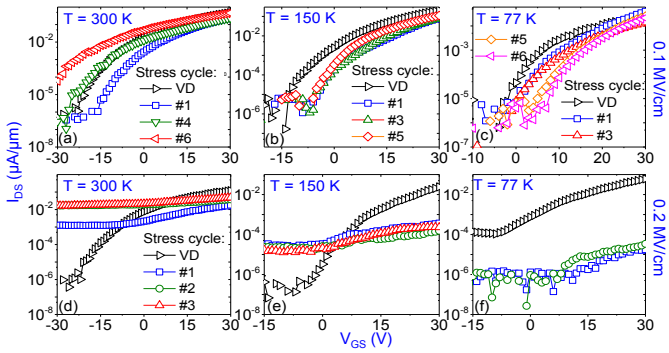

Fig. 6. Transfer characteristics after multiple stress cycles and at different temperatures. (a-c): Positive shift in V_{TH} followed by negative shift after a certain number of stress cycles. Significant shift is observed at lower temperatures. (d-f) At higher E_{SD}, the OFF as well ON state performance degrade due to stress-induced localized charge carriers and physical damage to the lattice.

increased phonon population, as well as physical damage to the lattice. The physical damage becomes more pronounced at lower temperatures (¡150K) due to increased mean scattering length (Fig. 4), which allows electrons to gain a higher energy before they scatter. Lower population at lower temperature increases probability of elastic collisions, i.e. less heat transfer and an increased damage to the lattice (Fig. 5). It is important to note that, initial rise in current for E_{SD} = 0.1 MV/cm and T=150, 77 K, is due to heat propagation from the channel to the contacts which facilitates increased thermionic injection across the source-channel barrier [4].

B. Electrical stress-induced device failure

It is interesting to know that the thermal equilibrium point after each stress shifts upwards at 300 K (Fig. 3). This is counter intuitive because long-term electrical stress is expected to damage the lattice more and hence shift the thermal equilibrium point downward after every stress cycle. Unlike at T = 300 K, downward shift of this saturation current (I_{sat}) is observed in devices stressed at lower temperatures (Fig. 4). Moreover, it is observed in the transfer characterisitcs of devices stressed at 0.1 MV/cm at 300 K that VTH undergoes a positive shift followed by a negative shift after 5th stress cycle wihtout remarkable change in the ON state performance. Similar trend is observed at lower temperatures (Fig. 6b, 6c). However, for ESD = 0.2 MV/cm, both OFF and ON state performance degrade with increasing number of stress cycles.

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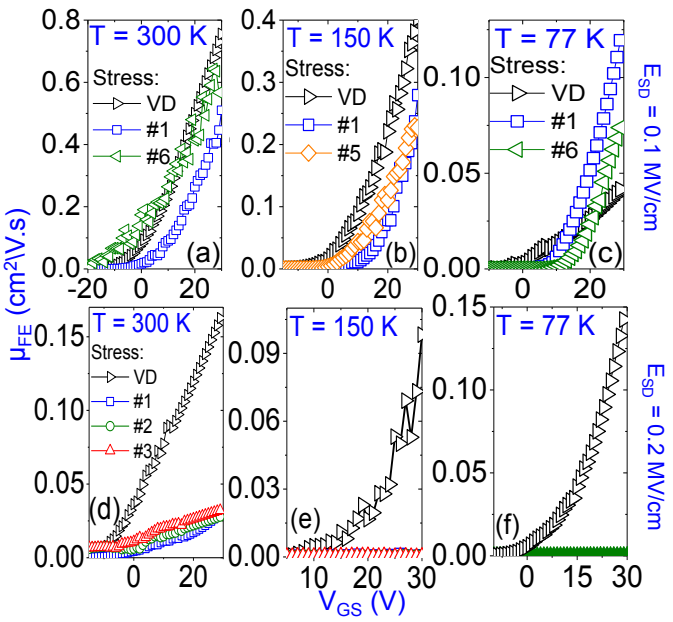

Fig. 7. (a-f) Subsequent fall in mobility is observed with increasing number of stress cycles at low as well as high temperature.

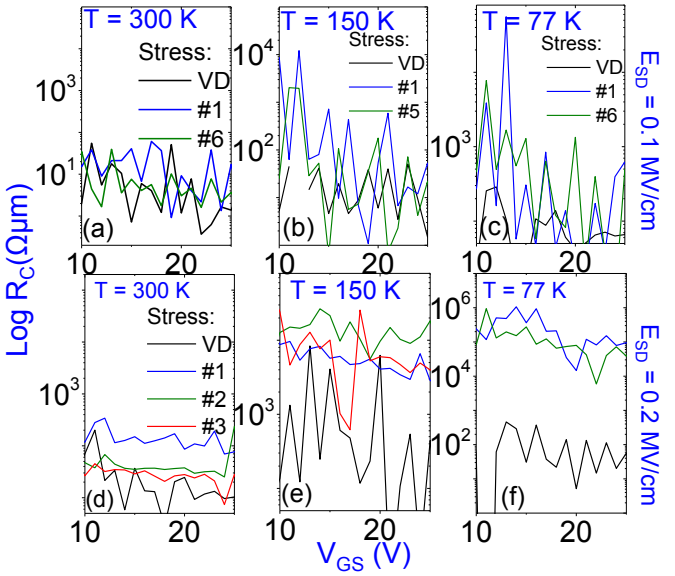

Fig. 8. (a-f) Reduction in R_C in the OFF state after higher field stress signifies enhanced hole injection.

Decrease in ON state current is attributed to physical damage of the lattice, as discussed above. Unlike in Fig. 6(d), this is observed in Fig. 6(e, f) where stress is applied at 150 K and 77 K. Increased OFF state current and negative shift in V_{TH} imply change in the channel properties, possibly due to introduced donor states attributed to Sulphur vacancies, that makes it more conductive in the sub-threshold regime and OFF state.

This is in good agreement with observed upward shift of I_{sat} in the temporal response of the device with increasing number of stress cycles. Degraded OFF state performance is complemented by mobility and contact resistance (Fig. 7

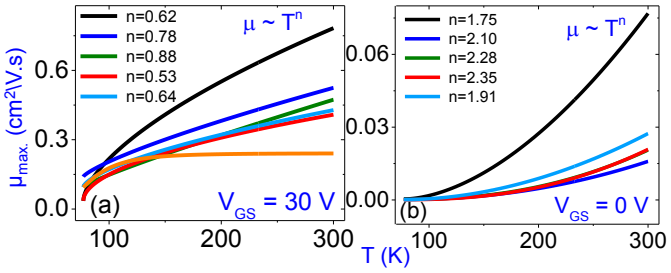

Fig. 9. Temperature dependence of mobility in two different device operating regimes- ON state and sub-threshold region.

8). These results suggest the following: impact of physical damage dominates in the ON state and unique localized material degradation enhances the OFF state current. Temperature dependence of is observed to have reduced in ON state (Fig. 9) with stress cycle. Fig. 10 and 10 show significant change in the contact properties, which changes from ohmic to schottky. This further signifies physical damage to be present across channel/contacts.

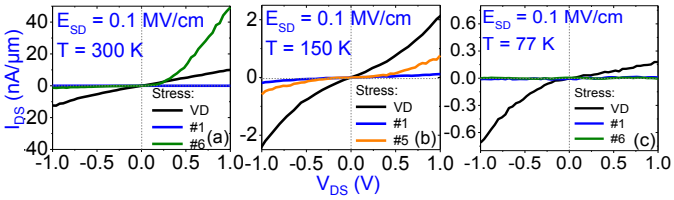

Fig. 10. I_{DS} at gate open condition. Channel resistance has decreased for device stressed at 300K due to temporal stress. This is counter-intuitive because temporal electrical stress is expected to increase channel resistance. VD=Virgin Device.

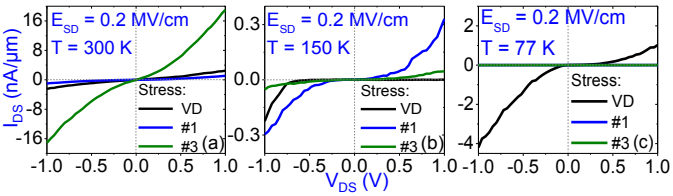

Fig. 11. I_{DS} at gate open condition for devices stressed at E_{SD} = 0.2 MV/cm.

C. Electrical stress-induced material degradation and its impact on device performance

A red shift in the A_{1g} phonon mode in the Raman spectra (Fig. 12) implies enhanced electron population in the channel when device was stressed at room temperature [5]. In the same device, PL spectra (Fig. 13) reveals higher intensity of the negative trion peak which is a result of enhanced electron concentration in the channel after 6th stress. These results clearly elucidate the fact that MoS_2 channel does enter a low resistance state, which is attributed to creation of S vacancies and its migration towards hot electrode [6], which makes MoS_2 more conductive than the virgin MoS_2 channel in the OFF state.These results are similar to those observed in MoS_2 based memristors [7]–[9] and hence are attributed to migration of S vacancies under electrical stress.

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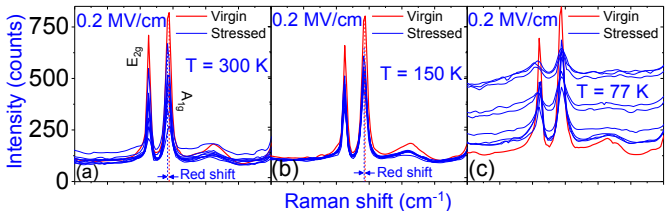

Fig. 12. Raman spectra comparing peaks of virgin and stressed regions. A red shift implies increased electron concentration and hence validates the presence of stress-induced localized regions with excess electrons. Moreover, significant reduction in peak intensity, especially after stress at 77K, implies more physical damage to the lattice.

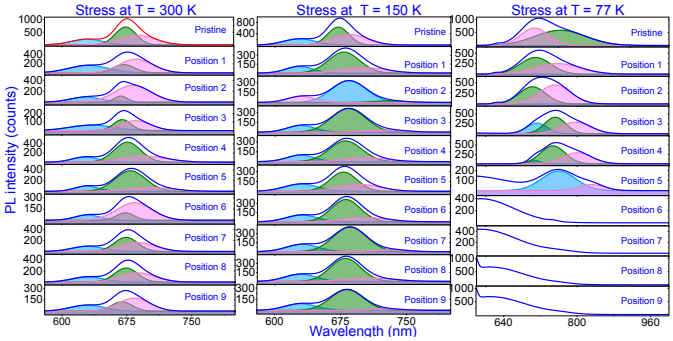

Fig. 13. PL spectra comparing peaks of virgin and stressed (E_{SD} = 0.2 MV/cm) regions. Increase in the negative trion energy peak intensity (pink curve) implies increased electron concentration and hence validates the presence of stress-induced localized regions with excess electrons. Different positions are positions are positions along the width of the device (spaced apart by 1μm spacing). (Green: A exciton, Blue: B exciton and Pink: A-trion.)

IV. Conclusion

MoS_2 continues to exhibit yet another fascinating behavior wherein it enters a high resistive state after first few electrical stress cycles and eventually collapses in a low resistance state under certain stress conditions which include E_{SD}, temperature, number of stress cycles and stress time. This is a unique behavior of a transistor channel material to possess and different than conventional (Si) FETs, which fail or degrade on stressing by achieving a high resistance state. Moreover, it is observed that two mechanisms; physical damage and change in material property to a low resistance phase at localized regions in the channel take place simultaneously. It is expected that this behavior is inherent to MoS_2 like materials because of their atomic arrangement similar to metal oxides.

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