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Superior resistance switching in monolayer MoS₂ channel-based gated binary resistive random-access memory via gate-bias dependence and a unique forming process

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Abstract

Resistance switching (RS) in 2D molybdenum disulfide (MoS₂) was recently discovered. Since the discovery, many reports demonstrating MoS₂ resistive random-access memory (RRAM) with synapse-like behavior have been published. These reports strongly justify applications of MoS₂ RRAM in neuromorphic hardware as well as an alternative to conventional binary memories. In this work, we unveil the effect of RS, induced by current–voltage hysteresis cycles across CVD-grown monolayer MoS₂-based gated RRAM, on its transistor's electrical and reliability characteristics. A unique gate voltage dependence on the RS is identified which has a remarkable impact on the switching performance of MoS₂ RRAM. RS behavior was found to be significantly dependent on the charge conduction in the channel. Moreover, we have shown a potential device-forming event when MoS₂-gated RRAMs were subjected to a steady-state electrical stress. Both hysteresis and steady-state electrical stress were found to disturb the transistor action of these gated RRAMs, which can in fact be used as a signature of RS. Interestingly, current–voltage hysteresis resulted in unipolar RS, whereas steady-state electrical stress before RS measurement led to bipolar RS. Moreover, successive stress cycles of such electrical stress lead to multiple resistance states, a behavior similar to synaptic properties such as long-term potentiation and long-term depression, typically found in memristors. We find that the charge transport mechanism dominant in the MoS₂ FET, in conjunction with steady-state stress-induced device forming, determine the extent of RS induced in thes MoS₂-based gated RRAMs. Finally, on the basis of insights developed from the dependence on the charge transport mechanism and steady-state stress-induced forming of the MoS₂ channel, we propose a certain steady-state electrical stress condition which can be used as a 'forming' process, employed prior to the use of MoS₂-based binary RRAMs for improved switching performance.

Supplementary material for this article is available online

Keywords: MoS₂, hysteresis, resistance switching

(Some figures may appear in color only in the online journal)

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1. Introduction

In order to reduce device footprint to enhance functionality and storage density [1–4], two-terminal vertically stacked memory devices such as resistive random-access memory (RRAM), etc, have been extensively explored. Trivial device structure along with a unique resistance switching (RS) mechanism in certain materials justifies their potential for memory applications. Phase change memory (PCM) [5], metal-oxide RRAM [6], and spin-torque transfer RAM (STT-RAM) [7], among others, are various devices that have emerged recently as alternatives to silicon-based flash memory. Interestingly, different mechanisms are responsible for the observed RS in these devices. For example, joule heating-induced crystallization and amorphization in PCM, electric field-induced migration of oxygen vacancies resulting in formation of conductive paths in metal oxide RRAMs, and spin-selective current injection-induced change in spin orientation of a 'free-layer' in STT-RAM; these form the basis of next generation memory devices [8]. Currently, there are a plethora of bulk materials that exhibit RS which promise further advancements in the field of semiconductor memory. Moreover, recently observed RS in 2D transition metal dichalcogenides (TMDCs) [9–15] has added another dimension to exploration of TMDCs for RS applications. Unlike bulk RS devices, discussed earlier, RS in 2D TMDCs occurs within an atomically thin film. Continued scaling of memory devices along with 3D integration can therefore make a further reduction in cost per bit plausible. Sangwan *et al* reported, for the first time, that chemical vapor deposition (CVD)-grown MoS_2 exhibits RS which is mediated by grain boundaries (GBs) [9]. Moreover, such a behavior was found to be gate tunable. In a separate work, they demonstrated spike-time dependent plasticity (STDP), short/long-term potentiation (STP, LTP) and short/long-term depression (STD, LTD), properties essential for neuromorphic applications [10]. Cheng *et al* reported RS in 1 T metallic phase vertical MoS_2 devices followed by demonstration of an odd-symmetric memristive device by stacking two 1 T phase MoS_2 devices back-to-back [11]. Vertical memristors on monolayer TMDCs were reported by Ge *et al*, the first demonstration of RS at sub-nanometer dimensions [12]. Arnold *et al* also captured LTP in MoS_2 transistors via hysteresis engineering [13]. Krishnaprasad *et al* fabricated CVD-grown MoS_2/graphene memristors which exhibit not only basic properties such as STP/STD, LTP/LTP and STDP but also a linear synaptic weight update, thereby making them suitable for use in hardware for unsupervised learning [14]. Another report on ion-based plasticity of MoS_2 memristors by Belete *et al* suggests the role of OH^- ions RS observed in MoS_2 devices [16]. Besides RS, a 2D-material based floating gate (FG) memory cell was demonstrated by Paul *et al* with MoS_2 as the transistor channel, graphene as the FG and hBN as tunneling oxide (TO). These devices were fabricated on a truly 2D platform and exhibited excellent data retention and endurance [17]. These reports suggest that MoS_2 does exhibit RS and other key behavioral traits that justify its importance in binary memory applications and neuromorphic computing hardware implementation.

In order to observe RS in any material, a current–voltage hysteresis curve is typically obtained. Once a material exhibits RS, the two possible states (in the case of binary memory devices, low resistance state (LRS) and high resistance state (HRS)), are revealed from their hysteretic behavior. (This does however need to be established via a suitable voltage sweep in a particular direction.) In other words, a current–voltage hysteresis operation induces RS in all two-terminal RRAMs. While every report on RS attempts to elucidate the fundamental mechanism behind RS along with the changes it induces in the material, very few reports discuss the impact of RS on the device behavior from an electrical point of view. Moreover, besides hysteresis, other methods to induce RS are unknown. This is precisely what we intend to address in this work. We investigate the impact of current–voltage hysteresis-induced RS on the transistor behavior of CVD-grown monolayer MoS_2 devices. Further, we identify this change in transistor behavior to be similar to a phenomenon observed earlier [18, 19] in which a steady-state DC electrical stress induces negative shift in the threshold voltage (V_T) and poor gate control. Hence, it is speculated that such a long-term electrical stress (LTES) also induces RS in MoS_2. To materialize the anticipated RS phenomenon, we observe how the polarity of an LTES affects the device behavior. It turns out that the channel resistance attains two different states, LRS and HRS, depending upon the polarity which manifests as bipolar RS in our devices. These results elucidate how RS affects the transistor behavior and clearly justify the fact that besides current–voltage hysteresis, an LTES is another way to induce RS in CVD-grown monolayer MoS_2. Both hysteresis and LTES result in a peculiar transistor behavior which can be used as a signature for RS. Based on the gate voltage-dependence of RS observed in our experiments, these findings unveil the possibility of increased density of mid-gap states in MoS_2 after hysteresis and LTES cycles. Such insights also reveal that RS realized during the OFF state operation of a MoS_2 transistor results in superior switching performance which can be further improved using a high voltage formation. Based on these results, we propose a forming process for MoS_2, as in the case of other RS materials [20], which can be used to improve the switching window (SW) and consequently its importance for binary memory applications.

2. Results and discussion

MoS_2 transistors in the back-gated configuration, figure 1(a), are fabricated using the process discussed in figure S1(a) (available online at stacks.iop.org/JPD/55/085102/mmedia). A ~ 19 cm^{-1} of separation between the two characteristic Raman modes (A_{1g} and E_{2g}), as shown in figure S1(b), implies that the devices are fabricated on CVD-grown monolayer MoS_2. A scanning electron microscopy (SEM) top view image of the as-fabricated transistor is shown in figure 1(b). All subsequent measurements are performed inside a vacuum probe station maintained at 10^{-4} Torr.
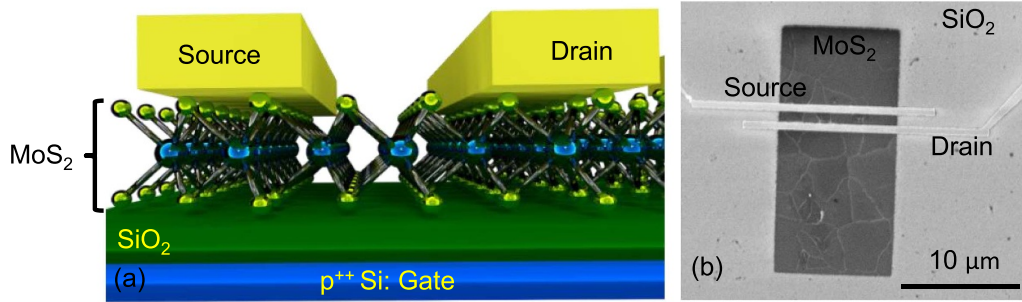
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Figure 1. (a) Back-gated configuration of MoS_2 FETs with channel length, $L_{CH} = 1$ μm and dielectric thickness, $T_{OX} = 90$ nm. (b) SEM top-view of the fabricated FET (scalebar $= 10$ μm).

2.1. Hysteresis-induced RS and its impact on transistor behavior

RS phenomenon in various materials is typically confirmed through the drain-to-source current–voltage hysteresis behavior. Such a behavior is observed when the drain-to-source voltage (V_{DS}) is varied in a 'dual-sweep' mode. This essentially means that the direction of V_{DS} sweep is varied and a RS mechanism manifests as dual-valued resistance (or current) for the same voltage. This is known as hysteresis and is observed in all the devices that exhibit RS [20]. For MoS_2 devices tested during this work, hysteresis is observed only at relatively large values of V_{DS}, as shown in figure 2(a). It is found that the voltage at which RS occurs is different at different gate voltages. For devices in the ON state ($V_{GS} = 60$ V), RS occurs at $V_{DS} = 25$ V whereas for an open gate device and a device in the OFF state (-60 V) RS occurs at $V_{DS} = 20$ V (figure 2(b)). Moreover, RS in devices in the gate open condition and OFF state is found to be abrupt at $V_{DS} = 20$ V. This is not true for devices in the ON state and a gradual transition to an LRS is observed at $V_{DS} = 25$ V. Such an observation is unique as it suggests that hysteresis-induced RS depends on the dominant transport mechanism in the device. It is important to note that minor charge carrier transport during the OFF state and gate floating condition happens through mid-gap states and those which are close to the conduction band minimum (CBM), respectively, with marginal density as variable range hopping at room temperature [21, 22]. It is possible that an abrupt increase in the current during hysteresis may be a manifestation of increased density of states within the bandgap. This is further discussed later in this section. To determine to what extent RS has occurred, two-terminal resistance of the device is measured before and after hysteresis. It is observed that, irrespective of the transport mechanism dominant during hysteresis, the two-terminal MoS_2 resistor, post hysteresis cycle, exhibits higher conductance than a virgin resistor (figure 2(b)). However, the extent to which the device conductance increases does depend on the transport mechanism dominant at the time of hysteresis. A remarkable 180% increase in the two-terminal conductance is observed for the device subjected to hysteresis during the OFF state operation. For the devices in the ON state and close to the threshold regime, the increase in the conductance is found to be 80% and 55%, respectively. These values are extracted from the $I_D V_D$ characteristic, shown in figure

S2, obtained for the two-terminal MoS_2 resistor device. Further insights into the possible impact of hysteresis on MoS_2 are established by obtaining transfer characteristics of MoS_2 FETs before and after the hysteresis event. It is important to emphasize that the transfer characteristics discussed next are of the same devices that presented in figure 2. Moreover, the current observed for the hysteresis of a device in the ON state (the blue curve) is found to be comparable to that of a device in the OFF state, which is not expected. It is important to note that devices are successively tested for hysteresis from a lower V_{DS} to the point at which it exhibits hysteresis. It is found that the current degrades significantly due to successive attempts to observe hysteresis, especially when in the ON state, as shown in figure S2.

InT general, it is found that devices after hysteresis exhibit degraded transistor behavior, which is identified by a huge negative shift in V_T, poor gate control and higher OFF state current (figures 3(a)–(c)). As shown in figure 3(a), a hysteresis cycle during the ON state ($V_{GS} = 60$ V) results in complete loss of gate control and degraded ON state current. Whereas hysteresis at $V_{GS} = 0$ and -60 V leads to significant negative shift in V_T, some loss in gate control and higher ON state current, shown in figures 3(b) and (c). From the transfer characteristics shown in figure 3, it is clear that hysteresis-affected devices exhibit significant charge transport for the complete range of gate bias. As a result, negligible current modulation is observed. These results also suggest the possibility of a hysteresis-induced increase in the density of mid-gap states which contribute to charge conduction when the fermi-level is tuned below the CBM. It can be argued that hysteresis introduces incredibly large density of mid-gap states for which the device exhibits comparable currents in the otherwise distinguishable ON and OFF states. More importantly, this phenomenon occurs irrespective of the state in which the device operates, i.e. independent of V_{GS}. This also explains the observed abruptness in the current hysteresis of devices in the OFF state and in the two-terminal configuration shown in figure 2(a). Prior to hysteresis, the density of mid-gap states is small in a high quality MoS_2 monolayer. As there are no defect peaks observed in the Raman spectra, shown in figure S1(b), it can be inferred that the defect density and hence density of mid-gap states is sufficiently low [23]. Post hysteresis, an extremely large increase in the density of mid-gap
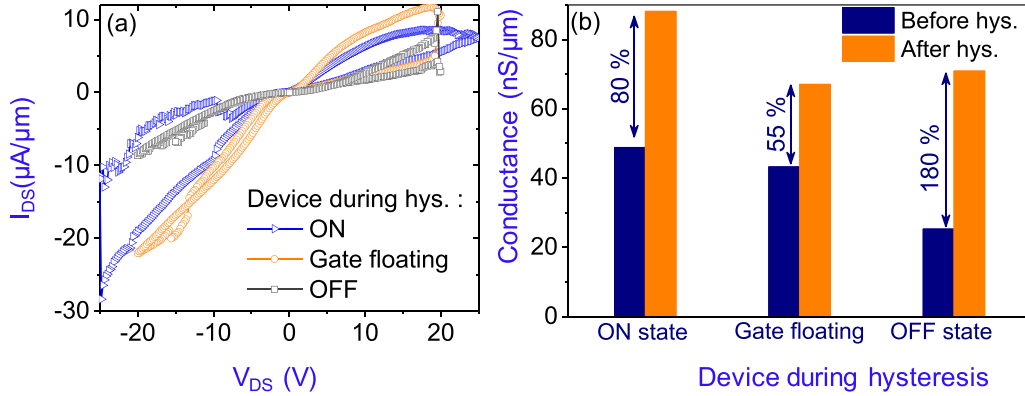
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Figure 2. (a) Hysteresis behavior observed when the transistor is in different operation regimes: ON state ($V_{GS} = 60$ V), two-terminal resistor (gate floating) and OFF state ($V_{GS} = -60$ V). The drain-to-source voltage at which hysteresis occurs depends on which state the device is operated by tuning the gate bias. Hysteresis leads to significant change in material properties which manifests as change in channel conductance which is known as RS. (b) Hysteresis-induced RS in our devices is found to increase the two-terminal resistance/conductance. In order to measure the two-terminal conductance, the I_D–V_D characteristic is obtained while the gate terminal is kept floating.
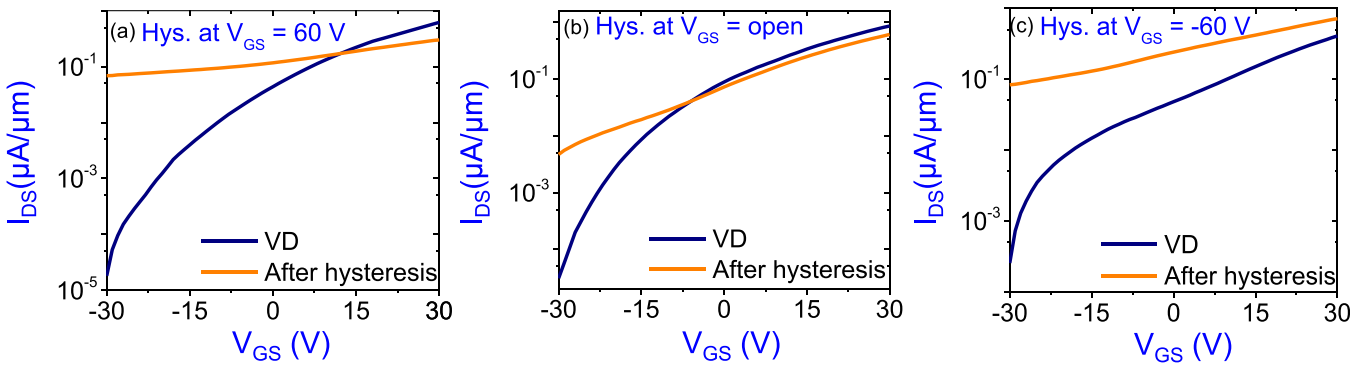

Figure 3. Transfer characteristics of MoS$_2$ FETs before and after the hysteresis cycle shown in figure 2(a). Hysteresis is performed on different devices which are operated in three major regimes of operation: (a) ON state, (b) two-terminal resistor by keeping the gate terminal floating and (c) OFF state.

states contributing to the charge transport in the OFF state ($V_{GS} = -60$ V) and near-band transport (floating gate) leads to an abrupt increase in the channel current. However, when the device is in the ON state, the increase in mid-gap states does not starkly affect charge transport because of the pre-existing transport through the conduction band with an abundance of states available for charge transport. Since this is a post-hysteretic effect, it is believed to be related to the commonly observed hysteresis-induced RS in MoS$_2$.

Interestingly, the effect of current–voltage hysteresis on transistor behavior is same as that of a steady-state/long-term DC electrical stress as discussed in our previous work [18]. Such a remarkable similarity in the impact on transistor behavior and well-established hysteresis-induced RS in MoS$_2$ [9–14, 16] encourages an investigation to validate the possibility of LTES-induced RS in our devices. Therefore, MoS$_2$ transistors are subjected to multiple LTES cycles with varying voltage polarity to observe change in the channel resistance.

2.2. LTES-induced RS

In order to further elucidate further the effect of LTES on transistor behavior, MoS$_2$ devices are stressed, as discussed

in an earlier report [18], under conditions that prevent current decay during stress. Such stress conditions are chosen to ensure minimum lattice damage due to electron–phonon scattering (EPS) in order to de-couple the RS mechanism from the EPS-induced change in the material. A unique behavior is observed when a device is stressed at drain-to-source electric field $E_{DS} = 0.2$ MV cm^{-1} and $V_{GS} = 0$ V for 300 s (figure 4(a)). The current through the channel is found to be constant at $I_{DS} = 1$ μA μm^{-1} during the first 300 s stress cycle. Interestingly, the current begins from a higher value at $I_{DS} = 3$ μA μm^{-1} in the second stress cycle and eventually rises abruptly to ∼8 μA μm^{-1} at $t = 200$ s and settles at ∼4 μA μm^{-1} towards the end of the cycle at $t = 300$ s. Current during subsequent stress cycles remains constant at ∼4 and 5 μA μm^{-1} after which it again abruptly rises to ∼11 μA μm^{-1} at $t = 280$ s during the fifth stress cycle and the device continues to remain at the same current density throughout the sixth stress cycle. During the course of six stress cycles, the device exhibits three different resistance states. This is attributed to the electrical stress-induced changes in MoS$_2$, reported previously by the authors, where localized low-resistance regions are found to have formed within the MoS$_2$ channel [18]. The effect of different cycles

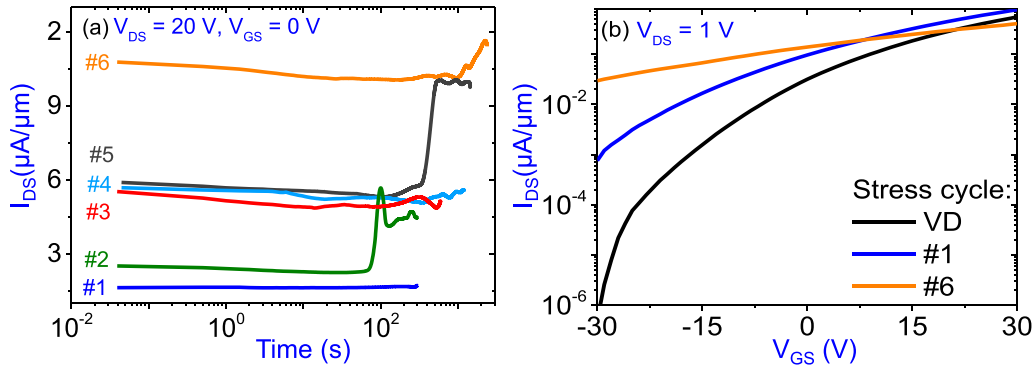J. Phys. D: Appl. Phys. **55** (2022) 085102

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Figure 4. (a) Current variation during steady-state DC electrical stress as a function of number of stress cycles. Bias conditions during the stress are: $V_{DS} = 20$ V and $V_{GS} = 0$ V. (b) Impact of steady-state electrical stress on the transfer characteristics of MoS$_2$ FET. Perturbation from conventional transistor behavior is observed after long-term stress and is found to be similar to that obtained after hysteresis in figure 3.
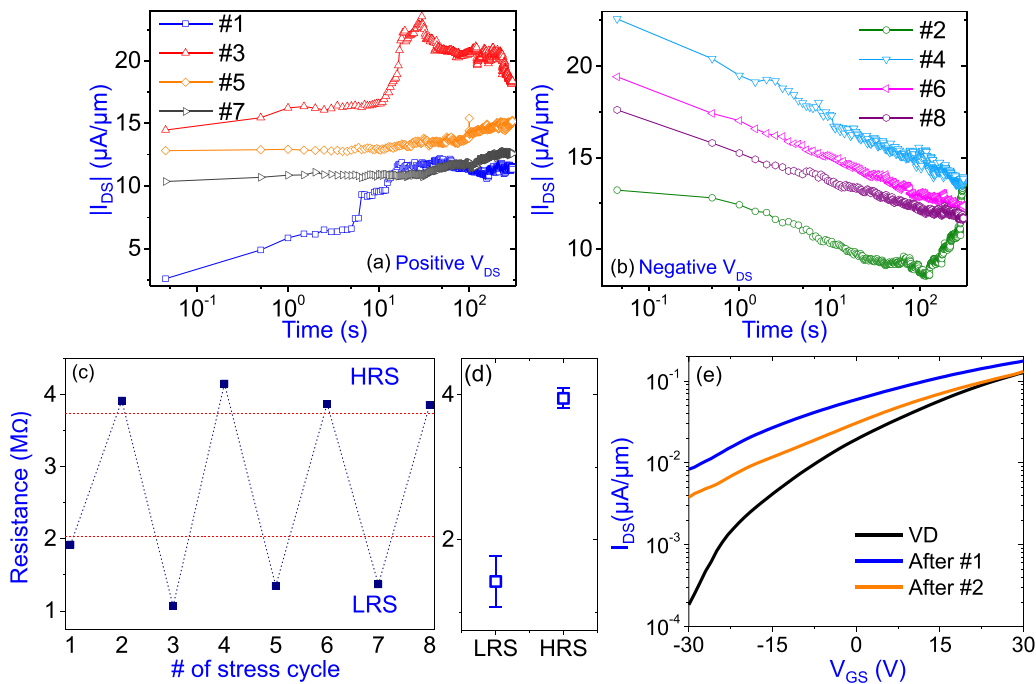

Figure 5. Current fluctuation during multiple cycles of steady-state electrical stress of (a) $V_{DS} = +20$ V and (b) $V_{DS} = -20$ V with $V_{GS} = 0$ V in both cases. Note that the device is subjected to alternate positive and negative stress cycles (odd number cycles are positive while even number cycles are negative, shown in (a) and (b), respectively). (c) Two distinct resistance states are realized due to successive stress cycles. All positive/odd stress cycles led to a LRS while all negative/even stress cycles resulted in a HRS. (d) The error/standard deviation in the values of two resistance states realized due to repeated operation is fairly low. (e) Effect of polarity of the steady-state stress on the transfer characteristics of MoS$_2$ FET. A negative stress following a positive stress event tends to nullify the effect of previous cycle on the transistor characteristics.

of stress-induced material reconfiguration on transistor behavior is shown in figure 4(b). In subsequent stress cycles, the V_T of the device is found to have shifted in the negative direction followed by a complete loss of gate control. This implies that the material has undergone changes such that the free-electron concentration in the channel has increased [18]. Different resistance states are observed in figure 4(a) which can be correlated to discrete increase in the electron concentration in the channel realized at different stress cycles. Observation of such discrete resistance states is similar to LTP, which is a synapse-like property of MoS$_2$ important for neuromorphic applications. In order to observe LTD through LTES, devices

are stressed with varying polarity of V_{DS}. Current variation during stress cycles of opposite polarity along with its impact on the transistor behavior are presented next.

Stress-induced current fluctuations and perturbation of transistor behavior is found to be dependent on the polarity of drain-to-source bias. As shown in figures 5(a) and (b), alternate forward ($V_{DS} = 20$ V) and reverse ($V_{DS} = -20$ V) stress cycles result in abrupt or monotonically increasing and decreasing current respectively. A forward (reverse) stress brings the device in a LRS (HRS). As observed in figure 5(c), device resistance fluctuates broadly between two values, within an error of ~25% in LRS and ~3% in HRS, when stressed alternately

under opposite polarity bias (figure 5(d)). In other words, positive stress leads to LTP whereas negative stress results in LTD. Moreover, the switching ratio (SR), the ratio between the resistance in LRS and that in HRS, is found to be ~2.76. This behavior is ascribed to the RS properties of MoS_2 wherein sulfur vacancies migrate under the effect of electrical stress and a bipolar switching occurs, which as discussed earlier has been observed by others [9–14, 16].

Such a variation with stress polarity is also observed in the transfer characteristics of the transistor, as shown in figure 5(e). Stress cycles with alternate polarity result in binary current fluctuation due to RS between the two resistance states. It is observed that, after the first positive stress cycle, gate tunability of the devices is significantly degraded along with a huge negative shift in V_T. A signature of LTD is found in the transfer characteristics when a subsequent negative stress cycle tends to bring down the overall channel current. However, it fails to realize the original virgin state of MoS_2. This implies that LTES results in a permanent change in MoS_2 which is irreversible in nature. Moreover, it also suggests that akin to current voltage hysteresis, discussed earlier, LTES triggers observable memory behavior in MoS_2. It is argued that both hysteresis and LTES result in a similar change in material configuration and hence perturbation in the behavior of MoS_2 transistors. Therefore, the above discussion suggests that RS in MoS_2 device can be triggered not only via hysteresis cycles but also via LTES with suitable stress conditions.

It can be inferred from figures 4 and 5 that LTES induces a permanent change in MoS_2 after which polarity-dependent realization of two resistance states can be achieved. Similar behavior is observed in certain RS materials for which a preliminary forming process is used to trigger memory characteristics. This drives attention towards a possible forming step for MoS_2 which can improve its switching performance. It turns out that LTES induces better switching performance in a MoS_2-based two-terminal RRAM thereby making it more relevant for binary memory applications, as discussed next.

2.3. Forming in MoS_2 for improved binary switching

As discussed, LTES-induced perturbation in MoS_2 is similar to voltage-induced formation of RRAMs and other memory devices [20] reported earlier. Such a forming process has been reported to trigger memory behavior in HfO_2-based RRAMs [24] and is followed by SET/RESET programming of the memory cell. Moreover, the fact that LTES induces RS in our devices appeals as a way of testing this phenomenon as a possible forming process for CVD-grown monolayer MoS_2. In order to implement LTES as a forming process, two-terminal MoS_2 devices are subjected to multiple SET and RESET cycles before and after LTES. This is done to observe the impact of LTES on binary switching behavior of these devices and address the question of a possible forming procedure in MoS_2.

The forming event is carried out by stressing MoS_2 electrically at $V_{DS} = 20$ V and $V_{GS} = 0$ V for the duration, until an abrupt change in the device current is observed. Such a scheme to form our devices is used because a sharp rise in current was

observed earlier in figure 4(a) with the same bias conditions as mentioned above. It is observed in figure 6(a) that after a sustained current level for about 30 s, current rises sharply and settles at a value about 1.7 times higher. Such a variation in current implies that the channel conductance has increased and therefore is regarded as a forming step. It is important to highlight the time instance at which current abruptly rises, which is different in figure 6(a) compared to that shown earlier in figure 4(a). A possible argument for such a variation in device current dynamics is that GBs, which are primarily responsible for RS in CVD-grown monolayer MoS_2[9], are randomly oriented and different devices can have a different number of GBs running randomly across the channel region. In order to identify the effect of this forming step, switching performance of our devices is compared before and after forming. In order to perform a memory test, two-terminal MoS_2 devices (open gate condition) are programmed (SET) and erased (RESET) by a train of 100 pulses of ±30 V of 100 ms with 50% duty cycle, as shown in figure 6(b). To read the state of the device without perturbing it, a 1 ms read pulse of 0.1 V is applied across the device (figure 6(c)). It is observed that a virgin device (VD) does not exhibit significant binary switching. Multiple program and erase cycles result in consistent current (~180 nA μm^{-1}) which implies that the resistance of the device does not switch. This is in contrast to the observed binary and analog switching in MoS_2 [9–14, 16]. Such a contrasting behavior is ascribed to program, erase and/or read bias conditions, insufficient to induce resistance change in the device. Identifying the right bias conditions for MoS_2 devices is not the focus of this work and is therefore not discussed in the paper. It is important to emphasize that this paper discusses the effects of LTES on the switching behavior in MoS_2 devices and qualifies it as a possible forming step. Interestingly and in contrast to the observed failure in performing a SET/RESET process on a VD, the same device exhibits decent switching performance after undergoing a stress cycle/forming step and is referred to as a stressed device (SD). A train of 100 pulses of ±30 V of 100 ms with a 50% duty cycle to SET/RESET the device results in two different resistance states corresponding to two different current values, ~0.45 nA μm^{-1} (SET or 1) and ~0.18 nA μm^{-1} (RESET or 0), measured when a subsequent read pulse (0.1 V and 1 ms) is applied, as shown in figure 6(c). This is observed for six alternate SET and RESET cycles with an SR (SET current/RESET current) of 2.5. These results clearly imply that LTES can be employed as a forming process for MoS_2-based two-terminal RRAMs to ensure better switching performance.

As observed earlier in the case of hysteresis-induced conductance change in figure 2, gate terminal plays an important role during RS in our MoS_2 devices implying that transport mechanism in the MoS_2 determines the amount of change in channel resistance. We, therefore, explore the impact of gate bias on the switching performance, as obtained from pulse measurements scheme, of MoS_2. It is observed that irrespective of gate voltage, formed devices (FDs) exhibit higher SW (current at LRS−current at HRS) than VDs (figure 7(a)). Note that these devices are formed at $V_{DS}/V_F = 20$ V and $V_{GS} = 0$ V. The SR is found to have improved by ~29% at $V_{GS} = -30$ V
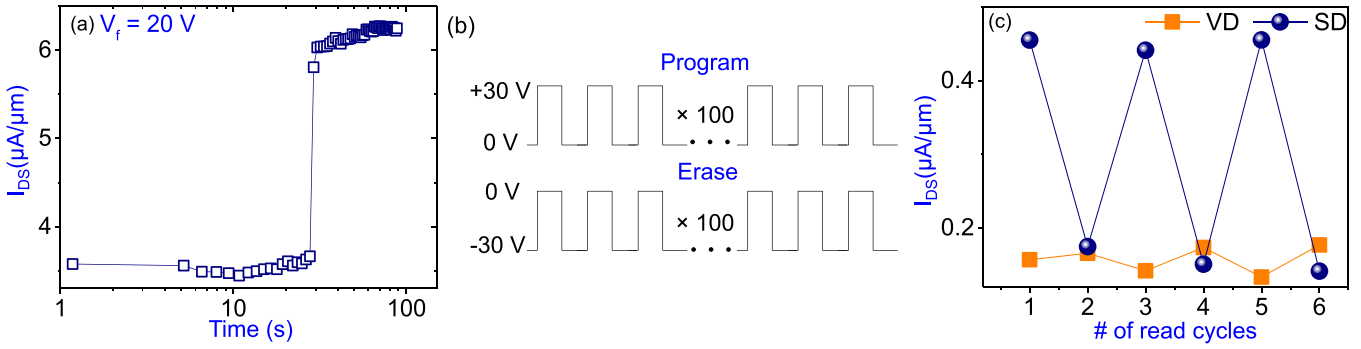
Figure 6. (a) Variation of device current during the forming process performed under the following stress conditions: V_f or $V_{DS} = 20$ V and $V_{GS} = 0$ V. (b) Pulse program and erase signals are applied across the two-terminal MoS_2 RRAM, before and after the electrical stress event shown in (a), to write '1' and '0', respectively. These signals are two trains each of 100 pulses of 100 ms and 50% duty cycle with amplitude of $+30$ V and -30 V for programming and erasing, respectively. (c) A read signal of 1 ms width and 0.1 V amplitude is used to read the state of the device and is applied after every program or erase cycle. This is done successively for six cycles. As mentioned earlier, each program and erase cycle is followed by a read cycle and such a write-read sequence is used to analyze the switching behavior of MoS_2 before (VD) and after (SD) forming.
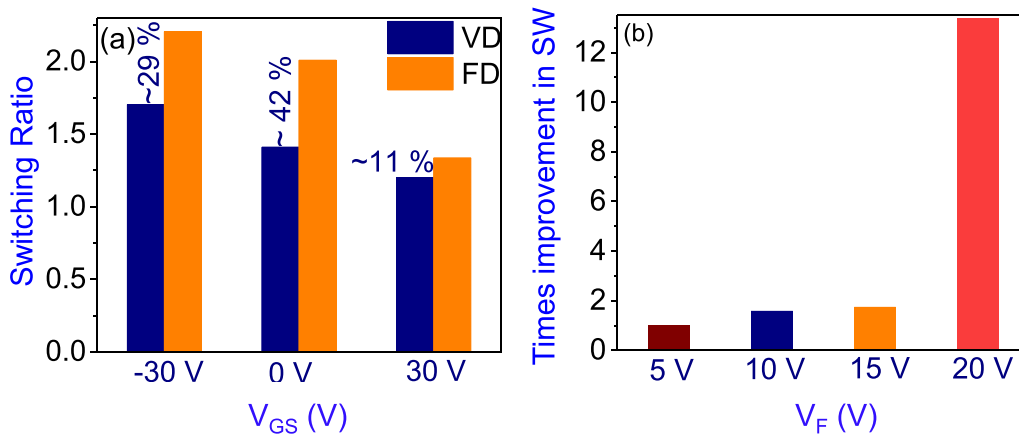

Figure 7. (a) SR as a function of gate voltage applied during program/erase and read cycles. SW is extracted from transfer characteristics shown in figure S3 of SI measured at $V_{DS} = 0.1$ V. (b) SW as a function of forming voltage (V_F). Here SW is extracted for the two-terminal device at $V_{DS} = 0.1$ V via a voltage sweep event, as shown in figure S3.

and the increase in SR is $\sim$42% and $\sim$11% at $V_{GS} = 0$ V and 30 V, respectively. This implies that SET/RESET cycles in both VD and FD are more efficient at lower and/or negative gate voltage and a forming process tends to improve the switching performance of VDs irrespective of the gate bias. Interestingly, the extent to which forming-led improvement in SR occurs depends on V_{GS}, and it turns out that at $V_{GS} = -30$ V and 0 V the increase in SR is larger than that at $V_{GS} = 30$ V. Note that while at $V_{GS} = 0$ V, the device is at the onset of the ON state operation and charge transport happens via states close to CBM, at $V_{GS} = -30$ V the device is in the OFF state due to transport through a limited number of mid-gap states. Such a dependence on gate voltage is the fallout of the forming-induced large density of mid-gap states that facilitate charge transport in MoS_2 in the OFF state, as discussed earlier. A subtle yet important observation is that switching in MoS_2 is more efficient when the device is in the OFF state, even without a forming step (figure 7(a)). These observations collectively imply that MoS_2-based RRAMs exhibit better switching performance when

they are depleted of free charge carriers, and an LTES forming step improves it further. It is worth mentioning that, owing to a large difference in the magnitude of current flowing in the three different regimes of operation, we choose SR as the parameter to compare switching performance at various gate voltages. While gate voltage has remarkable influence on the RS properties of MoS_2, stress voltage during the forming step, V_F, also determines the switching performance of FDs. Devices formed at lower V_F do not exhibit a significantly improved SW than VD. This is shown in the detailed transfer characteristics of VD and FD with varying V_F in figures S3(a)–(d) of SI.

Order to observe the effect of V_F on switching performance, MoS_2 devices are subjected to SET/RESET and read cycles before and after forming at varying V_F. The SW of VDs and FDs are compared and shown in figure 7(b) as a function of V_F. Note that the gate terminal is kept open during these cycles for both VDs and FDs. This is done to ensure a negligible effect of gate terminal on the switching behavior. The detailed $I_D V_D$ data for the gate open condition is shown in figures S3(e)–(h).

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Table 1. Comparison of SR of various RRAM devices with only MoS$_2$ as the active layer.

Electrodes	Substrate	Switching ratio	Reference
RGO/ITO	SiO$_2$	10^4	[26]
FTO/Ag	Glass	10^3	[27]
Au/Au	Si/SiO$_2$	10^3	[9]
Au/Au	Si	10	[25]
Ag/Ag	Glass	—	[11]
ITO/Ag	Glass	10^4	[28]
ITO/Al	Glass	10^2	[29]
Ag/Ag	Kapton	10^8	[30]
Ni–Mn–In/Cu	Si	10^2	[31]
Ti–Au/Ti–Au	Si	—	[32]
Au/Au	Glass	10^3	[33]
Ti/Ag	Ti	2	[34]
Ni–Au/Ni–Au	Si/SiO$_2$	2.5	This work

It is observed that forming at higher V_F leads to a much higher improvement in the SW (with SW the difference between the current at LRS and HRS). As shown in figure 7(b), the device formed at 20 V exhibits $\sim$13$\times$ improved SW than its virgin counterpart. However, improvement in SW for devices formed at $V_F = 15$ V, 10 V and 5 V is found to be $\sim$1.7$\times$, $\sim$1.6$\times$ and $\sim$1$\times$, respectively. Such a variation with V_F suggests strong influence of the drain-to-source electric field during forming on RS properties of MoS$_2$. While V_{GS} determines the dominant transport mechanism in MoS$_2$ FETs and lower or negative V_{GS} facilitates better switching performance, it appears that V_F triggers the formation of mid-gap states. Also, in order to introduce mid-gap states, sufficient V_F must be applied for an appropriate forming event to take place. The SR of other MoS$_2$-based RRAMs is compared in table 1, shown below. It is important to note that these reports discuss pristine MoS$_2$ devices and a forming process employed on these devices will further improve the switching performance. Use of white light to improve RS properties has been reported previously [25]. Photons are another stimulus, like LTES, that can be used to improve the switching performance of RRAMs. Moreover, white light and electrical forming process, proposed in this work, can be used together to further improve the performance. While a forming process under white light should not affect how defects are formed due to LTES, memory program operations under white light may result in much higher SW, owing to the relatively large number of formed defect states available for conduction due to photon-induced electron excitations from mid-gap states to the conduction band. However, this will depend on the relative energy difference of formed states and conduction band and therefore the scenario under white light illumination cannot currently be precisely sketched.

Insights developed regarding the impact of gate bias-controlled charge transport and forming voltage on the RS properties of CVD-grown monolayer MoS$_2$ strongly suggest that RS is most efficient when the device is depleted of free charge carriers and the switching performance can be further improved by a high voltage forming step prior to use as binary memory cells in a circuit environment.

3. Conclusion

We report new insights concerning a well-established phenomenon of current–voltage hysteresis which is known to induce RS in CVD-grown monolayer MoS$_2$. The extent to which hysteresis affects resistance of the device is found to be dependent on the charge transport mechanism dominant in MoS$_2$ during hysteresis. Therefore, tuning gate bias to control the charge transport mechanism and hence RS in our devices is key for achieving improved switching performance. Impact of hysteresis on the overall transistor behavior suggests that RS in MoS$_2$ is accompanied by a unique deviation in the transistor behavior with poor gate control and huge negative shift in the threshold voltage. It turns out that such a deviation from the conventional transistor behavior is a signature of RS and is also observed when an LTES DC is applied on our devices. Polarity-dependent realization of LRS and HRS confirm LTES-induced RS. With this, besides hysteresis, we introduce another way of achieving RS in MoS$_2$. We also find that devices that undergo LTES exhibit significantly improved switching performance compared to VDs. Therefore, we propose that LTES, under certain bias conditions, can be used as a forming step in our devices to achieve enhanced memory SW, i.e. larger separation between LRS and HRS. RS induced by LTES is found to be linearly dependent on the drain-to-source voltage during stress, referred as VF, and therefore higher VF is found to induce enhanced SW. Moreover, RS induced by hysteresis and LTES is more conspicuous for devices operating in the OFF state during which mid-gap states facilitate most of the charge transport across the channel via a variable range hopping mechanism. Such gate voltage dependence of switching performance and impact of RS on transistor behavior clearly imply that both hysteresis and LTES introduce mid-gap states in MoS$_2$ that lead to RS. However, a more direct way of characterizing these states has not been discussed in this work. Developed insights on gate voltage dependence on RS and impact of VF on the SW indicate that a higher forming voltage along with a negative gate bias to deplete the channel are essential to realize improved switching performance in CVD-grown monolayer MoS$_2$-based binary RRAMs, thereby making them more relevant for binary memory applications.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

Acknowledgments

Conflicts of interest

There are no conflicts to declare.

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Author contribution

Ansh fabricated and characterized all the devices. Ansh and M S analyzed the data and wrote the paper.

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