Current Filament Dynamics Under ESD Stress in High Voltage (Bidirectional) SCRs and It's Implications on Power Law Behavior

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Abstract— **Physical Insights into the early formation of current filaments in High Voltage SCR is presented. Repeated current filamentation and subsequent filament spreading, which in turn results in filament motion, is detected using 3D TCAD. Impact of different load lines on ESD robustness and filament dynamics with ESD stress duration has been studied using experiments and 3D TCAD simulations. Finally, impact of silicide blocking in mitigating filament strength has been studied, which in turn improves the ESD robustness.**

***Index Terms*—Electrostatic Discharge, Laterally Double Diffused MOS (LDMOS), Silicon Controlled rectifier (SCR).**

I. Introduction

ESD protection of high voltage (HV) functionalities, often a case in automotive or power-SoC applications, becomes challenging due to relatively higher power dissipation across protection elements and early space charge modulation [1]. Different HV ESD protection options are HV Diodes, LDMOS [2]-[3], LDMOS-SCR [4] and HV Silicon Controlled Rectifiers (SCR) [5]. HV SCRs are often favorable due it's compact integration in a bidirectional configuration [5] and higher ESD robustness when compared to other HV snapback devices. Still, HV SCR's ESD failure, unlike low voltage SCRs, don't follow the much required power law behavior/Wunsh-Bell curve [6]. Engineering HV SCR to improve it's ESD robustness under longer ESD stress or system level ESD conditions requires physical insights into the current filamentation and early failure of these devices under longer ESD stress conditions. Different groups in the past have made efforts to understand the current filament formation and its motion, as a function of stress time and stress amplitude in various different ESD protection devices [7-11]. However, such detailed study on High Voltage Bidirectional SCR devices using measured data and 3D TCAD simulations is still missing in the literature. Keeping the above in mind, this work presents insights into the filament dynamics in HV SCRs and it's implications on ESD power scalability.

II. High Voltage (Bidirectional) SCR Under Stress

HV SCR integrated in a bidirectional configuration as depicted in figure.1 is studied in this work. Here two P-Wells (can be symmetrical or asymmetrical) are implanted inside a HV N-Well, where the N-Well is left floating / without any N-type tap to take both positive and negative ESD strikes. The high side P+/P-well region inside N-Well acts as the

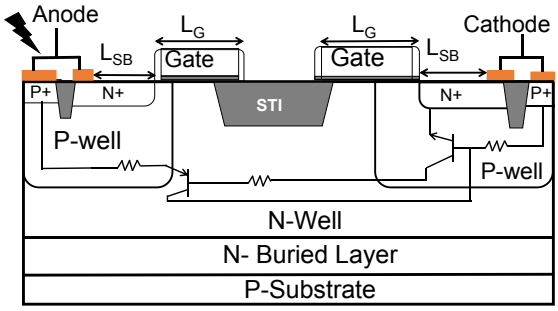

Fig. 1: 2D Cross-sectional view of HVSCR. The N-well is left floating. The P+ /P-well acts as anode terminal. The highly doped buried region (NBL) is underneath N-well for isolation. Here, L_{SB} is the silicide blocked length. When L_{SB}=0 it is Fully Silicided. The gate is grounded in all the measurements.

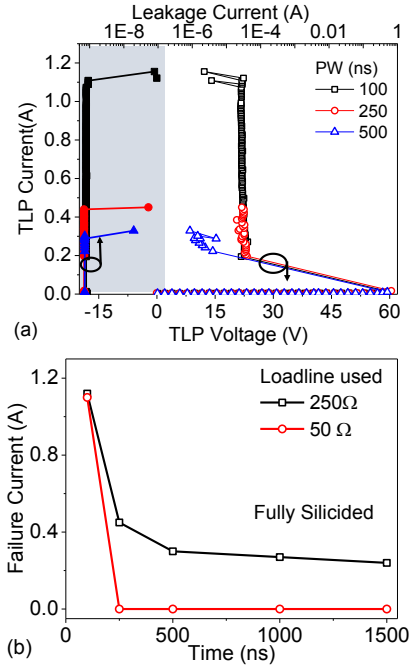

Fig. 2: Experimentally measured TLP I-V characteristics of fully silicided HV SCR under different pulse durations. 250 Ω load line is used in these measurements. (b) Failure current measured at different Pulse widths and load lines. A collapse in It2 for 50Ω load line beyond 100ns pulse is observed.

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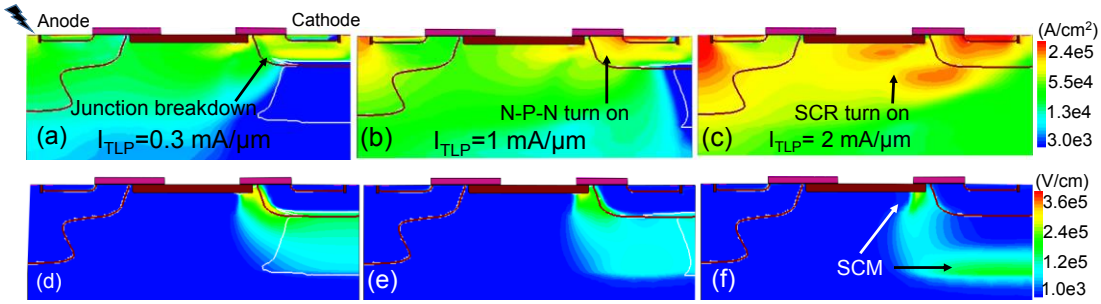

Fig. 4: (a-c) Conduction current density and (d-f) Electric field at different injection currents. Electrothermal simulations are employed.

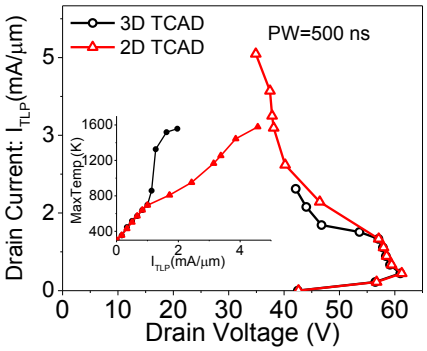

Fig. 3: Simulated TLP I-V characteristics of 2D and 3D devices. 3D device shows deeper snapback and increase in lattice temperature, which is attributed to presence of filament in 3D device.

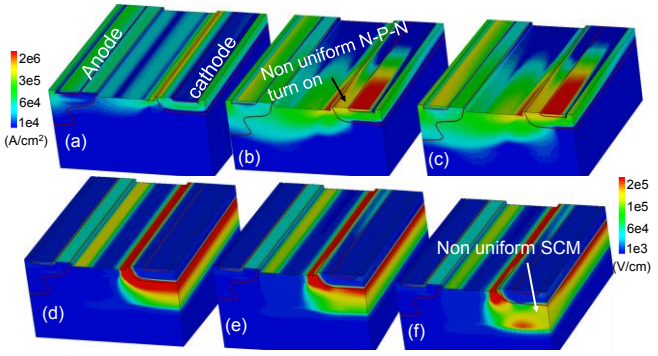

Fig. 5: (a-c) Conduction current density and (d-f) Electric field with increasing stress time extracted at an injected current of 1.5mA/μm by using Electrothermal 3D simulations.

anode contact, whereas the other P+ in P-Well acts as SCR's P-tap. The N+ in P-Well acts as emitter terminal of parasitic NPN, which can also have silicide blocking. The gate can be used to externally trigger the SCR. This work however studies the worst-case scenario, which is the grounded gate configuration. The device is in bidirectional configuration, which results in S-shaped I-V characteristic. Given the identical behaviour under positive and negative stress conditions, this work will present results and physics under positive stress condition.

III. Unique Experimental and 3D TCAD Observations

Measured TLP I-V characteristic (Fig. 2) of fully silicided HV SCR show the following trends: (i) very high failure current under 100ns TLP, which is independent of load line resistance; (ii) failure current drops dramatically at longer stress times (>200ns), depicting a clear dependence on load line resistance; (iii) high load line resistance (250Ω) allows the device to survive snapback state, however device fails a little above holding current, which attributes to ESD failure current independent of stress time for longer stress pulses; and (iv) lower load line resistance (50Ω) leads to high current injection immediately after snapback, leading to catastrophic failure resulting in practically zero ESD robustness of HV SCRs at longer stress pulses. 3D TCAD characteristics (Fig. 3) depict a deeper voltage snapback and sharp increase in lattice temperature post snapback when compared to 2D counterpart. It should be noted that 2D simulations in principle will not capture the 3D phenomena. The observed departure of high current 3D TCAD characteristics from 2D behaviour is unique to HV SCR (often not seen in LV SCRs), which depicts presence of non-uniformities, possibility in form of current filament, along the width (3D) plane.

IV. Physical Insights into Filament Formation

At current before snapback, well junction breakdown dominates the current conduction (Fig. 4a). Impact ionization (II) generated excess holes consequently trigger the parasitic NPN (Fig 4b), which floods the N-Well with injected electrons resulting in electron concentration higher than N-Well doping (**Fig 4c**). This subsequently results in space charge modulation (SCM) (**Fig 4d-f**), which shifts and localizes the peak electric field away from well junction (**Fig 4f**) and SCR turn-on. At the onset of junction breakdown, the current flows uniformly across the device width (**Fig. 5a**) and peak field was found to be around well junction (**Fig. 5d**). However, non-uniform II results in a non-uniform SCR turn-

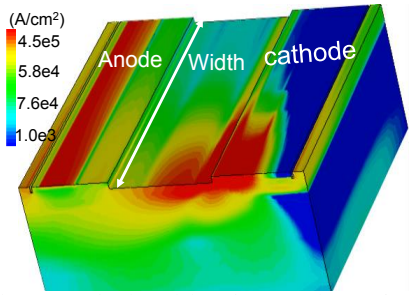

Fig. 6: Conduction current density at injected current of 1.5mA/μm extracted from 2D iso-thermal simulation. The formation of current filament implies that the filaments in HV SCR is electrical in nature.

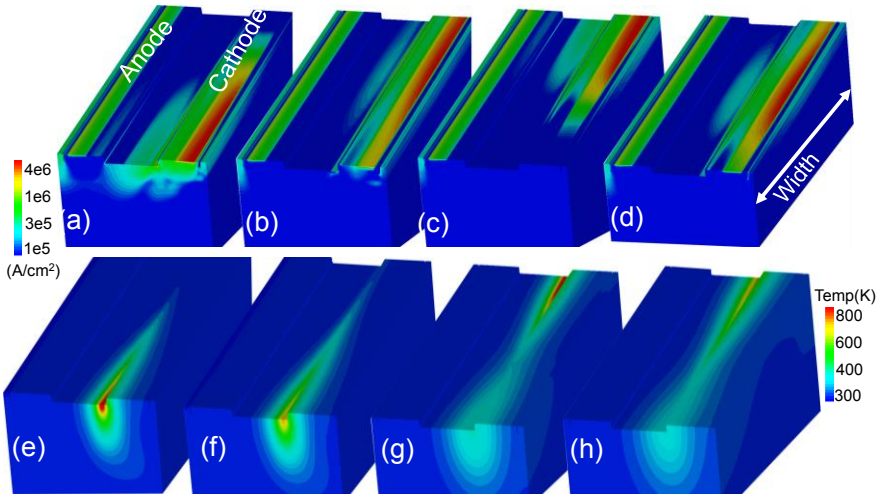

Fig. 7: (a-d) Conduction current density and (e-h) lattice temperature at different stress times at an injected current of 2mA/μm. The filament is observed to form at one of the edges (a), which results in a localized hotspot (e). With time, filament spread along the device width (b), which relaxes the lattice temperature (f). When it reaches the other corner, filament gets stronger at the other edge (c), which again creates a hotspot at the other corner (g). Same is found to repeat over the stress time (d & h).

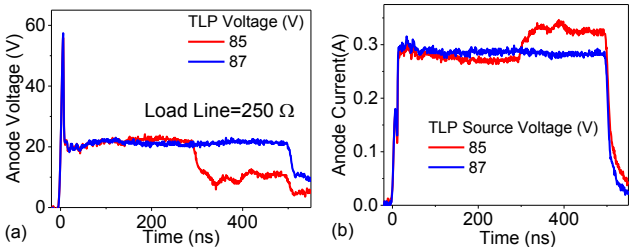

Fig. 8: Measured transient (a) voltage and (c) current, depicting the pulse to pulse instability. At low source voltage abrupt collapse in DUT voltage and increase in current is observed indicating presence of filament. At higher voltage the same behavior is missing because of current spreading.

on (**Fig. 5b**), which in turn leads to localized SCM at one of the corners (**Fig. 5e**). Localized space charge modulation causes localized e-field along the device width which further strengthens non-uniform II and localized SCM (**Fig. 5c,f**). This positive feedback action results in electrical instability and early filament formation, which consequently increases the lattice temperature inside the filament. Similar, mechanism is also discussed in [12]. Presence of filament in Iso-thermal 3D TCAD simulation **(Fig. 6)** validates that the filament is due to electrical instability as explained above and not because of thermal run-away.

V. Filament Dynamics: Repeated Filamentation and Spreading

Probing device behavior beyond filament formation revealed unique filament dynamics in HV SCR (Fig. 7 & 8). Formation of filament results in increased lattice temperature, which lowers the II rate inside the filament. Consequently, attributed to higher II rate outside filament, SCR turn-on efficiency improves outside the filament, which forces the filament to spread along the width plane (Fig. 9). This results in uniform current conduction and reduction in maximum lattice temperature. It should be noted that the II rate should be highest at the other corner, which is furthest from the hot

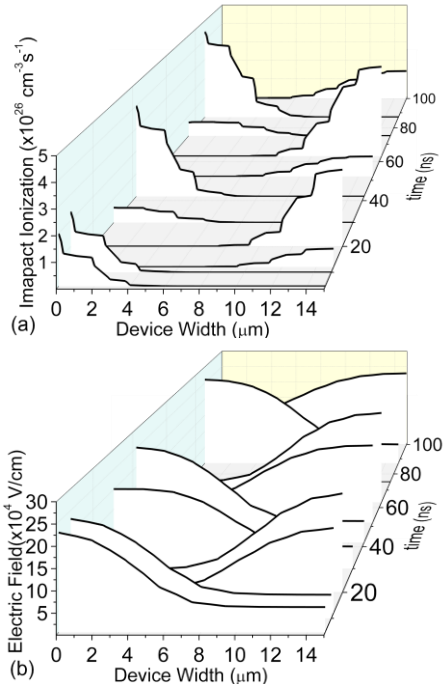

Fig. 9: (a) Electric field (EF) and (b) Impact ionization (II) in the device, with increasing stress time for the injected current of 2mA/μm. The shift in II and Electric field across the device width can be seen with increase in stress time. Filament formation causes lattice temperature to increase inside the filament region, which lower impact ionization rate. This allows the adjacent SCRs in the width plane to trigger faster, which forces filament to spread along the device width. Once it reaches the other edge, it becomes stronger again and starts spreading in the reverse direction.

spot / filament location. This parallelly triggers the same non-uniform turn-on action, however at the other corner. This way the filament shifts to the other corner post filament spreading (Fig. 7). The process continues and is seen as filament motions. This results in ringing in lattice temperature, which hinders the device to see a catastrophic failure immediately after formation of current filament (Fig. 10). This was validated through experiments, where transient behavior

depicts pulse-to-pulse instability (Fig. 8), which is due to presence of filament and it's spreading. It is worth highlighting that such filament motion/spreading was found to be possible due to the floating nature of N-well region, which allows faster turn-on of SCR and subsequent filament spreading before lattice temperature inside filament exceeds critical temperature for Si failure. The series of physical events responsible for the filament motion are summarized in Fig. 11. spreading before lattice temperature inside filament exceeds critical temperature for Si failure. The series of physical events responsible for the filament motion are summarized in Fig. 11.

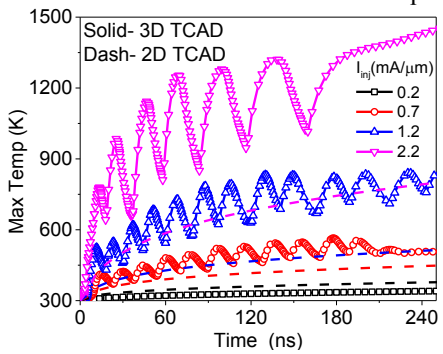

Fig. 10: Maximum lattice temperature as a function of stress time at different injected current extracted from both 2D and 3D simulations. Oscillation in temperature across 3D device is attributed to the filament formation and spreading, which however is missing in 2D simulations.

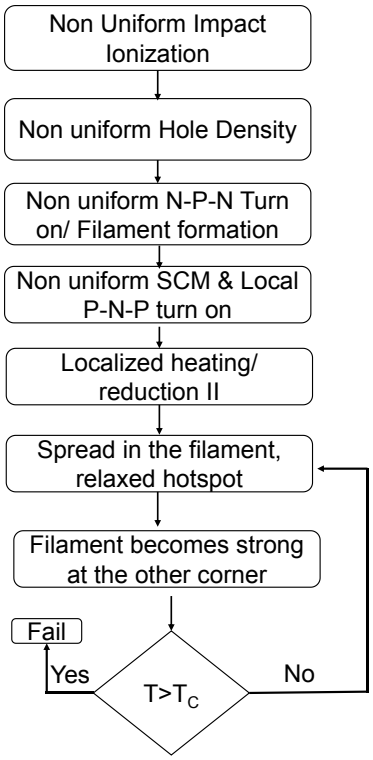

Fig. 11: Flow chart summarizing the series physical events discussed.

VI. Impact of Silicide Blocking

Figure 12 shows silicide blocking to improve ESD robustness and power scalability by suppressing strength of filament (**Fig. 13**). Though peak temperature inside filament was mitigated, presence of filament, filament motion and the root cause remain unchanged.

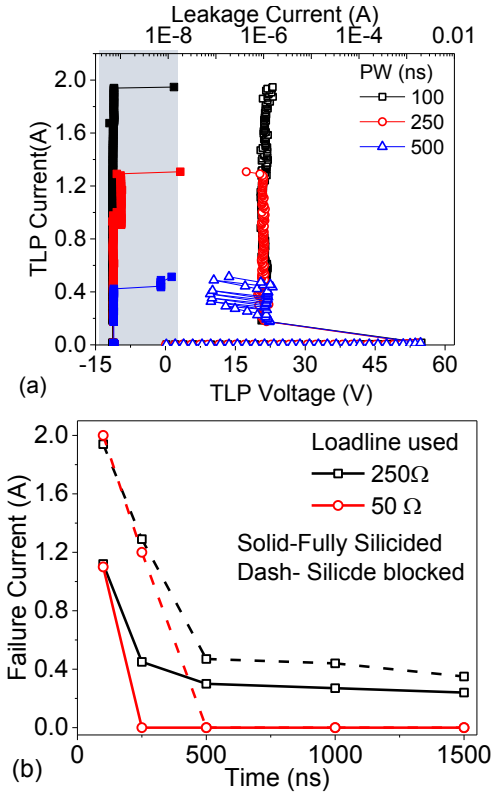

Fig. 12: Experimental TLP I-V characteristics of source side silicide blocked HV SCR. The experiments are carried out with 250Ω load line. (b) Failure current comparison for different load lines at various pulse widths. With 250Ω load line device survives longer pulses, whereas 50Ω load line results a collapse in failure current. Silicide blocked device was found to offer improved power law behavior however the same trend persisted at longer pulse widths.

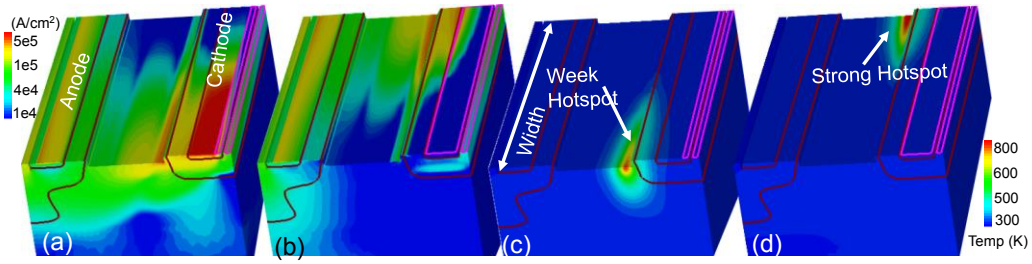

Fig. 13: (a-b) Conduction current density and (c-d) lattice temperature for silicide blocked (a & c) and fully silicided (b & d) device at injected current of 2mA/μm. Silicide blocking increases filament width, which lowers the peak temperature inside filament.

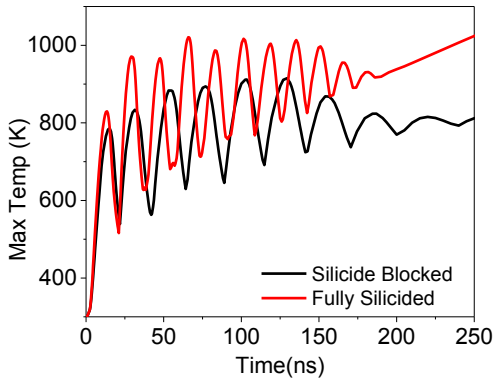

Fig. 14: (3D Sim.) Maximum temperature as a function of time across fully silicided and silicide blocked device at an injected current of 2mA/µm. Though both devices show filament formation, SB has lower average temperature.

VI. Conclusion

HV BDSCR devices were found to form electrical current filaments. The filament formation in these devices is attributed to an electrical instability resulting from non-uniform NPN turn-on, SCM and e-field localization. However, due to high resistance floating N-well, the filament was found to spread and subsequently move along the device width, which allowed device to survive snapback. While filament formation is electrical in nature, filament spreading is found to be electro-thermal phenomenon. Impact of load line in conjunction with early filament formation is discussed. Silicide blocking of NPN's emitter terminal mitigates the filament strength, which in-turn improves the Failure power even at longer pulse duration. Device behavior and presence of filament motion was however unchanged.

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