Physical Insights into the Low Current ESD Failure of LDMOS-SCR and Its Implication on Power Scalability

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Abstract— **A unique low current ESD failure during snapback region, which otherwise survive high current stress, is reported in LDMOS-SCR device. The failure is universal to LDMOS-SCR devices designed as self-protected MOS switch and found to be specific to a window of current between trigger and holding state, which can only be captured using high resistance load-line in TLP system. This resulted in severe power scalability issues in LDMOS-SCRs. In this work, while using systematic experiments and 3D TCAD simulations, we have developed detailed physical insights into the unique low current ESD failure phenomenon in LDMOS-SCR devices.**

Index Terms—**Electrostatic Discharge, Laterally Double Diffused MOS (LDMOS), Silicon Controlled rectifier (SCR).**

I. Introduction

High voltage functionalities which are key for building system on chips (SoC) or automotive products are often prone to ESD events. This results in a direct ESD threat to high voltage devices used in these circuits. In automotive environment these devices can see long ESD or ESD like stress events. Conventional high voltage options like LDMOS/DeMOS devices are known to be vulnerable against ESD stress [1-3]. Inserting a parasitic SCR within LDMOS device (LDMOS-SCR) was therefore proposed to improve ESD robustness under HBM or CDM conditions at the chip level [4]-[5]. However, HBM or CDM qualified LDMOS-SCR are often found to fail under system level ESD stress. For instance, long discharges from the system RC lines were found to causes early failure of LDMOS-SCR [6], which limited its uses to handle ESD stress beyond HBM time scales. To make LDMOS-SCR (Fig. 1) usable for automotive like applications and robust against system level ESD, ESD failure power scalability [7] with time is a must criterion. This paper for the first time, using detailed experiments and 3D TCAD simulations presents physical insights into missing power scalability and physics of current filamentation in LDMOS-SCR.

II. Power Scalability Issues in LDMOS- SCR

Fig. 2 shows that devices stressed with 50ns and 100ns wide pulse survive the snapback state and fail only at very high currents. However, the same when stressed using longer pulses fail during the snapback at very low currents and power. A collapse in power scalability was visible in all the measured devices (Fig. 3). However, such a collapse cannot be captured when TLP test was performed with low resistance load lines (50Ω in this case). For smaller load-lines

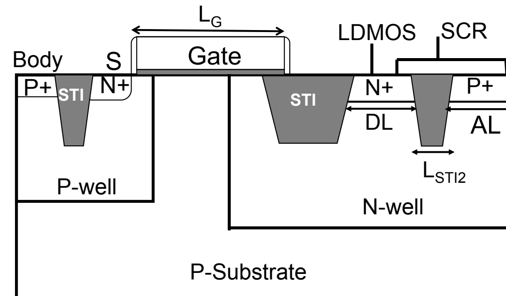
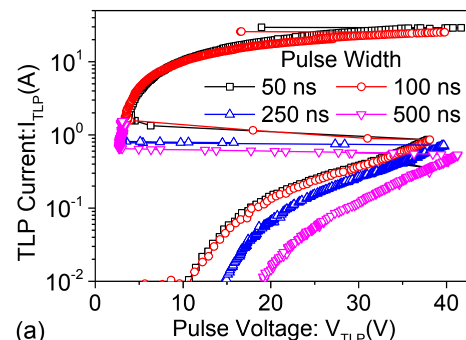


Fig. 1: Cross-sectional View of conventional LDMOS-SCR. 40V devices investigated in this work have DL = LAN = 0.5μm whereas LSTI2=1μm. To extract intrinsic LDMOS characteristics of LDMOS-SCR design, P+ (in N-Well) terminal was left floating.



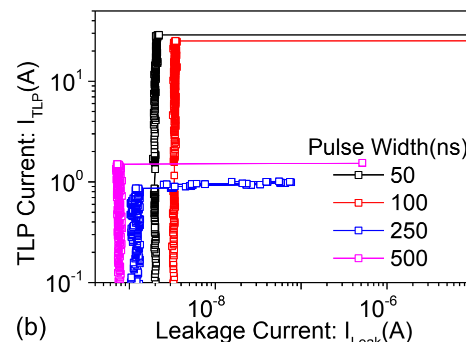


Fig. 2(a): Measured TLP I-V characteristics using >50Ω load-line of LDMOS-SCR device for different stress pulse widths. Higher load-line is used to capture device response to low currents during snapback. (b) Leakage current measured after each pulse. Device stressed beyond 100ns duration are observed to fail during the snapback.

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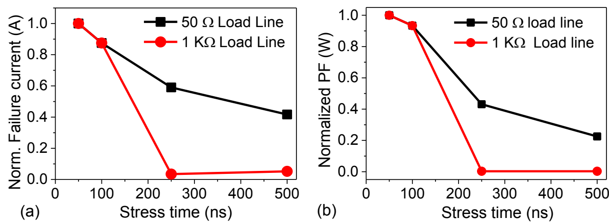

Fig. 3: (a) Normalized Failure current (Norm. with I_{Fail} @ 50ns) and (b) Norm. power to fail vs. stress (pulse) time extracted for 50Ω and 1KΩ load-line condition. TLP measurements using 1KΩ load-line are performed to capture device response to low currents during snapback. The LDMOS-SCR device has shown a sudden fall in failure current from 25A at 100 ns to 1.5 A for 250 ns, depicting severe power to fail scalability issues.

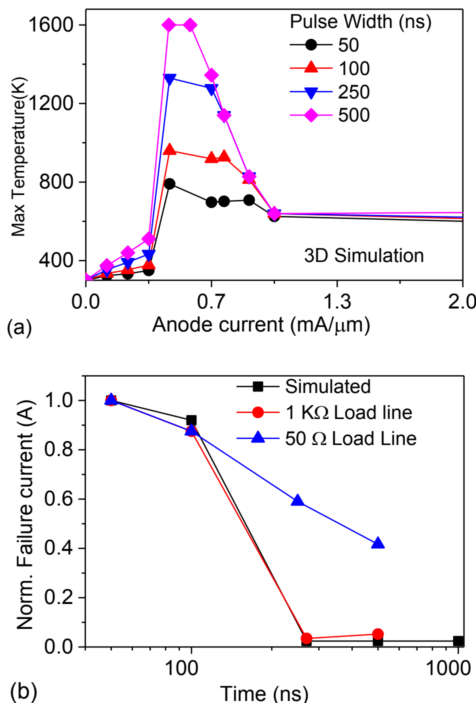

Fig. 4: Simulated (3D) maximum lattice temperature plotted as a function of stress current. Peak lattice temperature during the snapback region is observed, which was found to be due to formation of current filament. The max. temperature at low currents increases as function of stress duration. (c) Simulated (3D) normalized failure current compared with measured data confirming power scalability issue and 3D TCAD capability to capture collapse in the failure current at longer pulse durations.

the device experiences injection of very high currents immediately after snapback. The LDMOS-SCR devices were found to survive high current states, however were found to fail in a low current window between holding and trigger current. As a result, when current in the snapback window was enforced using higher load-line, power scalability was found to be missing. The same however was not captured when low current state was bypassed. 3D TCAD simulations are employed to understand the nature of such a weak power scalability and early failures during the snapback. Fig. 4a depicts (3D) simulated maximum lattice temperature as a function of injected current at different stress durations. Failure current with stress time extracted from 3D TCAD simulations was found to perfectly match with experimental trend (Fig. 4b). At this point it's worth mentioning that the

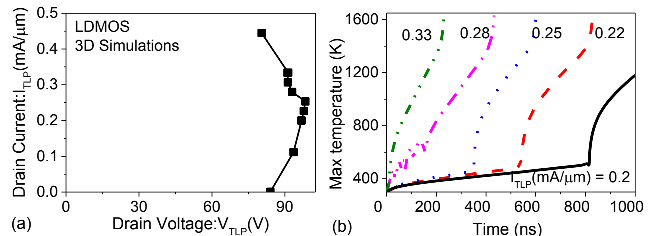

Fig. 5: Simulated TLP I-V characteristics of intrinsic LDMOS of LDMOS-SCR device. (b) Transient lattice temperature at different injected currents. Sharp rise in the temperature is due to electrothermal filament formation. The time for the filament formation decreases with increasing injected current, which is extracted for intrinsic LDMOS's 3D TLP simulations

3D Simulation data matches with the measured 1Kohm load line results, as the 3D TCAD simulations are performed with current stress boundary conditions. The device is stresses with all current values near the snapback region, as in the case of experiments with 1K ohm load line. Interestingly,

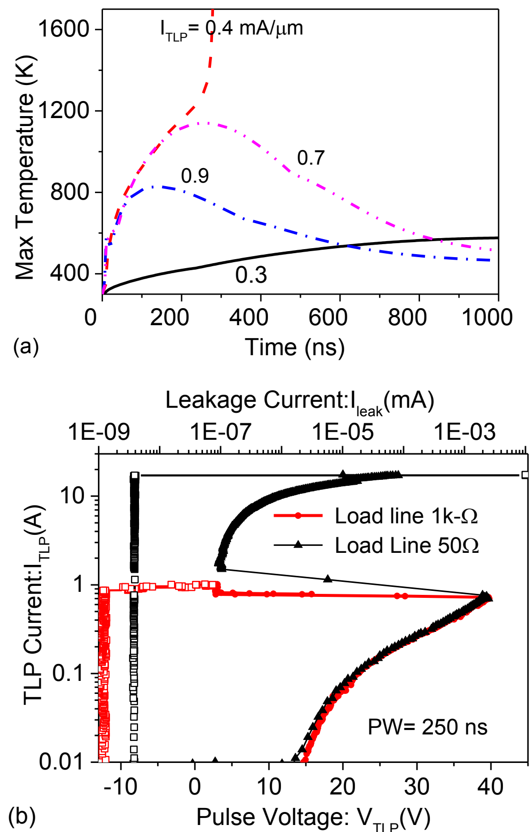

Fig. 6: (a) Maximum lattice temperature as a function of stress time in flipped LDMOS-SCR device for different injected TLP currents, in the low current snapback region. For small currents lattice temperature increases linearly with time, for medium current levels the lattice temperature increases exponentially leading to peak temperature above critical temperature. However, with increasing TLP current the peak temperature falls and shifts to lower time scales. A unique device failure is visible in a window of currents. (b) Experimental demonstration of the same behavior which shows device failure when injected current in the snapback region was limited by using a higher load-line when compared to low load-line case when injected current jumps to a very high current immediately after snapback, resulting in survival of filamentary behavior.

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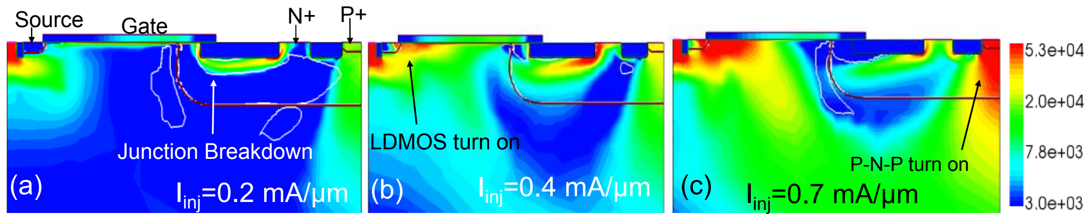

Fig. 7: 2D Current density(A/cm2) at (a) low current levels (0.2 mA/µm) after the junction breakdown (b) At moderate currents (0.4 mA/um), during the onset of LDMOS turn-on and (c) at higher current levels 0.7 mA/µm where the P-N-P turn is visible.

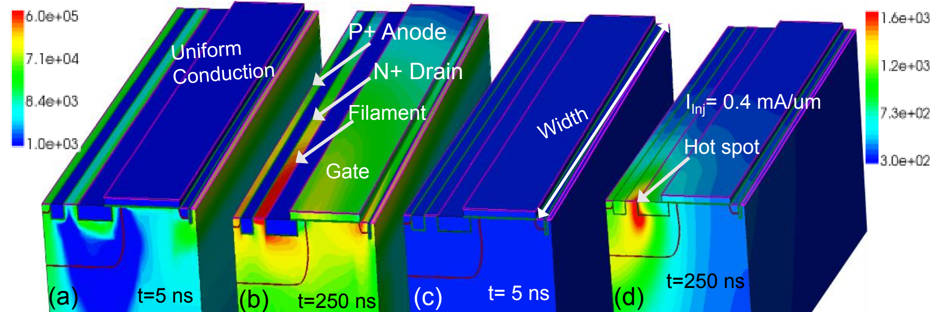

Fig. 8: (a)-(b) Current density (A/cm2) and (c)-(d) lattice temperature (K) for an injected current density (0.4 mA/µm) greater than trigger current, however lower than holding current of SCR extracted at 5ns and 250ns, respectively. The device is found to fail with the filament induced hotspot formation under the drain. It can be noticed that the intrinsic P-N-P was not yet triggered, and so didn't the SCR. This is evident from majority of electrons being collected by N+ drain contact (not by P+ contact, which would be the case of presence of SCR turn-on).

device tend to have highest temperature in the injected current window around snapback state, which at higher currents remain much below critical temperature to fail and doesn't change with stress time. During the snapback region however, lattice temperature is found to increase with increase in the stress time, which crosses critical temperature to fail for stress time > 250ns, resulting in device failure.

III. Low Current Failure: Physical Insights

A. Root cause of the problem: To understand the unique failure behavior of LDMOS-SCR at low currents, first the intrinsic LDMOS device is studied under similar ESD stress conditions (Fig. 5a). LDMOS device was found to fail due to space charge modulation induced electrothermal instability and filament formation [2][8], which leads to abrupt increase in lattice temperature as soon as filament is formed (Fig. 5b). In this case the time to trigger filamentary failure decreases with increasing stress current (Fig. 5b). A transient temperature analysis of LDMOS-SCR with increasing injected current near the low current snapback region reveals unique device behavior (Fig. 6a), as explained next. At very low injection currents (0.3mA/µm), the lattice temperature increases linearly with time. However, at moderate currents (0.4 mA/µm), the lattice temperature abruptly increases and crosses critical temperature for fail. However, at slightly higher currents (0.7 mA/µm), lattice temperature initially peaks to a value lower than the failure temperature and then falls as a function of time. The observed peak position shifts to lower time scales with increase in the injected current. The device was then found to survive higher currents. This shows the LMDOS-SCR fail within a "window" of current, during the snapback region for longer pulses. The same is experimentally verified (Fig. 6b) by enforcing or avoiding the low current state across the device with the use of lower load-line in the TLP setup. By bypassing the currents where the device is vulnerable to fail, the device is found to survive till very high currents under longer pulse durations.

B. Failure Physics: Fig. 7 depicts a series of physical events as a function of increasing stress. At low currents, the well junction breakdown dominates. Generated electrons collected at the N+ drain contact and holes traverse through the P-well are collected at the substrate contact. The positive potential developed under the source turns-on the intrinsic LDMOS's parasitic NPN (Fig. 7b). The N-well is then flooded with electrons which results in space charge modulation in the N-well region at moderate current (in the snapback state). It is to highlight here, that the N-well is more probable for early space charge modulation than the P-substrate, as the excess electrons in the N-well, because of N-P-N turn is very high, and holes in P-substrate is merely to keep to N-P-N turn on.

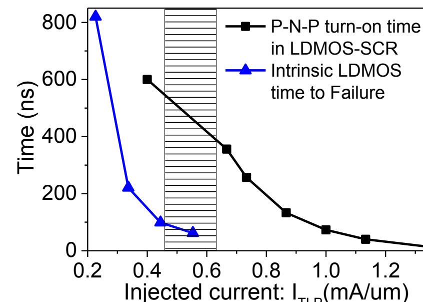

Fig. 10: Comparisons of P-N-P turn on time in flipped LDMOS-SCR and time required to form a destructive filament in intrinsic LDMOS device as a function of injection current. At a given injection current, intrinsic LDMOS fails before the P-N-P turns on. Presence of week P-N-P in the flipped configuration hinders SCR turn-on, which leads to the power scalability issues. The shaded region depicts the range of current in which the LDMOS-SCR fails if its P-N-P is not well designed.

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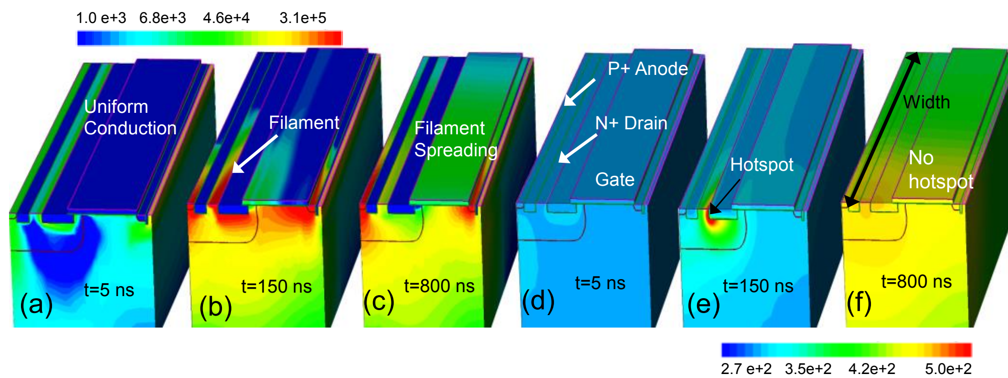

Fig. 9: (a) – (c) Current density (A/cm2) and (d) – (f) lattice temperature (K) extracted at different times: 5 ns (a,d), 150ns (b,e) & 800ns (c,f) for an injected current (0.9 mA/µm) greater than holding current. The current conducts uniformly until the filament formation. However, at high injection currents the P-N-P turns-on before the filament temperature reaches a critical value required for catastrophic filamentary action. Fast P-N-P turn-on at higher currents enables SCR turn-on before LDMOS driven filament failure and spreading of existing filament.

Further, increasing the current beyond the snapback state consequently turns-on the PNP causing SCR action (Fig.7c). Fig. 8 depicts the current density and lattice temperature at different time intervals at injection current of 0.4mA/µm, which resulted in space charge modulation in N-Well but was not enough for PNP turn-on. The Non-uniform space charge modulation leads to filament formation across intrinsic LDMOS device before SCR turns-on. It's worth highlighting here that the filament formation in LDMOS-SCR is dominated by the intrinsic LDMOS device, and the physics remain similar to [8]. Filament formation results in rapid lattice heating and eventual device failure. In this case, the absence of current through the P+ contact depicts absence of PNP/SCR turn-on. However, at high injection current, PNP turn-on (Fig. 9) causes SCR to trigger which allows filament to spread along the width before filamentary failure and lowers the temperature across the device. Thereby, devices survive failure at higher current levels. The PNP turn-on time reduces with increase in injected current, attributed to faster rate of electron injection in the N-well region (Fig. 10). Fig. 10 compares the intrinsic LDMOS time to failure vs. injected current with PNP turn-on time in LDMOS-SCR. Intrinsic LDMOS is found to dominate the failure in a specific window of injected current. Fig. 11 summarizes various physical events explained so far which governs the failure at low currents in the LDMOS-SCR. The future work will focus on providing the design solutions to improve the power scalability by using the physical insights developed in this work.

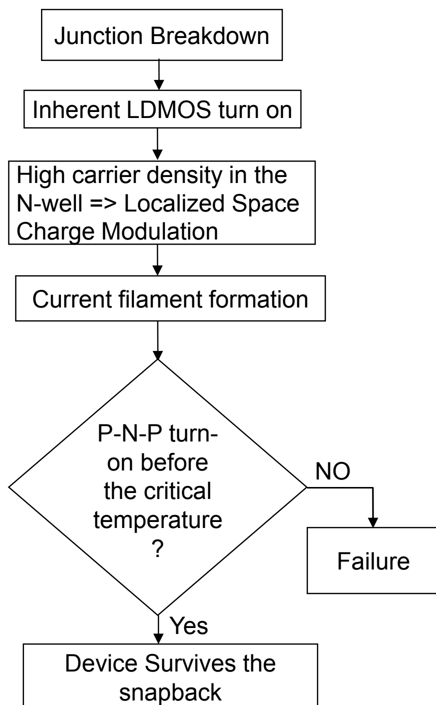

Fig. 11: Flow chart summarizing the series of physical events in LDMOS-SCR both as a function of time and injected current, leading of early failure.

IV. Conclusion

LDMOS-SCR devices were found to universally have severe power scalability issue. The devices tend to survive high current stress, however were found to fail under lower currents and longer pulses. The behavior was found to be dominated by the competition between scape charge modulation triggered filamentary action across intrinsic LDMOS device and SCR's turn-on. When the currents were high enough to form current filament across LDMOS device, however low enough to not trigger embedded SCR, LDMOS's electrical instability driven filamentary failure dominated the overall failure. However, when the currents were high enough to trigger SCR and SCR turn-on time was smaller than time for filamentary failure for a given current, SCR action drove the device to current spreading state after early filament formation. This allowed device to survive high current states, even when they fail at low currents.

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