Time Dependent Early Breakdown of AlGaN/GaN Epi Stacks and Shift in SOA Boundary of HEMTs Under Fast Cyclic Transient Stress

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***Abstract*—**This experimental study reports first observations of (i) SOA boundary shift in GaN HEMTs and (ii) early time to fail of vertical AlGaN/GaN Epi stack under fast changing (sub-10ns risetime) cyclic transient stress conditions for a 600V qualified commercial grade HEMT stack. It is shown that a stack qualified for 10 years lifetime under DC stress, fails faster under cyclic transient stress. Integrated electrical and mechanical stress characterization routine involving Raman/PL mapping and CL spectroscopy reveals material limited unique failure physics under transient stress condition. Failure analysis using cross-sectional TEM investigations reveal signature of different degradation and failure mechanism under transient and DC stress conditions. A failure model is proposed for failure under cyclic transient stress.

I. Introduction

AlGaN/GaN HEMTs promise superior switching performance than their Si counterparts. However, their reliability, in particular, under switching conditions is less explored. In a typical power converter, during OFF-cycle the high blocking voltage at drain introduces significant lateral (drain to gate) and vertical (drain to substrate) stress. While the corresponding time dependent failure physics has been widely studied, its limited however to DC like stress [1]-[5]. As a result, failure physics under practical switching conditions [6] remain broadly unclear. To enhance widespread adoption of GaN HEMTs, it is crucial to understand the failure mechanisms and estimate the lifetimes under switching conditions [7]-[12]. This work aims to contribute to the existing understanding of OFF-state stress, however under fast & cyclic pulse transient conditions, emulating real converter circuit like stress scenario. This study highlights serious implications of OFF-state transient stress during switching cycles on device's Safe Operating Area (SOA), shift in SOA boundary with accumulative stress and very small time to fail under fast transient stress conditions. The underlying degradation physics is investigated, and a unique failure model is proposed.

II. Devices Under Test

In this work two classes of HEMT devices were used: (i) commercially available e-mode GaN HEMT to study SOA and extract SOA boundary. (ii) In-house developed HEMT devices were used to study time dependent failure in GaN under vertical DC and fast transient cyclic pulse stress. Rise time (RT) of chain of voltage pulses was varied in sub-10ns range, which is typical in GaN based power converters. Stress measurements were done at different temperatures. Devices were also stressed at room temperature while giving intermediate heat treatment between stress cycles to study role of mechanical stress compensation. HEMTs were realized on a commercially available AlGaN/GaN layer stack on p-type silicon (111) substrate qualified for 600-V operation with 10-year DC lifetime (Fig. 1). Processed run had >90% device yield with variation less than ± 5%.

III. Stress Dependent SOA Boundary Shift

Figure 2 depicts a typical SOA boundary of HEMT and its degradation under pulse stress [5]-[7]. Maximum device degradation can be seen under OFF-state stress condition (Fig. 2b), which justify OFF state stress conditions, as worst-case scenario, used in this work. Figure 3 shows a shift in SOA boundary when device was pre-stressed under OFF state before extracting SOA boundary. This is unusual as such a SOA shift doesn't exist in Si power devices and was never explored earlier for HEMTs. Such an unusual SOA boundary shift sets serious limitations to the use of GaN HEMTs and therefore requires detailed explorations as presented in subsequent sections.

IV. Device Characterization

Experimental setup used in this work (Fig. 4a) tends to mimic OFF state stress scenario across HEMTs in a DC-DC converter (Fig. 4b) by applying cyclic fast transient pulse stress. High voltage pulse chain with ON time of 500ns and varying rise time was used to stress the drain contact with respect to substrate, keeping source and gate were left floating during the stress. It should be noted that OFF period between two consecutive pulses was in the order to 1s, to ensure reasonable time given for relaxation. Following measurements (Fig.4c) were carried out: (i) drain to substrate leakage current after each pulse, (ii) HEMT's DC I-V and C-V characterization, at regular intervals, to capture impact of applied stress on device parameters, (iii) μ-Raman mapping to record mechanical stress profile and (iv) UV-Photoluminescence (PL) mapping to monitor defect distribution in source-drain access with stress time, (v) Cathodoluminescence (CL) spectra at locations with high PL intensity of defect bands, to determine defect location in the epitaxial stack. Post failure SEM and TEM analysis was done routinely.

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Time to Vertical Breakdown under Pulse Stress: Time to fail (TTF) extracted using fast transient cyclic pulse stress shows exponential dependence on applied stress voltage (Fig. 5) however the TTF was found to be much smaller compared to the same under DC stress case. For instance, 600V GaN Epi-stack qualified for 10-year lifetime under DC stress, failed after ~100 pulses, each being 500ns wide. Interestingly, TTF was found to improve when pulse rise time was increased, which indicates transient time dependent failure to be related to rate of change in electrical stress. Unlike under DC stress case (Fig. 6b), under cyclic pulse stress the vertical leakage with stress time remain unchanged till the verge of failure (Fig. 6a). Rapid and more sever changes in device characteristics are observed under pulse stress compared to that under dc condition (Fig. 7). Drain to substrate vertical leakage hysteresis was found to increases with stress time under pulse stress (Fig. 8), which points to charge trapping in different layers present between drain and substrate. PL mapping of drain-source region (Fig. 9) reveals increased defect generation introducing deep level traps within energy range of E_C - 0.48 eV and E_C - 1.14 eV. Highest PL intensity is observed near the drain contact (Fig. 9c). CL spectra (Fig. 10) taken at same location verifies increase in Blue (BL) and Yellow luminescence (YL) intensities with stress and penetration depth of ~1.2 μm from top surface. Hence, defects in GaN buffer are located close to 1.2 μm below surface in the drain contact vicinity. Raman map confirms mechanical stress builds up at the drain contact edge after the device is stressed for 5000 cycles under pulse condition (Fig. 11). Since AlGaN is transparent to used visible (532 nm) laser, the stress signature received is from GaN buffer. This correlates well with penetration depth calculated from CL. Post failure cross-sectional SEM shows a catastrophic damage in GaN buffer, in vicinity of drain contact (Fig. 12). HR-TEM of defected region reveals fine cracks near GaN buffer and AlGaN transition interface (Fig. 12). However, under DC stress, damage is localized to device surface and no failure signature is observed in the bulk.

V. Discussion and New Physical Insights

Understanding Failure Under Cyclic Transient Stress: Under time dependent drain-to-substrate DC stress, the devices show a time-dependent failure (Fig. 1) with strong field dependence. Failure is believed to occur via percolation paths between drain and substrate formed by defect activation at high electric field [3]. Exponential dependence of TTF on pulse stress voltage, shows field dependent failure mechanism similar to DC stress condition. However, the defect percolation theory (borrowed from gate dielectric failure models) cannot explain significantly reduced TTF, its dependence on rise-time (Fig.5) and aggressive catastrophic failure (Fig. 12) under cyclic transient stress condition. These newly discovered trends and findings indicate an electrical shock-based fatigue phenomenon responsible for time dependent GaN Epi stack failure. Electrically developed fatigue was earlier reported for piezoelectric materials [13]. This can be explained as following: when, a voltage stress is applied across the stack vertical component of electric field (E_Z) introduces piezoelectric in-plain strain in AlGaN/GaN layers which is given by [14]: $\sigma_{XY} = \left(e_{33}\frac{C_{13}}{C_{33}} - e_{31}\right)E_Z$. Here, σ_{xy} is in-plane strain, e_{33}, e_{31} are piezoelectric coefficients and, C_{13}, C_{33} elastic stiffness tensors. Piezoelectric strain generates defects in bulk region, in drain contact vicinity, where peak field lies and accumulates with increasing number of stress pulses (Fig. 11b). Furthermore, under pulse stress, the piezoelectric AlGaN/GaN stack undergoes cyclic loading via mechanical strain generation-relaxation as evident from the Raman map, captured before and after pulse stress (Fig. 11). Over time, cyclic stress causes changes in piezoelectric properties [13] and results in time dependent strain variation [15]; $\sigma_{XX}(t) = \sigma_0\left(1 - e^{\frac{-t}{\tau}}\right)$. Such an electrical fatigue is accumulative in nature as evident from increased YL, BL bands in CL spectra (Fig. 10) and increased hysteresis (Fig. 8) over time. Electrical fatigue nucleates micro-cracks at GaN buffer/AlGaN transition interface which has highest residual stress (Fig. 12). High strain energy at crack tip under cyclic electrical loading propagates it towards device top and hits the surface to form pits and causes catastrophic failure (Fig. 12). Fatigue accumulation accelerates with rate of change of electric field (pulse rise time), resulting in drop in TTF for faster cyclic transients (Fig. 5).

Validation of Proposed Failure Model: Stress accumulation and defect generation in GaN epi layers under pulse condition occurs due to electrical cyclic loading via compressive piezoelectric stress. Heating in device introduces thermoelastic tensile stress [16] which partially relaxes the field induced piezoelectric stress, as confirmed using Raman mapping (Fig. 16). This resulted in TTF improvement when stress applied at higher temperature or heat treatment was given in between cyclic stress (Fig. 17).

VI. Conclusion

Shift in SOA boundary under pulse stress was found, which is uncommon in Si power devices. Vertical drain to substrate breakdown in GaN Epi-stack under fast and cyclic pulse stress was found to obey different degradation physics than DC stress. TTF extracted for GaN Epi-stack from fast, cyclic pulse stress measurements did not obey the lifetime predicted by DC stress. Time to fail, under pulse stress showed exponential dependence on stress voltage, which however increased with pulse rise time or temperature. Cyclic electrical loading invoked electric fatigue in buffer. Defect density increased in buffer with stress time due to accumulative nature of fatigue. Increased deep level defects deteriorated device performance. Under pulse stress, cracks nucleated at GaN-buffer/AlGaN-transition region, triggered device failure. Failure under DC stress occurred close to device surface and with no signature of damage in bulk.

References: [1] Warnock et. al. IEEE TED, pp. 3131, 2017, [2] M.Meneghini et. al. APL,pp. 33505(1), 2012, [3] M.Meneghini et. al. IEEE TED, pp. 2549, 2015, [4] M.Borga et. al. IEEE TED, pp. 3616, 2017, [5] M. Borga et.al. IEEE TED, pp. 1-6, 2018, [6] S.Bahl et. al. IRPS 2016, pp. 4A.3, [7] Ikoshi et. al. IRPS 2018, pp. 4E-1, [8] Huang et. al. ISPSD, 2014, pp 273-276, [9] A.Castellazzi et. al. IRPS 2018, pp. 4E-1, [10] B.Shankar et. al, IRPS 2017, pp.WB5-1, [11] B.Shankar et. al, IRPS 2018, 4E.3, [12] B.Shankar et. al, IRPS 2018, pp.4E.4, [13] Glaum et. al. J. Am. Ceram. Soc., pp. 665, 2014, [14] Sarua et. al, Semicond. Sci. Technol. 085004, pp. 1-8, 2010, [15] Chung et. al. Mater.Res.Exp.3, 105026, 2016, [16] J.P. Jones et.al, ITHERM 2014, pp. 959

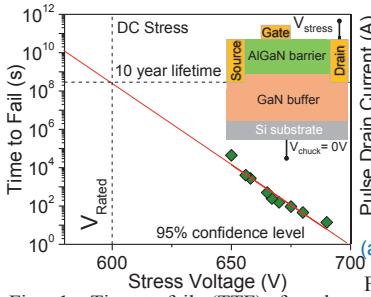


Fig. 1. Time-to-fail (TTF) for the commercially available 600V AlGaN/GaN stack (used in this work) demonstrating 10-year lifetime for 600V dc stress.

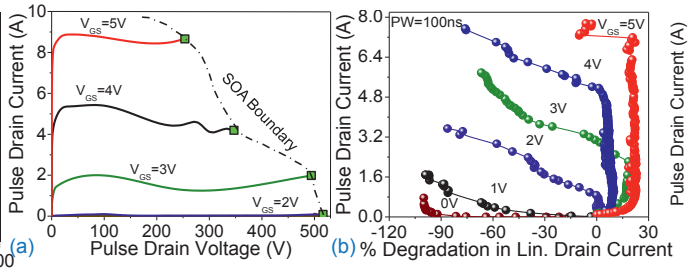


Fig. 2. Typical safe operating area (SOA) and resulting device degradation GaN HEMTs. (a) Fast pulse I-V characteristics depicting SOA boundary of a commercially available e-mode HEMT device. (b) Percentage change in linear drain current (on x-axis) measured after each voltage/stress pulse. Under OFF state stress condition, device shows highest degradation.

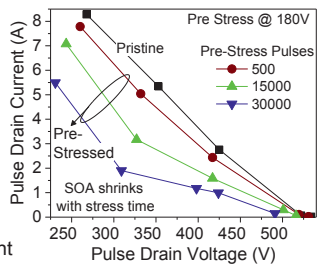


Fig. 3. SOA of commercial e-mode GaN HEMT, extracted at different stages of OFF-state stress cycles. Set of devices are pre-stressed for different no. of pulses before extracting SOA boundary. Shift in SOA boundary as a function of stress can be seen.

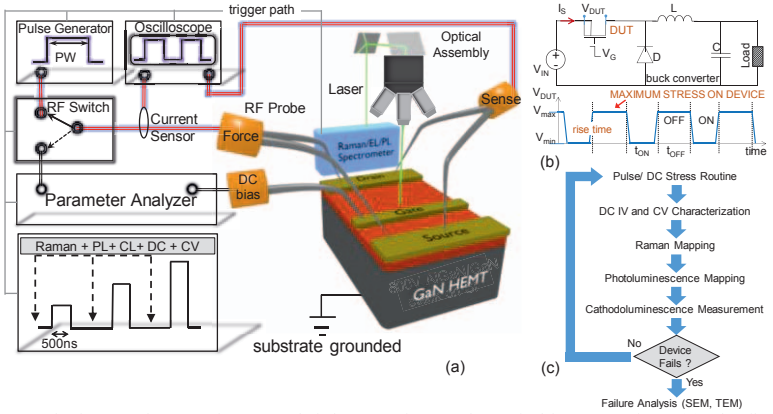


Fig. 4. (a) Schematic of experimental setup with integrated Raman, PL and sub-µs pulse generator used for on-the-fly electrical and material characterization of HEMT/Epi-Stack under dc and pulse stress conditions. Electrical stress routine (dc and pulse) was interrupted at regular intervals, to record, evolution of mechanical stress profile using visible Raman (λ=532nm) and defects density distribution using UV-PL (λ=325nm) across the active region. CL spectra was also captured in gate-drain region at different stress time. Inter-pulse dc IV and CV characterization was also done to record variation in device parameters with stress time. (b) Schematic representation of a buck power converter showing device voltage (V_{DUT}) waveform during switching. Maximum voltage stress appears across the device during the OFF-cycle of the converter. Hence, pulse stress degrades the device performance with each cycle. Hence device's safe operating area shrinks over time under switching operation. (c) The flowchart represents the sequence of various types of device and material characterizations performed during pulse and dc stress routines.

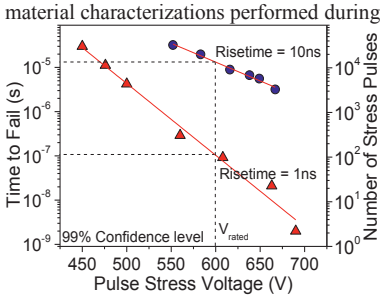


Fig. 5. Time to fail (TTF) under pulse stress conditions presented on left y-axis and the corresponding number of pulses required for device failure at different voltages, shown on right side y-axis. Here pulse width of 500ns and OFF state period between two consecutive pulses are 100µs. Figure depicts, TTF is significantly lowered under pulse operation compared to that under dc and exhibits dependence on the rise time (slew rate) of the stress pulse.

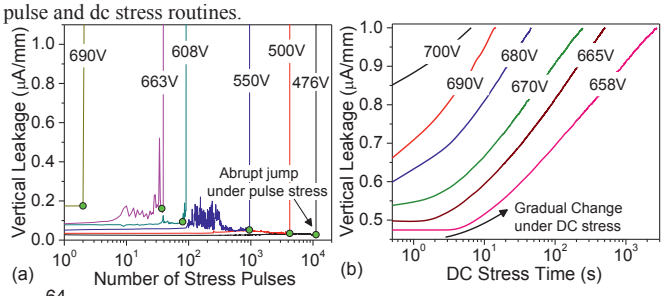


Fig. 6. (a) Time evolution of vertical (drain to substrate) leakage current at different (a) pulse voltages and (b) dc stress voltages. Under pulse condition the leakage remains unchanged until the hard breakdown point where it increases abruptly. On the other hand, it increases gradually under DC stress.

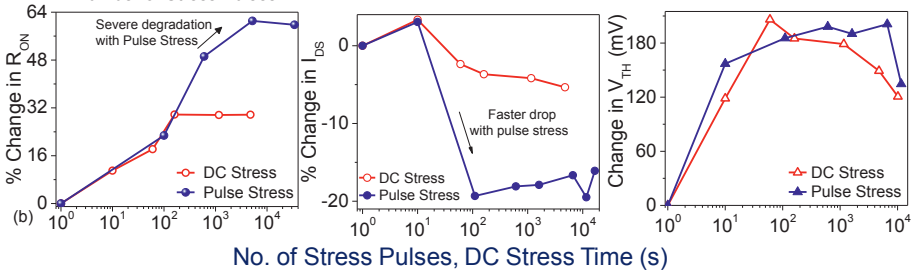


Fig. 7. Degradation in the device parameters recorded on-the-fly during dc and pulse stress measurements done at 185V. (a) ON-resistance (R_{ON}) increases and (b) ON-current (I_{ON}) decreases at a much faster rate under pulse stress condition when compared to DC stress. With stress time, the density of deep levels in GaN increases, as evident from increased Yellow luminescence and Blue luminescence in Fig. 10, which electrostatically influence 2DEG and increase R_{ON} and lowers I_{ON}. Threshold voltage instability gets accelerated under pulse stress. For instance, with just ten stress pulses applied on drain, the V_{TH} changed by 180mV as evident in (c).

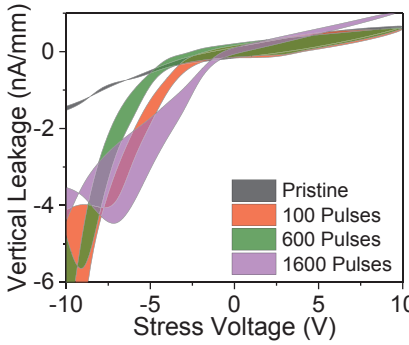


Fig. 8. Hysteresis behavior recorded between drain and substrate current after different number of stress cycles (pulse stress voltage = 200V). Increase in loop area highlights charge /trap accumulation in buffer and transition regions with each stress pulse, attributed to increased density of defect in bulk GaN. This correspond to blue and yellow luminescence as visible from broadened FWHM of defect band (400-600nm) in CL spectra of GaN recorded close to drain edge. Carrier de-trapping is slow from deep levels, which results in accumulation of trapped charges in buffer layers with increasing stress cycles. This translates to increased hysteresis.

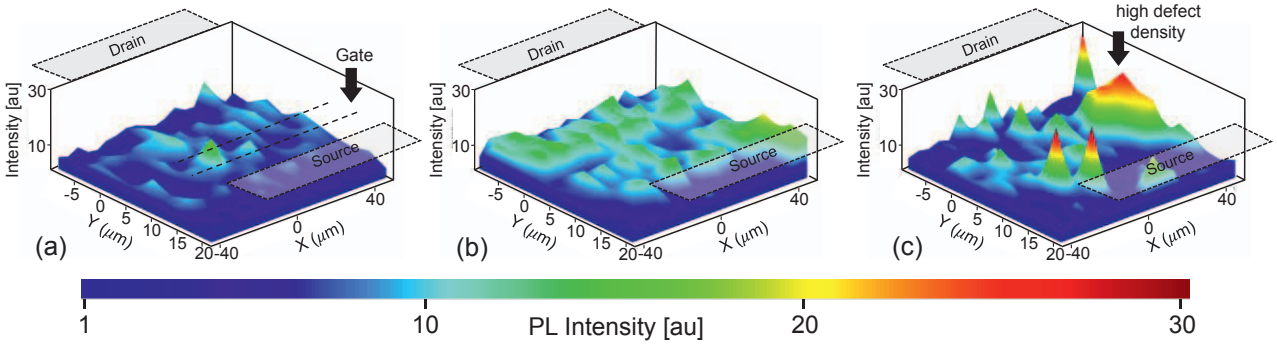


Fig. 9. PL intensity distribution for defect band (425-525nm) captured between source-drain region of the HEMT device (a) before stress, (b) after stressing with 5000 pulses and (c) at the verge of failure. Figure reveals that the density of mid-bandgap defects, increases with number of pulses (of 200V) with peak concentration close to drain contact edge.

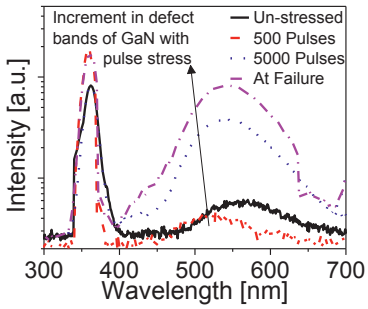


Fig. 10: CL spectra of GaN captured between gate - drain region. FWHM of the defect band (400nm-600nm) increases with number of stress pulses (@ 200V) applied at drain with substrate grounded. It reveals increased density of deep levels under pulse stress.

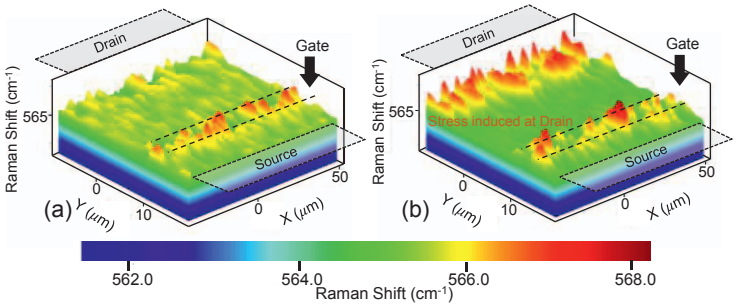


Fig. 11. (a) Raman map captured between source - drain region of pristine device, i.e. before applying stress. Figure reveals residual compressive stress in recessed region under gate. (b) Raman map of the device after application of 5000 stress pulses (@180V) between drain and substrate. Stress accumulation can be noticed near the drain contact edge, beside gate finger.

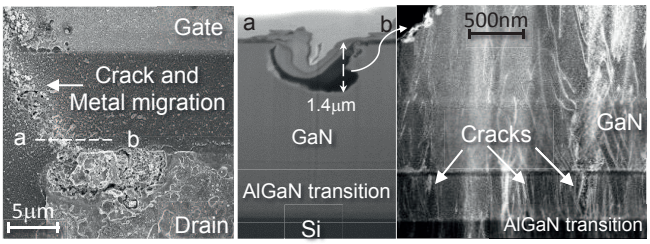


Fig. 12. (a) Top view SEM image depicting HEMT device failed under 600V pulse stress condition. Failure occurred with massive crack in the gate-drain region. (b) Cross-sectional SEM taken along line a-b reveals that the damage reached 1.4 micron deep into GaN buffer. (c) HR-TEM image of the region below damage area depicts cracking at the interface of GaN buffer/AlGaN-transition region.

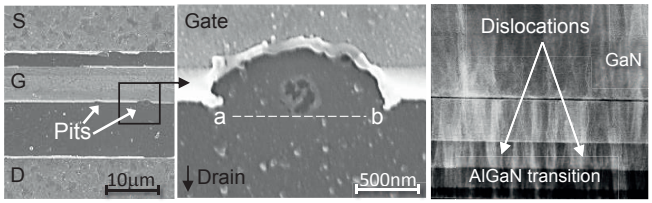


Fig. 13. (a) Top view SEM images of HEMT device failed after 600V of DC stress depicts shallow damage confined to top surface. (b) Cross-sectional TEM along a-b line shows no damage in bulk along dashed line 'a-b', reveals the failure occurred in device's active region close to AlGaN/GaN interface at the top. No signature of bulk failure found. Similar localized failures observed in other dc stressed devices near top surface.

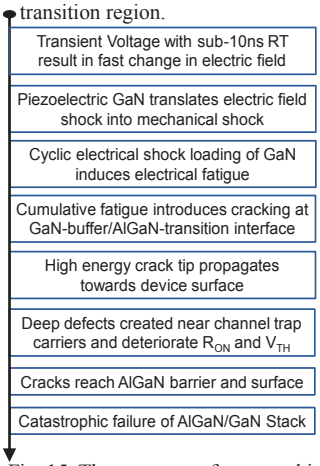


Fig. 15. The sequence of events which are responsible for Fast Transient Stress Assisted Time Dependent Breakdown and Shift in SOA Boundary of AlGaN/GaN Epi Stacks & HEMTs.

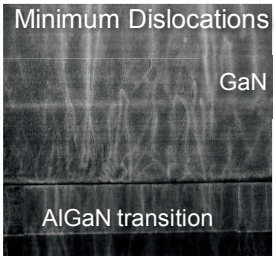
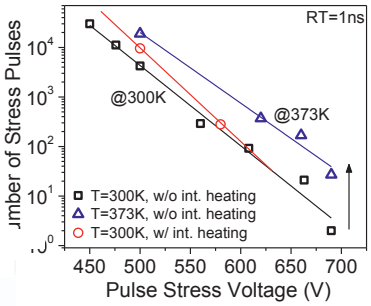


Fig. 14: TEM image of a pristine device taken under the drain depicting least dislocation density. Therefore, it can be said that failure under dc stress occurs via dislocations which are leakage path

Fig. 17. Variation in vertical time-to-fail under pulse stress, recorded at different temperatures treatment. The increase in temperature, improves the TTF.



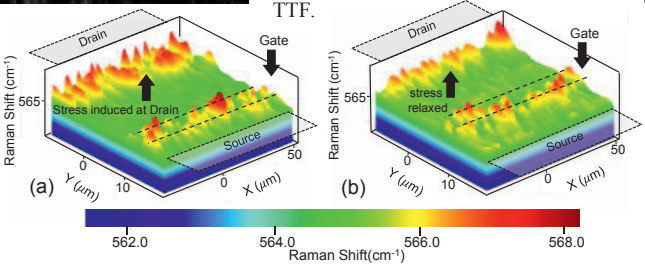


Fig. 16: (a) Post stress Raman map device stressed using 5000 pulses depicts stress accumulation around drain contact. (b) Relaxation in device stress, confirmed from Raman map captured, after the device was heated at 100°C for 10 mins post pulse stress