Comprehensive Computational Modelling Approach for Graphene FETs

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***Abstract*—Graphene has shown a great scope beyond the bulk silicon devices for future transistor applications. Even though it has undergone intensive investigations through experimental approach, there are no easy and time efficient computational approaches for analysing the graphene transistors. In this paper we provide methodology for simulating graphene transistors using conventional TCAD tools with appropriate model calibration. We demonstrate the calibration methodology along with few graphene FET simulations with the calibrated set-up.**

***Index Terms*—Graphene FET, Graphene Simulation, Graphene TCAD Simulation**

I. Introduction

Graphene a carbon based material has become of great interest beyond the silicon devices due to its ability to provide high mobility carriers and ballistic transport even at larger channel lengths. Theoretical estimations provide mobilities greater than 10000 cm^2/Vs [1]–[3]. Experimental investigations on graphene FET have been so intense that the state of art has shown considerable improvement in the transistor performance. For studying the transistor characteristics theoretically, there has been a great bottleneck from the number of computations. The conventional tools such as Atomistic Tool Kit, Vasp used for studying the atomic scale materials like graphene require intense computations for studying the transistors even for the dimensions of transistors closer to 20nm. Quantum mechanical models are used for computations at atomic scale, where the computational complexity increases exponentially with dimensions. Transistors made of bulk semiconductors like Silicon, III-V compound semiconductors can be analysed fairly well using the Technology Computer Aided Design(TCAD) Tools. TCAD Tools use semi-classical approach to analyse the transistor characteristics, which reduces the computational complexity to a great extent when compared to the quantum mechanical models. Reduction in complexity aids in analysing the transistors with the dimensions reaching even close to millimetres in adequate time. In this manuscript we present a method to simulate the characteristics of the graphene FET using the TCAD Tools. This approach is able to match the characteristics fairly well with experimental data, making the approach more efficient. Models used in this approach are general models used for the bulk semiconductors, making it easier to adopt into any TCAD Tool.

The complete paper is organised as follows. The next section "Experimental Studies" provides the details of the device structures used and data extraction methodology. Section III provides the details of models, fitting parameters and their evaluation from experimental data. The details of fine tuning of these parameters for matching the transistor characteristics to experimental data are also provided in this section. Section IV concludes the work and provides the details of the future work.

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II. Experimental Studies

For extracting different parameters from the experimental data one of the best performing TLM structure has been selected from the experimental data. These parameters have been used for fitting the parameters of the different models required for the simulation. TLM Structure includes many transistors with different channel lengths as shown in the Fig. 1, which are used for extracting the contact resistance. Fig. 2 shows the cross section of the graphene FET used for the experimental study in the TLM structure. Cross section includes heavily doped Si substrate which serves as a back gate, 285nm silicon oxide used as a back gate dielectric, graphene monolayer channel grown by CVD, e-beam evaporated Palladium(Pd) metal contacts for source and drain electrodes. TLM structure parameters are given in the Table I. These structures have been replicated in TCAD and are simulated to study the characteristics.

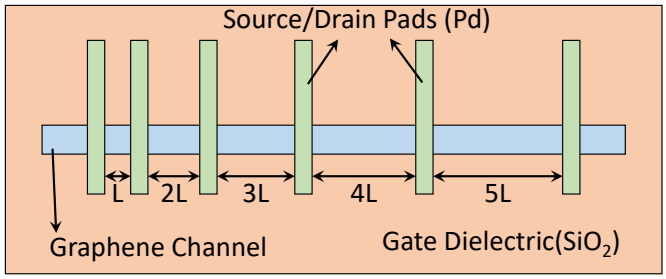

Fig. 1. Top view Schematic of the TLM Structure used for the experimental study.

TABLE I
Parameters of the TLM Structure experimentally prepared.

Parameter	Value
Channel length L_G	1-5 μm
Source/Drain Height H_{SD}	70nm
Source/Drain Length L_{SD}	300nm
Gate oxide thickness t_{OX}	285nm

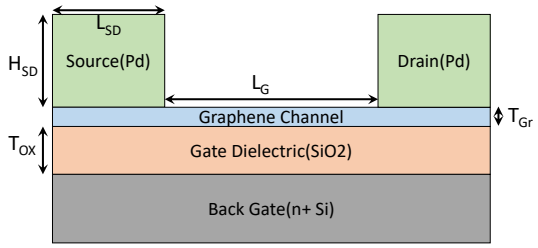

Fig. 2. Schematic cross section view of the graphene FET used for experimental study.

From the TLM structure contact resistance has been extracted. Value of Maximum mobility of the carriers and channel electric fields are evaluated from eqn (1) and (2) using the transfer characteristics of the device and the extracted contact resistance.

$$\mu = \frac{C_{OX} \cdot L}{W \cdot V_{DS}} \cdot \frac{dI_D}{dV_{GS}} \tag{1}$$

$$E_{Ch} = \frac{\frac{I_D}{V_{DS}} - 2R_C}{L_{Ch}} \tag{2}$$

III. Simulation Strategy and Parameter Fitting

For efficient evaluation of characteristics of a device we need to calibrate the simulation set up to the experimental characteristics. For graphene parameter evaluation, we first focussed on calibrating the parameter mobility, which determines the ease at which the carriers move inside a material. Mobility is influenced by many parameters like doping, defects and particularly electric field at shorter channel lengths. We focussed on calibrating the mobility against the electric field effects. For FET, the effect of electric field is from two sources, one from drain field and the other from gate field. Drain field is responsible for the carrier velocity which determines the current in the device. Current density in a semiconductor device is given by the eqn (3)

$$J = nqv_d \tag{3}$$

Here n is the majority carrier density, q is the electron charge and v_d is the drift velocity of majority carriers. Drift velocity increases linearly with drain field at low electric fields, and then gradually saturates to a value specific to the material and the carrier type. The effect of saturation of velocity is called velocity saturation, which is usually accounted in simulations using High field saturation models. Different models can be used to incorporate this effect. Here we use Extended Canali model [4] for calibrating the graphene mobility against high field saturation effects. The model is represented by the eqn (4) given below.

$$\mu(E) = \frac{(\alpha+1)\mu_{low}}{\alpha + \left[1 + \left(\frac{(\alpha+1)\mu_{low}E}{v_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \tag{4}$$

In the equation, μ is the mobility, E is the electric field, v_{sat} is the saturation velocity, α and β are the fitting parameters. Contact resistance is extracted from the TLM structure with five different channel lengths from 1-5μm. Using this contact resistance, electric field across the channel is evaluated using the eqn (2), which is responsible for mobility degradation as well as carrier velocity saturation.

Fig. 3 shows the fitting of experimental characteristics against the Extended Canali model using MATLAB. Using this fitted model different parameters of the model have been extracted and are summarized in the Table II

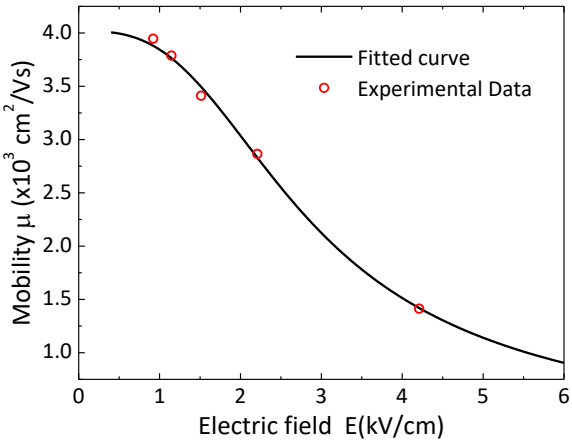

Fig. 3. Fitting of experimental data using the model and the corresponding parameters

TABLE II
Fitted parameters of the extended Canali model using the experimental data.

Parameter	Value
Alpha α	-0.62
Beta β	2.97
Saturation velocity v_{sat}	4.1x10^6 cm/s

Fig. 4 shows the comparison between simulated input characteristics using the field effect mobility extracted corresponding to the channel length, with the experimental characteristics. Characteristics show the same trend as that of experimental except for the exact values and the slight deviation of trends from the experimental currents at higher voltages.

To match the trends even at higher gate bias we need to go for calibration of mobility degradation at higher gate biases. For this we consider Enhanced Lambardi Model [5] with the degradation from the surface, which is given by eqn 5 and eqn 6.

$$\frac{1}{\mu} = \frac{1}{\mu_{Low}} + \frac{D}{\mu_{ac}} \tag{5}$$

where μ_{ac} at room temperature is given by

$$\mu_{ac} = \frac{B}{E_{norm}} + \frac{C(N_{A,0} + N_{A,0} + 1)^{\lambda}}{E_{norm}^{\frac{1}{3}}} \tag{6}$$

Using this model mobility variation against gate electric field at higher gate bias has been fitted. Fig. 5 compares

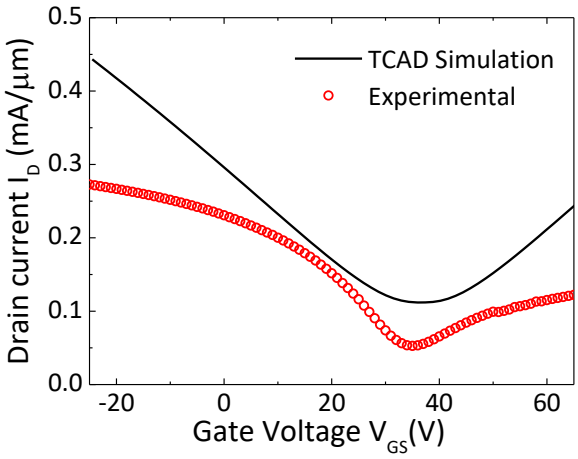

Fig. 4. Comparison of simulated input characteristics of FET against the experimental characteristic. Note that the dirac points have been adjusted to 0V for proper comparison of the trends.

the fitted characteristics (using MATLAB) against the experimental characteristics. The parameters of fitted model are summarized in the Table III. These parameters will be used for the simulation of graphene FET characteristics for various studies.

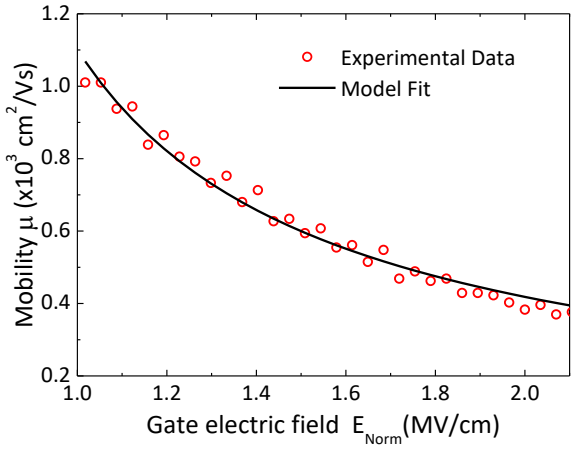

Fig. 5. Comparison of Enhanced Lambardi model fit against the experimental characteristics. Characteristics show better match through out the field range.

TABLE III
FITTED PARAMETERS OF THE ENHANCED LAMBARDI MODEL AGAINST THE EXPERIMENTAL DATA.

Parameter	Value
B	9.42E+6
C	-56.8
D	1.247
Lambda λ	0.309
$N_{A,0}$	0.805
$N_{D,0}$	0.805

Currently the parameters for the effects of both the fields have been obtained using the corresponding models. These models are already available in TCAD for the other materials like Silicon. For simulating the graphene FET characteristics these parameters will be replaced in the place of silicon material parameters for the corresponding models. These parameters will be further fine-tuned for better matching of the FET characteristics against the experimental data. These fine-tuned parameters using the above two models will finalize set up for graphene FET simulations. Fine-tuning of these parameters happens in two stages. First stage is simulating the characteristics by replacing the basic silicon material parameters with the extracted and fitted parameters in the corresponding model. In this stage simulated and experimental characteristics are compared, and a set of experiments are designed to nullify the differences. For the first model in consideration Fig. 6 shows the comparison between initial characteristics obtained from the simulation and the experimental characteristics.

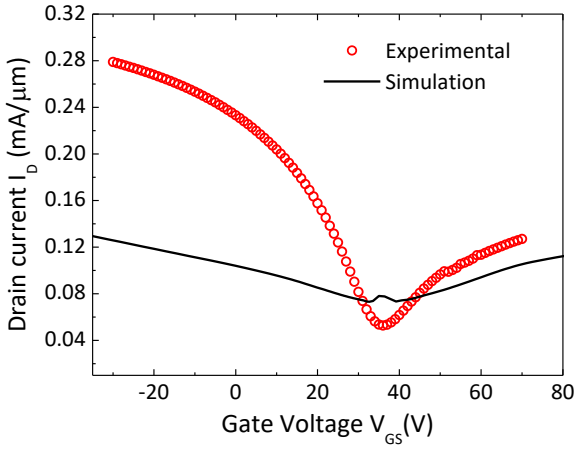

Fig. 6. Comparison between the characteristics of the Graphene FET simulated with the fitted parameters against the experimental characteristics.

For matching the characteristics there is a need for increment in the currents of the device obtained through the simulation. The parameters mobility and the saturation velocity obtained from fitting are low when compared to the theoretical evaluations present in the literature. Hence these parameters have been increased to rise the cur-rents through the device. After rising these parameters and fine-tuning along with other parameters the characteristics of the device have been compared in Fig. 7 with the experimental data. The characteristics obtained through this method shows a better match against experimental data explaining the efficiency of the method employed.

Even though the above characteristics look matching, the set-up is not complete as it doesn't include the effect of gate field. In the next step the characteristics have been further fine-tuned with the Normal field effect calibration. When the normal field effect model is included characteristics found to be similar to the one presented in Fig. 6. This required the further calibration of fitted parameters of both high field saturation model and Normal Field Effect Models. Fig. 8 compares the experimental and the simulated characteristics after calibrating both High Field Saturation and Normal Field Effect Models. Input characteristics show better matching everywhere except

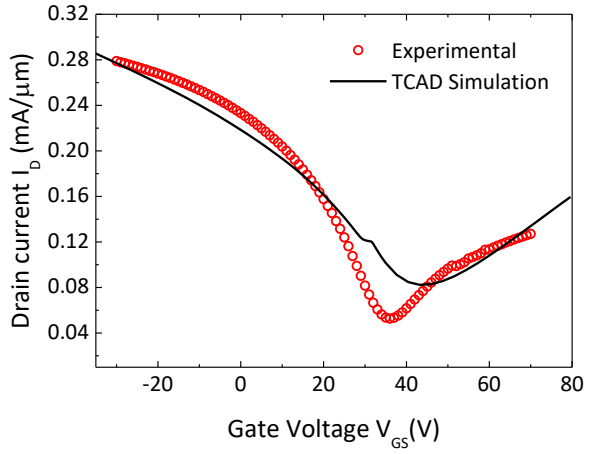

Fig. 7. Comparison of Simulated characteristics of the Graphene FET after fine-tuning the parameters of the High Field Saturation Model against the experimental data.

around Dirac point. With this set-up performance of the long-channel devices can be estimated fairly and with less time compared to the other tools being used for the simulation of Graphene FETs.

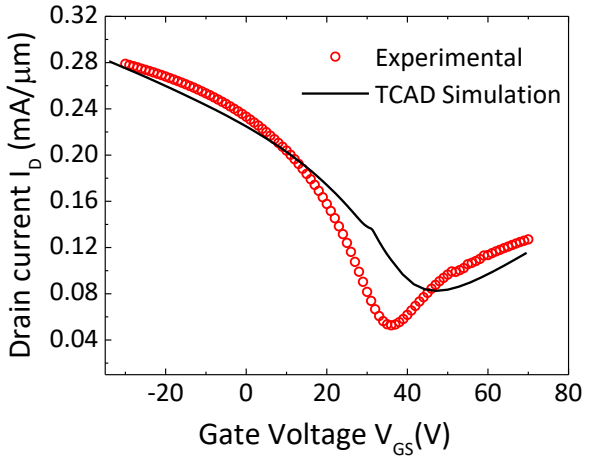

Fig. 8. Comparison of Simulated characteristics of the Graphene FET after fine-tuning the parameters of the Normal Field Effect Model against the experimental data.

With an aim of knowing how the set up will work, RF simulations have been carried out for the schematic shown in Fig. 9. Structural parameters of the schematic are summarized in Table IV. When compared to the experimental structure oxide thickness and the overlap of gate with source and drain electrodes have been reduced for better RF performance. One of the RF performance metric unity gain frequency(f_T) has been extracted corresponding to the channel length variations and is compared in the Fig. 10. f_T increases almost exponentially with the decrease in channel length and tends to drop at very low channel lengths. Maximum unity gain frequency of 170GHz has been found for the channel length 40nm. Further optimization of the structural parameters can give the better f_T values ranging in 1-2 THz, as estimated theoretically for Graphene FETs.

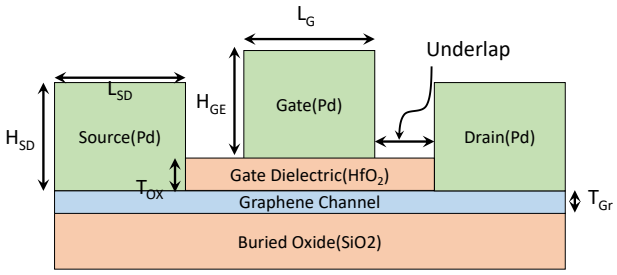

Fig. 9. Schematic of the graphene FET used for RF simulations.

TABLE IV
STRUCTURAL PARAMETERS OF THE GRAPHENE FET USED FOR RF SIMULATIONS. ALL THE STRUCTURAL PARAMETERS HAVE BEEN REDUCED FROM THE EXPERIMENTAL STRUCTURES FOR ACHIEVING BETTER PERFORMANCE.

Parameter	Value
Channel length L_G	20, 40, 80, 100 nm
Source/Drain Height H_{SD}	70nm
Source/Drain Length L_{SD}	70nm
Gate oxide thickness t_{HFO_2}	3nm
Under lap	7nm
Gate Electrode Height H_{GE}	70nm

Current set-up as calibrated for long channel devices works very efficiently at longer channel lengths. To increase the efficiently at very low channel lengths needs the calibration of quantum confinement and ballistic transport models against the experimental data of lower channel length devices. We are currently preparing the lower channel length devices experimentally, data from which will be used for further calibration of the set-up by including these models.

IV. Conclusion and Future Work

Proposed method has shown the potential of TCAD Tools for simulating graphene FET Characteristics. Fitting of model parameters of mobility experimental values has given the

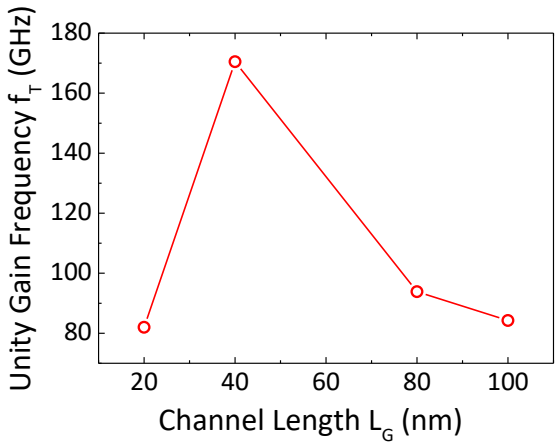

Fig. 10. Simulated variation of Unity gain frequency with channel length. f_T increases exponentially with decreased channel length except for 20nm L_G, where increased parasitic capacitances inhibit the performance rise.

better match of simulation characteristics, against experimental values, there by enabling the use of TACD tools for studying the characteristics of graphene FETs. Evaluated parameters have been further fine tuned to better match the simulation characteristics against the experimental characteristics, thee by increasing the accuracy. Currently the set-up is ready for long channel device simulation of Graphene Transistors, where the other Tools require very large amount of time. Further calibration will be done by including quantum confinement and ballistic transport models, to increase the efficiency of the set-up at very low channel lengths.

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