Physical Insights into the ESD behavior of Drain Extended FinFETs

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Abstract - In this paper, physical insights of Drain extended FinFET under ESD stress condition is explored. Key features like bipolar triggering, conductivity modulation and localized hot spot formation pertaining to DeFinFET failure mechanism are discussed comprehensively. Non-uniformity and filament formation in multi-finger DeFinFET is explored.

I. Introduction

Drain extended FinFETs essentially aim to provide high voltage (HV) FinFET based integrated technology for System on Chip (SoC) applications such as DC-DC convertors, level shifters etc. [1,2]. The planar counterpart, high voltage Drain extended MOS (DeMOS) devices were highly prone to ESD stress conditions due to filament formation and hot spots driven by non-uniform current distribution [3]. Failure signature are seen through metal migration or meltdown, as well as semiconductor fusing off. Several works have been reported, discussing the failure mechanism in De-MOS devices [4, 5], and the space charge modulation, a physical phenomenon was considered as the key role in forming non-uniformities in the current conduction [6,7]. Device design and processing of HV device for FinFET integration can be adapted through the planar DeMOS technology, with an introduction of additional mask for high voltage wells, in a standard process flow of FinFET technology. Performance and through put can be estimated conservatively from the state of art know-how. However, no significant study has reported till date estimating the ESD reliability of DeFinFET devices. This work highlights a detailed physical behavior of DeFinFET devices with various regimes of operation under Transmission Line Pulsing (TLP) stress. Non-uniform current conduction in the multi-fin arrangement of DeFinFET under ESD stress condition is studied.

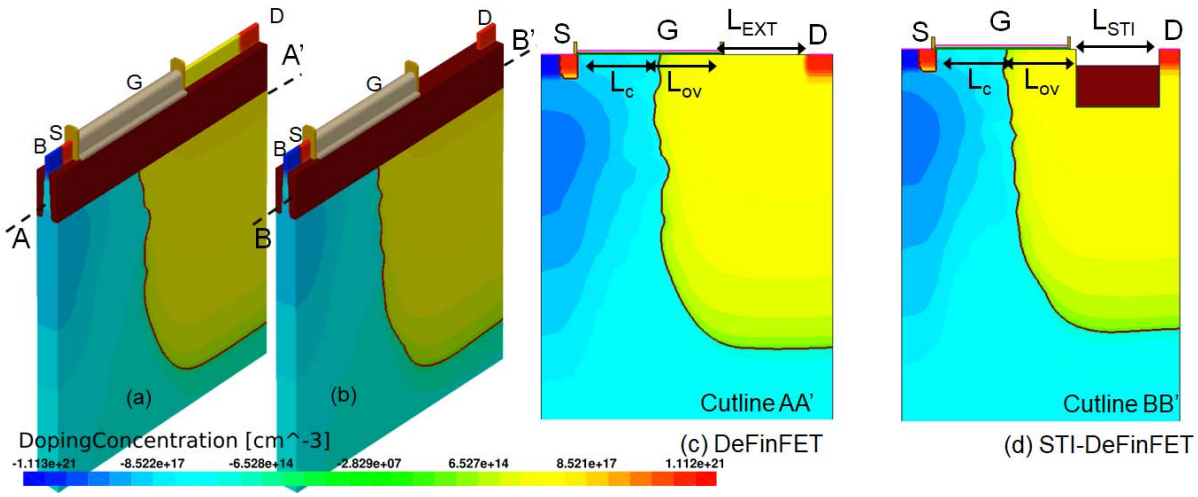

Figure 1: 3D view showing the doping concentration of high voltage wells of (a) Drain Extended FinFET (DeFinFET) and (b) STI-DeFinFET where a shallow trench isolation (STI) is incorporated between the gate and drain, (c) and (d) depicts the cross-sectional view of DeFinFET and STI-DeFinFETs respectively.

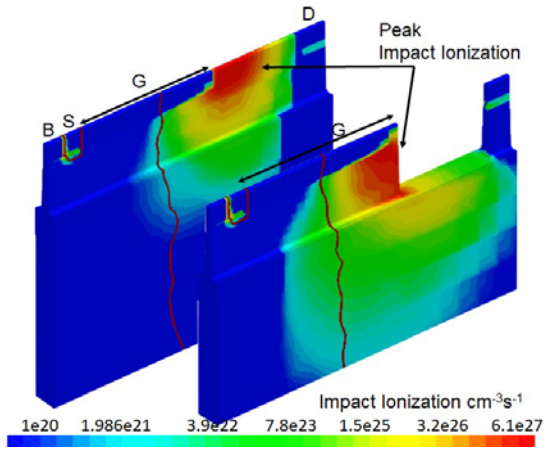

Figure 2: Impact Ionization of DeFinFETs, inset points towards the peak impact ionization position of DeFinFET and STI-DeFinFET.

II. DeFinFET Device Design & TLP Behavior

Fig. 1 shows the description of De-FinFETs. HV Wells of the device are implanted and annealed using Sentaurus TCAD Process simulations. A composition of HfO2 and SiO2 is used as gate oxide with effective oxide thickness of 1.1nm and TiN as gate metal is used with fin to fin pitch of 50nm. A highly doped drain is kept afar from the gate for high voltage functionality of DeFinFET with (L_{EXT}) and STI separation (L_{STI}) for STI-DeFinFETs. A P-type well is implanted deeper under the active fin, while keeping the channel region moderately doped. Source and body of the device are contacted in P-well and drain is contacted through N-well. The gate overlap (L_{OV}) is extended over the N-well region to reduce the surface field. Drain extension (L_{EXT}) and trench isolation (L_{STI}) for DeFinFET and STI-DeFinFET respectively is opted to achieve desired breakdown voltage. Contacts of the device are thermally terminated with 10-micron equivalent metal interconnect thermal resistance for conservative lattice heating estimation. Silicon depth of 4-micron is used to capture heat diffusion into the bulk. The device physics is studied using drift diffusion model calibration simulation deck [2, 8]. All the subsequent analysis of ESD behavior is studied using a model calibrated simulation deck.

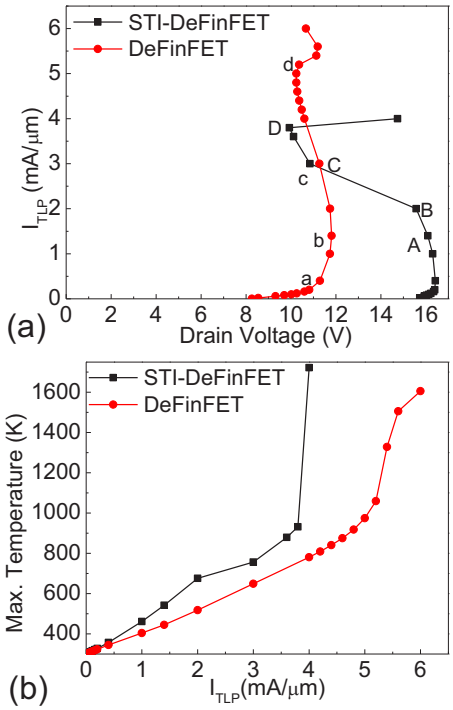

Figure 3. (a)TLP-IV characteristics of drain extended devices (b) Lattice Temperature vs TLP current. (lower-case alphabets correspond to DeFinFET & uppercase for STI-DeFinFET).

A. TLP Behavior of De-FinFETs

1. Junction Breakdown

Unlike a conventional planar equivalent DeMOS, the electric field in a DeFinFET is confined between gate edge and drain contact due to the fin topology

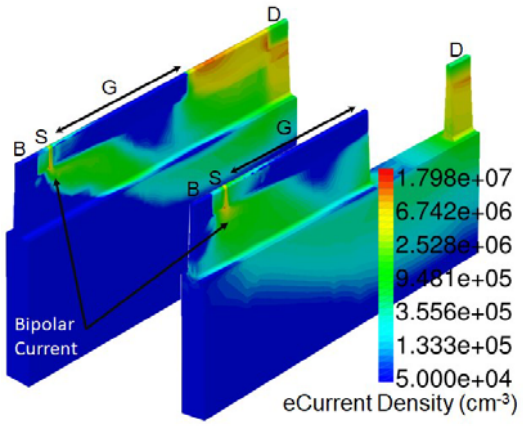

Figure 4: Injection of electron current through the source terminal under transient ESD current stress depicts the onset of bipolar triggering.

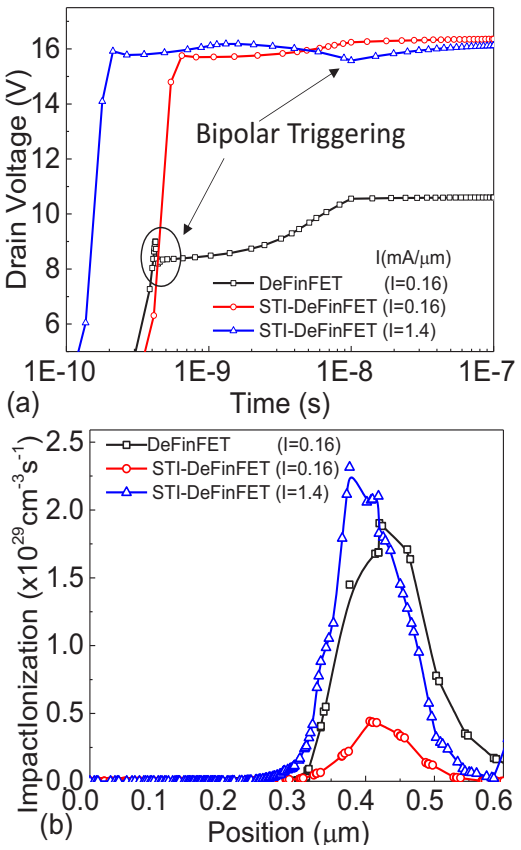

Figure 5: (a) Drain voltage vs transient time of DeFinFET devices. Snapback in voltage w.r.t time depicts the bipolar triggering. STI-DeFinFET takes higher current and longer time to trigger. (b) Peak impact ionization at the junction between P/N well (data is extracted under the STI). Note: STI-DeFinFET higher current stress to generate carriers from impact ionization.

[2]. Therefore, the peak impact ionization position of DeFinFET & STI-DeFinFET falls under the drain overlap/edge of the devices as depicted in Fig. 2. Moreover, having STI in the N-Well enables the de vice to sustain higher voltage. Fig. 3(a) shows higher breakdown voltage of STI-DeFinFET. However, due to STI in the drift region the power density of the device stands higher than in DeFinFET at a given current stress. Therefore, the failure current for STI-DeFinFET is significantly lowered due to excessive lattice heating.

2. Bipolar Triggering

A parasitic BJT is formed between N+ source, P-well and N-well. TLP current value at data point 'a' in Fig. 3(a) refers to the bipolar triggering. From

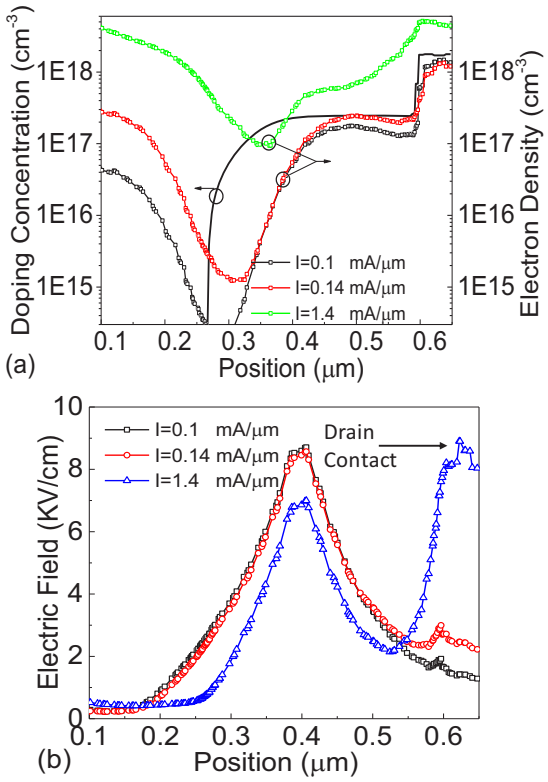

Figure 6: (a) Background doping of the drift region and electron density flooding the drift region for different current values. (b) Shift in the peak electric field towards drain contact depicts the conductivity modulation.

Fig. 2, holes generated by the impact ionization, migrate towards the body terminal and raises the well potential underneath, which in turn triggers the bipolar. Fig. 4 depicts the bipolar triggering by providing the electron current from the source terminal. Fig. 5(a) shows the transient analysis of TLP voltage w.r.t time. In DeFinFET, a snapback of voltage within 1ns is observed due to BJT triggering.

However, in case of STI-DeFinFET, longer time (10ns) and higher current is required to trigger the bipolar action. This is attributed to a lower impact ionization at a given current as shown in Fig. 5(b) and is due to the presence of STI. In STI DeFinFET the conduction of current goes deeper under the STI, which keeps the current density lower at the surface of the fin, contrary DeFinFET possess higher current density at the surface resulting in early bipolar triggering. Moreover, higher TLP current stress is required to generate carriers. Therefore, the bipolar triggering takes place at higher current in case of STI-DeFinFET.

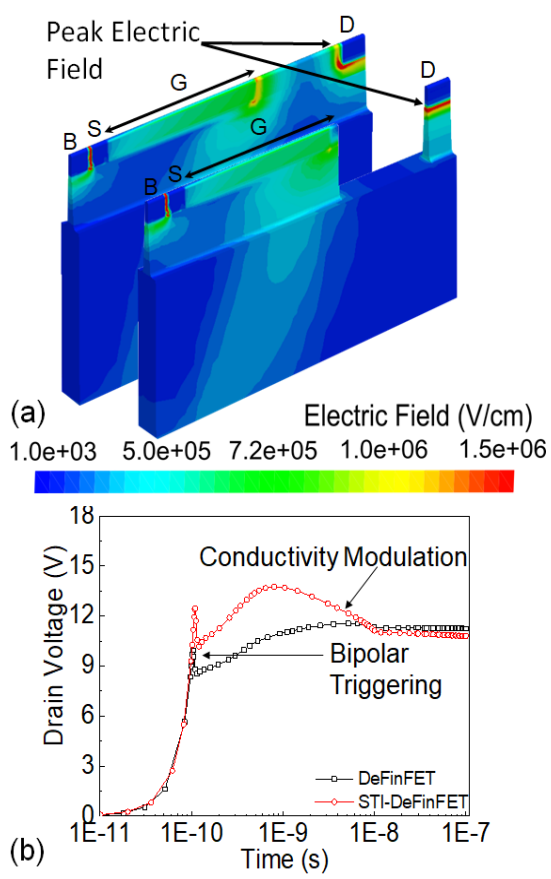

Figure 7: (a) Contour plot showing the Peak electric field after space charge modulation, where the electric field is concentrated at drain contact. STI-DeFinFET exhibits intense drain electric field, due to the narrow opening of the drain region, which further leads to higher impact ionization, (b) Transient drain voltage w.r.t time first snapback in voltage shows the triggering of bipolar whereas second level of decay in voltage in STI-DeFinFET depicts space charge modulation.

3. Conductivity Modulation

After the bipolar is turned on, the drift region gets flooded with excessive carrier as the stress current is increased. At point 'b' in TLP IV of Fig. 3(a), injected current is enough to populate the drift region with excessive electrons. Fig. 6(a) shows the electron density exceeding the background doping, which results in a shift in the electric field towards the drain contact as shown in Fig. 6(b). With this shift in the electric field (which is conductivity modulation [2]), the peak impact ionization now gets localized at the drain contact, which further increase the electron density in the N-well. Fig. 3(a), point 'c' is the current where the space charge

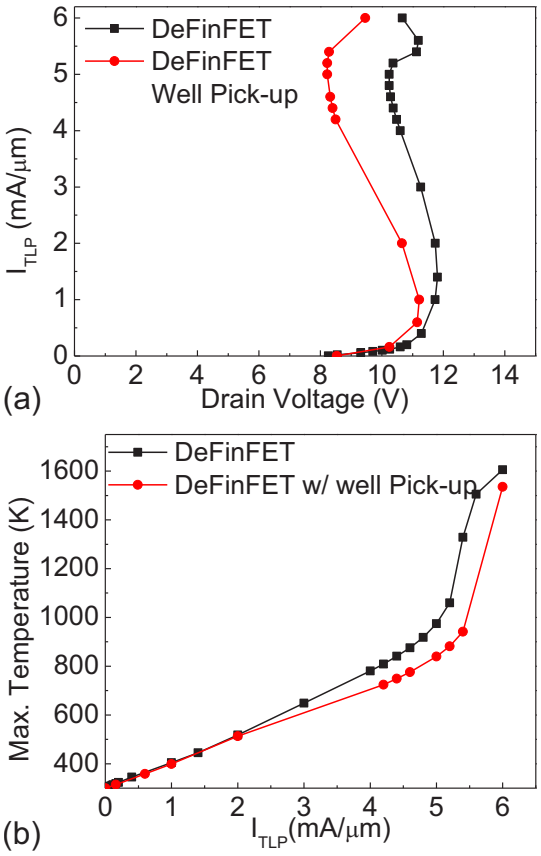

Figure 8: (a) TLP IV characteristics of DeFinFET compared with DeFinFET with ring type equivalent well pick up, here the body contact next to the source is removed and a well pickup is placed at 4 microns deep from channel region to collect the substrate current (b) Temperature vs I_{TLP} comparison w/ and w/o well pick up.

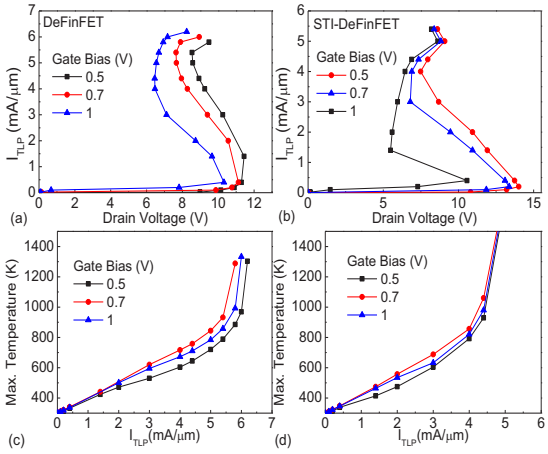

Figure 9: TLP IV characteristics of (a) DeFinFET (b) STI-DeFinFET. Here the TLP current stress is zapped under different gate bias.

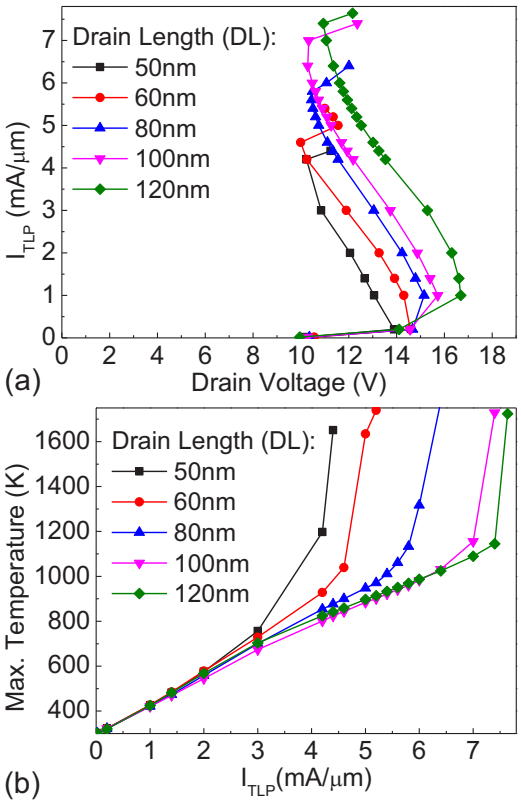

Figure 10: (a) TLP IV characteristics of STI-DeFinFET with various drain opening length (DL), (b) Temperature vs I_{TLP} comparison of STI-DeFinFET for various (DL).

modulation strengthens and is followed by excessive carriers which cause the snapback in TLP IV characteristics. Fig. 7(b) shows the transient response of the injected current corresponding to point 'c' in Fig. 3(a). It is worth highlighting that the depth of the voltage snapback is smaller in DeFinFET as compared to that of STI-DeFinFET. This is because of a narrow opening of drain in STI-DeFinFET (Fig. 7(a)), which leads to higher current density, followed by high impact ionization. This physical event creates excessive carriers in the drift region, therefore a deeper snapback is observed. Fig. 7(b) shows a bipolar action during the transient rise time, whereas the second decay in voltage is observed only in the STI-DeFinFET attributed to intense conductivity modulation due to narrow drain opening (DL). Having reached a current value with strong conductivity modulation and snapback, localized heating gets pronounced at the drain edge creating a hot spot. Fig. 3(a), point 'd' shows the deviation in the IV characteristics and a quick rise in lattice heating is seen through Fig. 3(b), this

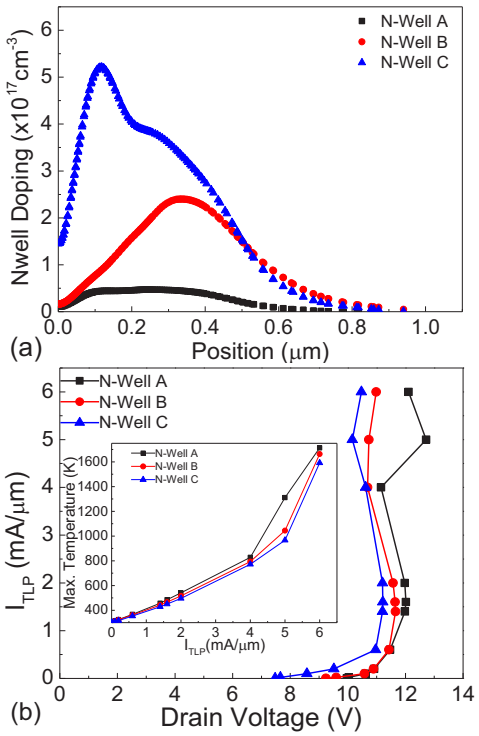

Figure 11: (a) Doping Concentration of N-Well from top of the fin into depth of the well, (b) TLP IV characteristics of various doping profiles of DeFinFET N-Wells.

excessive lattice heating is summarized as a progressive effect of bipolar triggering, space charge modulation and intensified current density. At this stage, with a localized hot spot, lattice

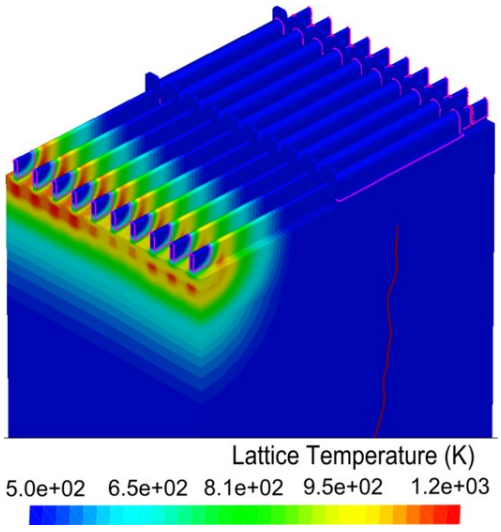

Figure 12: Lattice Temperature profile in a multi-fin (with number of fins = 10) DeFinFET device extracted at I_{TLP}= 4 mA/μm at 100ns, depicting non- uniform current conduction under transient current stress. A fin to fin variation of the n+ drain doping is investigated.

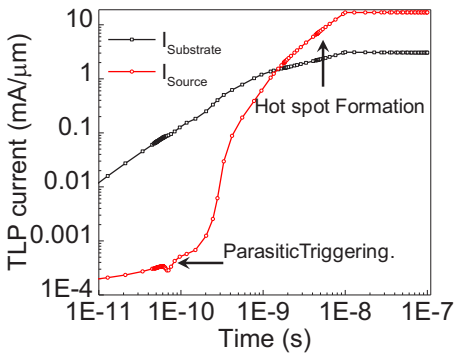

Figure 13: Transient Substrate and source current of multifin DeFinFET. A notch in source current corresponds parasitic bipolar triggering. Space charge modulation after bipolar triggering leads to localized hot spot formation close to the drain contact.

temperature reaches beyond silicon thermal limits and causes permanent melting. The current required for creating a hot spot is considered as the device failure current It2.

4. Substrate Current Pick Up

Substrate/body terminal collects the holes generated from the avalanche multiplication, which indeed raises the well potential and triggers the parasitic bipolar. Fig. 8(a) shows the TLP IV characteristics of DeFinFET w/ and w/o butted body contact. In case of w/o butted body contact, the body/substrate is grounded through the bottom of the device, this setup is a manifestation of ring type p-well/body pick up often used in large array of device fingers. When the butted substrate contact is removed, holes start accumulating under the source terminal and trigger the bipolar more effectively and therefore, causes a deeper snapback than the one with butted substrate contact. Fig. 8(b) shows the reduced lattice heating due to back of drain voltage for a given current.

B. Safe Operating Area and Device Design

Fig. 9 (a) & (b) shows the safe operating area (SOA) of the HV devices. Under increasing gate bias the current required for voltage snapback decreases. This is attributed to relaxed electric field distribution under the gate region in De-FinFETs, therefore, It2 increases with gate bias. However, in STI-DeFinFET hot spot formation is purely dependent on current crowding under the drain contact opening (DL). Therefore, irrespective of gate bias, failure current It2 remains same. Fig. 10 shows the TLP IV characteristics of STI-DeFinFET with increase in Drain contact opening (DL). As it was discussed earlier, current crowding under the drain causes hot spot. One solution to mitigate current crowding is to increase DL, Therefore, with the increase in DL the current density lowers and failure current increases. Fig. 10(a) shows increase in current to snapback and failure current It2.

Fig. 11(a) shows the investigation with different N-well configurations. The dopant distribution of N-Well from the surface to its bottom is plotted. The peak doping concentration of N-well is implanted away from the surface of the semiconductor/fin so as to have current conduction through the bulk of silicon as well as to reduce the surface electric field. Fig 11(b) depicts the TLP IV characteristics of DeFinFET for various N-Well designs. It can be clearly seen that, lower doping of drift region has higher breakdown voltage, however attracts space charge modulation for lower current densities. Therefore, low doping comes with high breakdown voltage at a cost of lower failure threshold. In the other case, where the peak doping is higher beneath the STI, and where the conducting volume of silicon increases (due to the termination of STI), current density is reduced and delay the kirk effect with respect to the injected current. Hence, a well-designed N-Well plays a crucial role in determining the performance of the transistor as well as ruggedness towards electro-static discharge as the failure threshold increases.

Multi-Fin DeFinFET

In the previous sections, physical behavior of a DeFinFET and STI-DeFinFETs under TLP stress corresponding to a unit cell/device was discussed. Fig. 12 shows the multi-fin arranged DeFinFET, where N (N=10) number of identical fins are placed in parallel. Parallel fin arrangement is an equivalent of large width devices to increase the device drive current. Moreover, parallel fins in FinFET technology discretize/digitize the device width. Even in the case of multifin DeFinFET, physical events under TLP stress is similar as that of a single fin DeFinFET. Fig. 13 shows the transient source and substrate current, wherein the bipolar triggering, conductivity modulation and hot spot formation continue to remain the same as discussed

for the single finger DeFinFET. However, multi-finger DeFinFET carry non-uniform current conduction at higher TLP current stress (Fig. 12). This is attributed to conductivity modulation in the N-Well (drift) region close to the drain contact area [6]. Among the fins along the width, variation of drain doping, fin width and contact silicidation determines the non-uniform conduction mechanism in multi-finger DeFinFETs. Due to the non-uniform current conduction, filaments form in the multi-finger DeFinFETs as depicted in Fig. 12.

III. Conclusions

Detailed analysis of ESD behavior of High Voltage DeFinFET and STI-DeFinFET are studied. Various physical attributes of TLP IV characteristics are summarized comprehensively. Bipolar triggering and space charge modulation followed by hotspot formation in HV FinFET causes failure under an ESD stress. Moreover, large array of fingers or multi-fingered DeFinFET also undergo the similar physical mechanism as that of single finger DeFinFET/STI-DeFinFET. However, in a multi-finger arranged DeFinFET/STI-DeFinFET, non-uniform current conduction takes place at high current injection levels, which is attributed to conductivity modulation in the drift region. Moreover, in a multi-finger device, variations in contact doping, fin width, silicidation and metal connection among the fins determine which of the total fins participate in non-uniform current conduction and filament formation eventually leading to ESD failure. Contact resistance among the fins formed by the FinFET processing will be crucial towards the ESD failures in DeFinFET devices.

References

[1] Y.T. Wu, F. Ding, D. Connelly, P. Zheng, M. H. Chiang, J. F. Chen, T. J. K. Liu, "Simulation-Based Study of Hybrid Fin/Planar LDMOS Design for FinFET-Based System-on-Chip Technology," in IEEE Transactions on Electron Devices, vol. 64, no. 10, pp. 4193-4199.

[2] B. S. Kumar, M. Paul, M. Shrivastava, "On the design challenges of drain extended FinFETs for advance SoC integration," 2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Kamakura, 2017, pp 189-192.

[3] M. Shrivastava, J. Schneider, M. S. Baghini, H. Gossner, V. R. Rao, "A new physical insight and 3D device modeling of STI type De-NMOS device failure under ESD conditions," 2009 IEEE International Reliability Physics Symposium, Montreal, QC, 2009, pp. 669-675.

[4] A. Chatterjee, S. Pendharkar, Y. Y. Lin, C. Duvvury, K. Banerjee, "A Microscopic Understanding of Nanometer Scale DENMOS Failure Mechanism under ESD Conditions," 2007 IEEE International Electron Devices Meeting, Washington, DC, 2007, pp. 181-184.

[5] M. Shrivastava, H. Gossner, C. Russ, "A Drain-Extended MOS Device with Spreading Filament Under ESD Stress," in IEEE Electron Device Letters, vol. 33, no. 9, pp. 1294-1296, Sept. 2012.

[6] M. Shrivastava and H. Gossner, "A Review on the ESD Robustness of Drain-Extended MOS Devices," in IEEE Transactions on Device and Materials Reliability, vol. 12, no. 4, pp. 615-625, Dec. 2012.

[7] E. J. Yoffa, "Screening of hot-carrier relaxation in highly photo-excited semiconductors," Physical Review B, vol. 23, no. 4, p. 1909-1981.

[8] S. Natarajan et al., "A 14nm logic technology featuring 2nd generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm^2 SRAM cell size," 2014 IEEE International Electron Devices Meeting, San Francisco, CA, 2014, pp. 3.7.1-3.7.