Trap Assisted Stress Induced ESD Reliability of GaN Schottky Diodes

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Abstract - Electro-thermal behaviour and degradation of recessed GaN Schottky diode are studied under forward and reverse ESD stress. Impact of different surface treatments at Schottky interface, on trap generation and degradation is investigated. Evolution of mechanical stress and defects is probed using on-the-fly Raman spectroscopy. Distinct failure modes are discovered in each case.

I. Introduction

Power devices based on AlGaN/GaN hetero-junction have shown outstanding switching performance in power electronics applications. This is inherited to the high density 2DEG (~10^{13} cm^{-2}) with better mobility (1500-2000 cm^2/V) and high peak electron velocity ($3x10^7$cm/s), present at AlGaN/GaN interface. Also, the wide bandgap (3.4eV), high critical breakdown field (3.3MV/cm) and low dielectric constant (9) of Gallium Nitride (GaN) project it as a promising material for power semiconductor devices. Like transistor, diode is an indispensable part of a typical power electronic convertor. In conventional Si MOSFET, the body diode, offers freewheeling path to current conduction however, such diode is absent in GaN HEMT. GaN Schottky diode is an attractive option to solve this. Therefore, research activities related to the GaN Schottky diode and its robustness have recently gained immense attention. During operation, diodes face various types of electrical overstress conditions which pose reliability issue. Several studies are reported on the long-term reliability of GaN Schottky diode in literature [1] – [2]; however, study of ESD reliability of GaN Schottky is very limited [3]- [4]. In present work, device behaviour of recessed GaN Schottky diode is studied under forward and reverse ESD stress and ESD failure mechanisms are investigated. Evolution of device degradation is studied using on the fly I-V, C-V and Raman.

II. Device Fabrication

Schottky diodes were fabricated on the AlGaN/GaN layer stack grown on 4-inch Si (111) as shown in Fig.1. 100 µm wide devices were processed with different anode to cathode spacing, using UV lithography. First, devices were MESA isolated on-wafer, by etching up to 180 nm GaN using Cl_2/BCl_3 chemistry in Inductively Coupled Plasma-RIE system. Then AlGaN barrier in anode region was completely etched, to form direct contact with 2DEG. Anode recess was achieved by using O_2/BCl_3 based digital etch technique. Recess depth was optimized to give least contact resistance. For cathode, Ti/Al/Ni/Au metal stack, was deposited using E-beam evaporation and later annealed in N_2 ambient to form Ohmic contact with 2DEG. Defect and carrier trapping at Schottky interface limit the diode reliability [1], [4] and a high quality Schottky interface is always desired. Therefore, after RIE etching of anode, diodes were processed with four different types of surface treatment runs namely; (i) A1- 700 °C RTA for 60 sec. followed with HCl and HF dip. (ii) A2- 500 °C RTA for 5 sec. followed with HCl and HF dip, (iii) B1: Buffer oxide (BOE) treatment for 30 sec. and (iv) B3: without any surface treatment. At last, anode, Ni/Au metal stack was deposited followed by annealing at 300 °C, 30

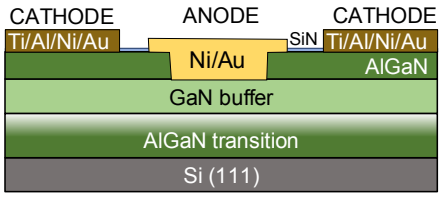

Figure 1: Schematic view of AlGaN/GaN recessed Schottky diode under test. ESD reliability of Schottky contact is studied which is processed with different types of surface treatments.

sec. in forming gas, to form a Schottky contact with the 2DEG.

III. Device Characterization

TLP characterization of diodes was done using pulses of 10 ns pulse width (PW) and 1 ns rise time. Here, small pulse width is preferred than larger PWs, to minimize the thermal effects like defect annealing [4], originating from self-heating, while probing electrical effects like defect generation, carrier trapping and piezoelectric effects. Diodes were tested under forward (ESD at anode) and reverse stress (ESD at cathode). TLP characteristic of device under test (DUT) were obtained by averaging device voltage and current waveforms over 70 -90 percent averaging window of the pulse duration. After each pulse, following diode parameters were spot measured namely; (i) forward linear current at 1 V and (ii) reverse leakage current at -10 V, to monitor degradation. DC I-V characterization of diode was done in between the stress test, to record the change, if any, in diode behaviour. During initial stage of TLP measurement, DC characterization was done after each 20V increment in TLP stress. However, at later course of test, DC characteristics were recorded whenever a change in the spot current was noticed. In our earlier study [4], it was discovered that Schottky/GaN interface degrades with ESD stress and limits the diode reliability. Therefore, in present study, to improve the robustness of the Schottky diode, Schottky/GaN interface is undergone different surface treatments. And the interface quality is determined by measuring the interface defect density (D_{it}) in each case. For this, the depletion capacitance is measured at -2 V reverse bias and 20 kHz frequency at regular intervals during the test and D_{it} is determined at Schottky/GaN interface using the following relation;

$$Dit \approx \frac{2.5}{q}\left(\frac{G_P}{\omega}\right)_{\max}$$

where G_p is the conductance and ω is the frequency.

At high voltage, mechanical stress develops in GaN due to its piezoelectric nature and causes shift in the native GaN Raman peaks; $E_{2\text{-}H}$ (567.5 cm^{-1}) and $A_{0\text{-}L}$ (735 cm^{-1}) [5]. The increased mechanical strain creates crystallographic defects in GaN, [6] and engage in carrier trapping and associated device degradation. Therefore, during the TLP test, 2D profile of mechanical stress in anode-cathode region was also recorded, at regular intervals using on the fly Raman mapping. All measurements were done under dark and at room temperature (300K).

IV. Experiments and Observations

Schottky diodes were stressed in two operating regions; (i) Forward-mode: anode stressed with cathode grounded and (ii) Reverse-mode: cathode stressed with anode grounded.

A. Forward Mode ESD Stress

Figure 2 shows a comparison of TLP characteristics under forward stress for diodes processed with different anode surface treatments. Following observations can be noticed; (i) Although diode-A1 (with 700 RTA) has larger $V_{CUT\text{-}IN}$ as depicted in inset of Fig.2a, it showed higher TLP current than the diode-A2 (with 500 RTA) which is attributed to its lower R_{ON} and smaller Schottky barrier height (SBH = 0.54eV). (ii) Diode-B1 (with BOE), failed earlier than diode-B3 (without BOE). BOE treatment on GaN increases the surface roughness which translates to increase in D_{it} at Schottky interface [7] Spot measured leakage characteristics are shown in Fig. 2(b)-(c). Forward linear current (I_F) showed negligible degradation in all cases except in diode-A1 as depicted in Fig. 2(b). However, beyond a critical stress current, called safe operating stress current, reverse leakage (I_R) increased by several orders of magnitude in all the cases, are shown in Fig. 2(c). This observation highlights that reverse leakage in GaN Schottky diode is sensitive parameter to capture degradation.

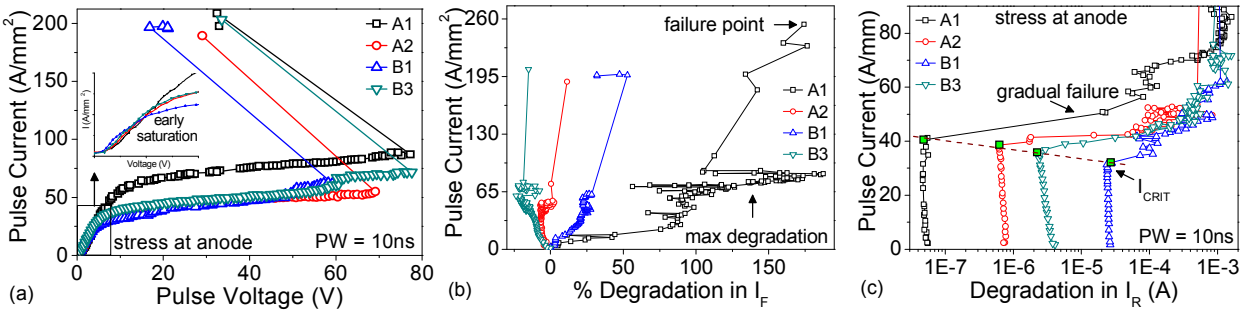

Figure 2: TLP characteristics of recessed diode with different anode surface treatments, when anode is stressed with respect to cathode. (a) A1-diode (with 60s RTA @700 °C) showed improvement in TLP current while B1-diode (with BOE treatment) failed early. (b) Degradation in spot measured forward diode current exhibits maximum degradation in A1-diode. (c) Significant increase in spot measured reverse leakage is noticed and diode suffers soft/gradual failure beyond a critical value of stress current (I_{CRIT}), in each case.

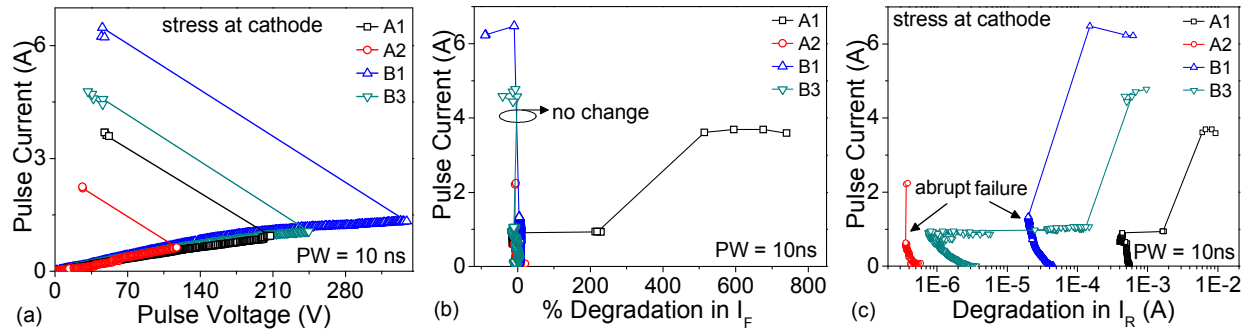

Figure 3: TLP characteristics of recessed diode with different anode surface treatments, when cathode is stressed with respect to anode. Interestingly, linear TLP characteristics are observed under 10 ns pulse width. Figure reveals; diode with BOE treatment (B1) exhibited much higher robustness (V_{SNAP}) than diode without BOE treatment (B3). (b) No significant change is noticed in spot measured forward diode current, except for diode-A1. However, the spot measured reverse leakage followed unique degradation trend as shown in (c) and the diode faced abrupt failure beyond a critical value of stress current in each case.

B. Reverse Mode ESD Stress

Next, the diodes were tested under reverse mode, with cathode positive stressed and anode grounded. Figure 3 shows the TLP characteristics of different types of diodes under test. Figure 3(a) reveals the following; (i) Linear TLP characteristics are observed in all the cases. (ii) Diode-A1 (with 700 RTA) and diode-B1(with BOE) exhibited higher robustness than diode-A2(with 500 RTA) and diode-B1(with BOE) respectively. The corresponding spot measurement results are summarized in Fig. 3(b)-(c). As observed in Fig. 3(b), forward spot linear current remained unchanged like that under forward-mode stress. However, reverse spot leakage degraded significantly. But, unlike in forward-mode, its degradation happened from the very beginning of the stress. And beyond a critical stress current, it increased abruptly on device failure.

V. Analysis & Discussion

A. Trap Assisted Schottky Interface Degradation in Forward Mode

DC characterization of devices is done at regular intervals during the stress, to gain physical insight into mechanism responsible for ESD failure of GaN Schottky diode. Figure 4 summarizes the obtained results. As depicted in Fig. 4(a), Schottky diode degraded gradually with constant increase in reverse leakage under forward-stress and anode contact gradually changes from Schottky to Ohmic. However, under reverse stress, the dc characteristics remained intact until the abrupt device failure occurred. Same behaviour was observed in all the cases. Therefore, it is discovered that GaN diode undergoes soft failure under forward stress and it fails abruptly under reverse mode stress.

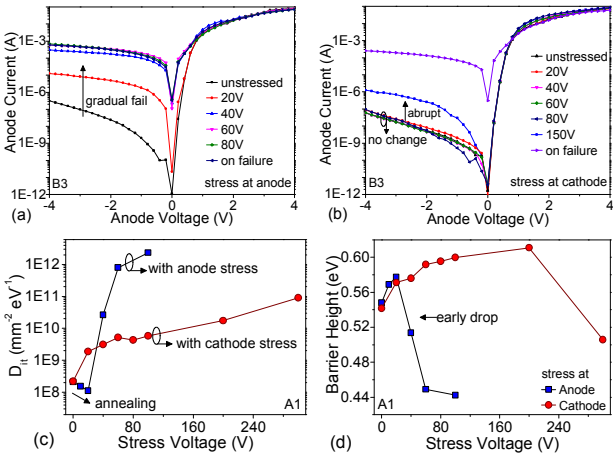

Figure 4: DC I-V characteristics of DUT measured during a 10 ns TLP stress test (a) applied at anode shows gradual change from Schottky to Ohmic nature. While TLP stress (b) applied at cathode induces abrupt device failure with three orders increase in reverse leakage. Interface defect density and barrier height at Schottky junction show significant change with stress, in each case. (c) TLP stress at cathode, causes gradual increase in Dit while such increment is rapid when TLP stress is at anode. As a result, Schottky barrier height degrades early for TLP stress at anode as in (d).

To understand the root cause of these distinct failure modes, Schottky barrier height (SBH) and interface defect density (D_{it}) were monitored during stress under forward and reverse mode. Figure 4(c)-(d) shows the variation in D_{it} and SBH recorded in device under stress. As depicted in Fig. 4(c) diode under forward ESD stress, saw initial drop in D_{it} which is attributed to thermal annealing of the interface defects at high forward current [8]. Beyond a certain stress current value, called safe operating stress current, an increase of 4 orders is recorded in D_{it}. The increased D_{it} gradually deteriorates SBH from 0.58 eV to 0.44 eV which induces gradual increase in dc reverse leakage (Fig. 4a) and spot leakage (Fig. 2c) according to the Schottky diode equation;

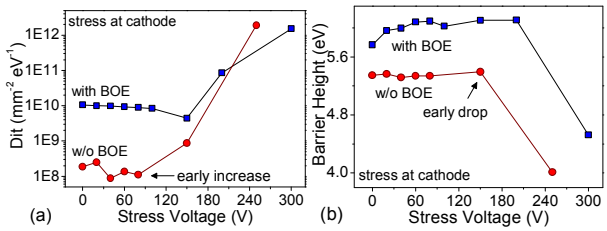

Figure 5: Health of Schottky interface is monitored at regular intervals during the stress. (a) Diode processed with pre-BOE treatment exhibits higher D_{it} that diode without BOE treatment. However, diode without BOE treatment, shows early increment in D_{it} which lowers SBH at much lower stress voltage as in (b).

$$I = I_S\left[e^{\frac{qV}{\eta kT}} - 1\right] \text{ and } I_S = AA^*T^2e^{\frac{q\phi}{kT}}$$

where I_S is the reverse saturation current, η is the ideality factor, Φ the SBH, T the absolute temperature, k the Boltzmann constant, A* the Richardson constant and A is Schottky contact area.

D_{it} in diode under reverse stress, increased linearly from the very beginning of the stress as depicted in Fig. 4(c) but, at much slower rate compared to that under forward stress. However, despite of D_{it} increment, a constant increase is noticed in SBH which is unexpected. Irrespective of type of surface treatment, the trend of D_{it} increment and SBH remained unchanged as shown in Fig. 5. Therefore, D_{it} increment is not the root cause of diode failure under reverse stress and possibly there exists a different failure physics.

B. Piezoelectric Stress Induced Failure in Reverse Mode

GaN/AlGaN material system possess intrinsic piezoelectric nature which poses reliability challenges at high voltages. In present study, the evolution of mechanical stress in DUT captured on the fly during ESD stress using 2D Raman mapping revealed interesting failure physics under reverse mode ESD stress. Figure 6 shows, the evolution of

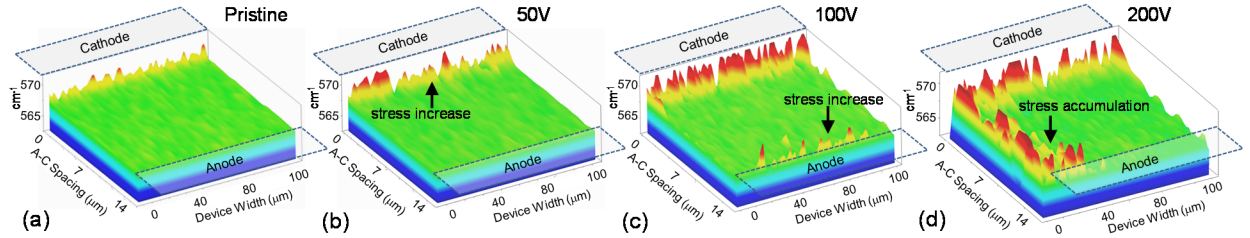

Figure 6: (a) Raman map captured in anode-cathode region of pristine diode, before stress. Figure reveals residual compressive stress at cathode edge. On the fly Raman map was captured during reverse-mode ESD stress (b) at 50V, (c) at 100V and (d) at 200V stress on cathode. With increasing ESD voltage, compressive stress accumulates at edge and corner(s) of recessed anode.

mechanical stress in anode-cathode region with increasing TLP stress at cathode. Raman map of pristine device as shown in Fig. 6a before stress, reveals residual compressive stress present at cathode which possibly originates from CTE mismatch between cathode metal stack (Ti/Al/Ni/Au) and underlying AlGaN, after post metal deposition anneal. 2D Raman maps shown in Fig. 6(b)-(d), reveal that with increase in ESD voltage, the compressive stress builds up at the recessed anode edges and corners. This explains why failure occurred at recess edges in diodes under reverse ESD stress as shown in Fig. 7(a)-(b). Therefore, ESD failure of GaN Schottky diode under reverse mode, is governed by the piezoelectric stress distribution, hence exhibits field dependent failure.

VI. Failure Analysis

After TLP testing, failure analysis of ESD damaged regions of diodes was done to gain physical insight into the degradation mechanism(s). Figure 7 shows post failure SEM micrographs of device failed under different stress conditions. Figure 7(a) SEM image of diode-A2 damaged under TLP stress applied at cathode. The damage occurred at anode recess edge with no traces of metal melting/ migration observed. Figure 7(b) shows image of diode-B3 with similar damage at anode edge. This observation highlights the universal nature of failure mechanism and is independent of Schottky interface quality/treatment under reverse mode ESD stress. The absence of metal melting/folding and migration in failed regions reveals the non-thermal nature of the failure and points to field dependent failure. Figure 7(c) SEM image of a diode which failed under forward ESD stress. Massive crack can be seen at anode contact corner with metal migration. EDX analysis confirms Au (14%) migrated from anode to cathode edge. This observation reveals thermal nature of the failure. Post failure SEM image of diode-A1 which failed under forward stress shows multiple cracks at anode corner due to fringing field. Also, anode metal melting and peel-off further confirms electrothermal device failure. Pits and dislocations

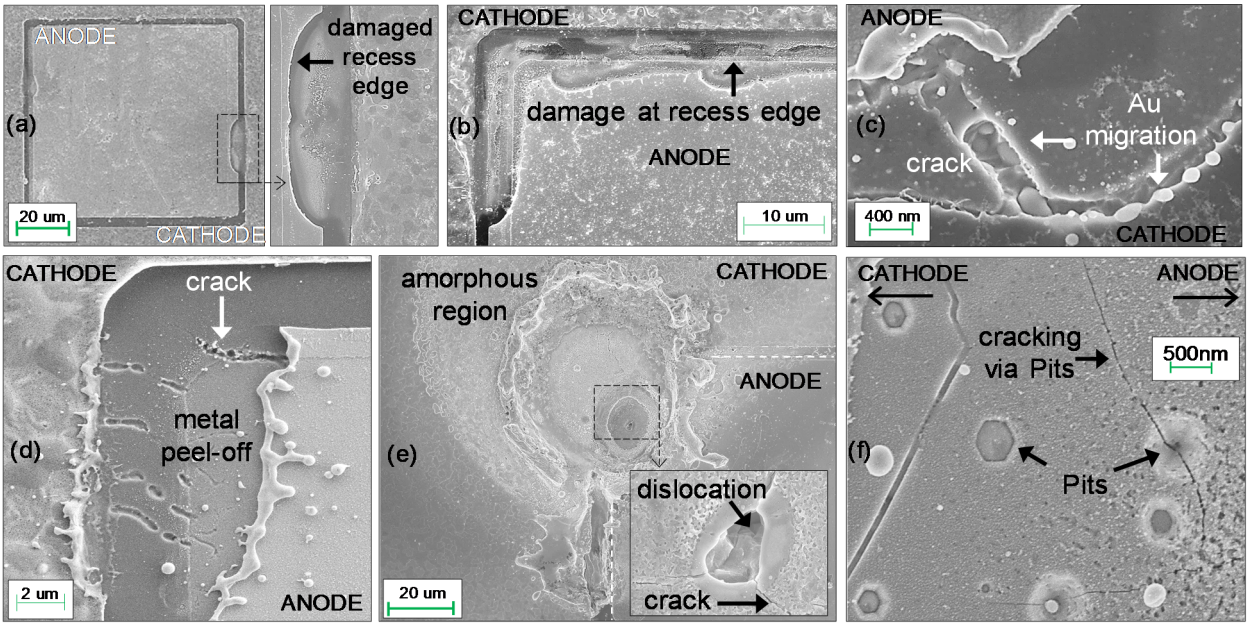

Figure 7: (a) SEM image of diode damaged under 10 ns TLP stress applied at cathode. Damage at anode recess edge is visible. No traces of metal melting/ migration observed which highlights non-thermal nature of the failure. (b) Diode failure at anode recess edge under reverse mode stress. (c) SEM image of diode failed when stressed at anode. Massive crack is seen at anode contact corner with metal migration. EDX analysis confirms Au migrated from anode to cathode edge. This observation reveals thermal nature of the failure on on-state failure. (d) Post failure image of diode which failed under forward mode ESD stress. Multiple cracks at anode corner possibly occurred due to high fringing field. Also, anode metal melting and peel-off confirms electrothermal failure. (e) Post failure SEM image of diode-A2, with damaged region between anode and cathode. Magnified view shown in Inset, reveals dislocation induced cracking and consequent diode failure. (f) Image of another failed A2-diode, shows a network of pits/dislocations which provided path form crack propagation.

can also nucleate the cracks in anode-cathode region, as seen in Fig. 7(e)-(f).

VII. Conclusion

Different failure mechanisms were discovered in recessed GaN Schottky diode under forward and reverse mode ESD stress. Failure in forward mode was found to be assisted by generation of traps at the GaN/Schottky interface where gradual device degradation occurred with increment in interface defect density. Failure under reverse mode, was observed to be governed by piezoelectric stress distribution in anode-cathode region where, stress accumulation at recessed anode edge/corners induced device failure. Under forward stress, failure was found to be gradual, whereas it was abrupt under reverse mode ESD stress. Spot measured reverse dc leakage current was discovered to be an efficient parameter to monitor degradation. Failure analysis results corroborate well with the finding.

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