Part I: Physical Insights Into Dynamic R_{ON} Behavior and a Unique Time-Dependent Critical Stress Voltage in AlGaN/GaN HEMTs

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***Abstract*— We report a unique OFF-state drain-to-source critical stress voltage above which the dynamic performance of AlGaN/GaN HEMTs is significantly deteriorated. Physical insights are developed through detailed experiments conducted for different design variants, increased substrate bias, varying temperature, varying stress time, and experimenting buffers with lower C-doping. The surface leakage measurements on dedicated test structures and experimentation of devices realized over GaN buffer with different carbon doping reveal that the observed phenomenon is solely caused by traps present in carbon-doped GaN buffer. Surface traps have no role to play as far as they do not modulate the electric field in the GaN buffer (discussed in Part-II). Stress time, substrate temperature, substrate bias, electric-field shape, and depletion regions formed under the gate as well as field plate region were found to play a key role in governing trap-assisted transport and carrier trapping in the GaN buffer. A deeper physical insight to explain the observed phenomena and its dependency on various conditions are developed through detailed measurements, TCAD simulations, electroluminescence, and photoluminescence spectroscopy. With the help of the physical insight gained into the underlying mechanism, a novel surface passivation scheme using a p-type oxide is reported in Part-II, which helps relaxing the field distribution across the access region and buffer, and in turn improves the dynamic performance of the HEMTs. Besides, the Part-II also unifies the mechanism across different gate-stack designs and reveals the interplay between the surface and buffer, which governs the dynamic performance of these devices.**

***Index Terms*— AlGaN/GaN HEMTs, buffer traps, critical voltage, device design, dynamic ON-resistance.**

I. Introduction

DESPITE several unique features offered by AlGaN/GaN HEMTs, like wide bandgap and excellent channel transport properties, dynamic ON-resistance (R_{ON}) is one of the major performance bottlenecks that prevents its wide-scale acceptance in power-switching applications [1]–[16]. Dynamic R_{ON} is the increase in R_{ON} immediately after an OFF-state stress, which can be observed while switching from OFF- to ON-state. It is argued to be caused by traps present in the AlGaN/GaN HEMT system. Few groups suggested it to be due to trapping of electrons in the GaN buffer [1]–[6], whereas some other works argued it to be due to the traps present at the HEMT surface [7]–[10]. Possibility of dynamic R_{ON} due to traps present at the HEMT surface or surface defects was mostly argued by addressing dynamic R_{ON} issue by surface passivation using SiN_x [7], AlN [8], [9], GaN cap [10], and NH_3 plasma surface treatment [12]. On the other hand, with increased focus on buffer design to reduce leakage and improve breakdown voltage of the device, traps introduced in the GaN buffer by intentional doping [1], [2], [17]–[19] are becoming increasingly relevant. Moreover, recent studies suggest an interplay of surface and buffer properties in determining dynamic performance of the device [13], [14]. Besides, the physics behind this interplay has not been probed yet. Attributed to these, the phenomena responsible for dynamic R_{ON} in GaN HEMTs is still not completely understood, which has led to an increased requirement to understand buffer trap dynamics and its impact on dynamic performance of the HEMTs. Recent reports suggest hole emission from the carbon-doping-induced buffer traps and subsequent redistribution to be responsible for dynamic R_{ON} [15]–[17]. However, the model is limited to dynamic R_{ON} under lower stress voltages which result in negligible carrier injection into the C-doped GaN buffer of the devices.

In this work, we report a unique physical phenomenon governing dynamic performance of the device. Detailed dynamic stress experimentation on AlGaN/GaN HEMTs revealed a unique stress time and device geometry-dependent critical OFF-state drain stress voltage. Devices showed a drastic increase in dynamic R_{ON} as the drain stress voltage was increased beyond the observed critical voltage. Karboyan *et al.* [20] earlier reported preliminary investigations demonstrating similar dynamic R_{ON} trends with OFF-state stress times in AlGaN/GaN HEMTs having a C-doped GaN buffer. While a first report on the observance of critical voltage was presented in our recent work [6], a detailed physical insight into the process involved is largely missing. Further, based on findings from various experiments per-

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formed and TCAD-based analysis, a detailed physical insight to explain the underlying mechanism is also presented in this work. The proposed physical phenomena successfully encapsulated different factors governing the critical voltage, including gate–drain distance (L_{GD}), field plate length (L_{FP}), passivation thickness (t_{passi}), stress time, buffer doping, surface properties/passivation, substrate bias, and temperature. With the help of the physical insight gained into the underlying mechanism, a novel surface passivation scheme using a p-type oxide is reported in part II of this work, which helps relaxing the field distribution across the access region and buffer and in turn improves the dynamic performance of the HEMTs. Besides, the part-II also explains the interplay between the surface and buffer, which governs dynamic R_{ON} behavior.

This work is arranged as follows: device fabrication and measurement procedure carried out to study dynamic R_{ON} in AlGaN/GaN HEMTs is explained in Section II. In Section III, the dependence of dynamic R_{ON} on drain stress voltage is evaluated and presence of a critical drain stress voltage beyond which dynamic R_{ON} increases drastically is reported. The dependence of the critical voltage on GaN HEMT design parameters: 1) lateral parameter viz. L_{GD}, L_{FP}, and 2) t_{passi} is also discussed. The physical origin of the critical voltage and its dependence on the HEMT design parameters are explained in Section IV. Additionally, the transport mechanism of electrons to the traps and its dependence on electric field are investigated using electro-luminescence, photoluminescence and computational analysis. Finally, the proposed mechanism is validated in Section V by performing dynamic R_{ON} measurements for different temperature, substrate bias, and buffer doping. This work is concluded in Section VI.

II. Device Fabrication and Experimentation

Schottky-gated AlGaN/GaN HEMTs were fabricated on a 6″ (commercial grade) carbon-doped GaN on Si epi-stack, as shown in Fig. 1(a). The epi-stack consists of a 18-nm $Al_{0.25}Ga_{0.75}N$ barrier layer grown over a GaN channel with a 5-μm buffer layer and 1.5-μm stress-relieving layers. The HEMTs have a 2-DEG concentration of $\sim 8.5 \times 10^{12}$ cm^{-2} and sheet resistance of $\sim$400 Ω/□. A well-optimized process flow and recipe was used, which is explained in detail in our earlier work [21]. Here, Ti/Al/Ni/Au-based ohmic contact to the 2-DEG was formed by annealing the metal stack at 820 °C for 30 s in N_2 ambient. Subsequently, Cl_2-based dry etching was used for MESA isolation. HEMTs with varied device parameters: L_{GD}, L_{FP} and t_{passi}, were fabricated for this work. The *in situ* SiN_x passivation thickness in the source and drain access regions was varied by its selective etching using O_2-CHF_3 plasma. The *in situ* SiN_x was also completely removed from the channel region followed by Ni/Au e-beam evaporation and a long anneal to form the gate finger. The gate finger was extended over SiN_x passivation toward the drain pad to form the field plate (FP) structures. It is worth highlighting here that all the wafers were processed simultaneously (in a single process lot) using the optimized processes

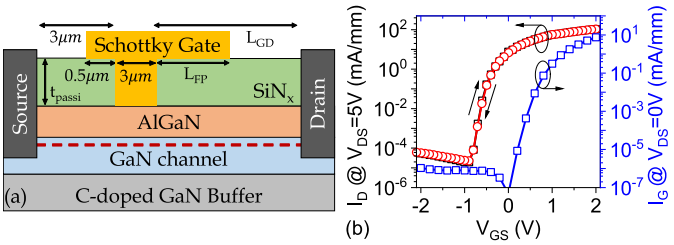

Fig. 1. (a) Schematic of the Schottky-gated AlGaN/GaN HEMTs under test. (b) Absence of hysteresis in the dual sweep transfer ($I_D - V_{GS}$) and gate leakage ($I_G - V_{GS}$) characteristics depicts superior gate-stack quality of the HEMTs under test. Device dimensions: gate–drain distance (L_{GD}) = 15 μm, field plate length (L_{FP}) = 4 μm, passivation thickness (t_{passi}) = 20 nm.

to ensure minimal process-related variability across wafers. Fig. 1(b) shows transfer ($I_D - V_{GS}$) and gate leakage ($I_G - V_{GS}$) characteristics of the fabricated HEMTs, which depict low gate & OFF-state leakage, high I_{ON}/I_{OFF} and threshold voltage (V_{TH}) ≈ -0.8 V. V_{TH} typically higher than earlier reports is attributed to surface modification under the gate, which is achieved by extensive surface cleaning before gate metal deposition and an optimized gate metal anneal (at 300 °C for 10 mins in forming gas). The superiority of the gate-stack used here is however confirmed by the lower OFF-state leakage and negligible hysteresis seen in the $I_D - V_{GS}$ characteristics depicted in Fig. 1(b).

Dynamic R_{ON} (ΔR_{ON}) study on the HEMTs was carried out by pulse stressing of the device as reported in [14]. The HEMTs were typically stressed in OFF-state ($V_{GS\text{-}Stress} = -3$ V$\sim V_{TH} - 2$ V) with substrate grounded, using 26XX Keithley SMUs. For probing the time dependence of ΔR_{ON}, devices were stressed for different stress times (t_{Stress}). The output characteristics of the devices were measured at $V_{GS} - V_{TH} = 2$ V, immediately before and after the OFF-state stress, to extract the pre-stress and post-stress R_{ON}, respectively. R_{ON} was extracted from the inverse slope of the $I_D - V_{DS}$ characteristics with V_{DS} ranging from 0.25 to 0.5 V. ΔR_{ON} for the HEMTs was then calculated as follows:

$$\Delta R_{ON}\ (\text{in}\%) = \frac{R_{Post\text{-}Stress} - R_{Pristine}}{R_{Pristine}} \times 100. \quad (1)$$

Here $R_{Pristine}$ is R_{ON} of the HEMT before stress, whereas R_{ON} post the OFF-state stress is referred to as $R_{Post\text{-}Stress}$. A typical $I_D - V_{DS}$ characteristic, of HEMTs under test, extracted at various stages of the stress-measure-recovery test routine is shown in Fig. 2(a). It depicts a significant increase in R_{ON} as t_{Stress} was increased (for $V_{DS\text{-}Stress} = 150$ V). It is worth highlighting that $R_{Post\text{-}Stress}$ was found to be independent of V_{GS} or gate overdrive used to measure R_{ON}. Post-stress R_{ON} is therefore extracted for a lower gate overdrive (2 V) to avoid impact on post-stress recovery time or gate leakage, which may drift the dynamic R_{ON} values. The OFF-state stress also did not result in any V_{TH} shift in the HEMTs, as seen in Fig. 2(b), which confirms negligible carrier trapping under the gate. The HEMTs were allowed a 180 s wait under unbiased condition, between subsequent OFF-state stress cycles, to allow the devices to completely recover from the degradation before

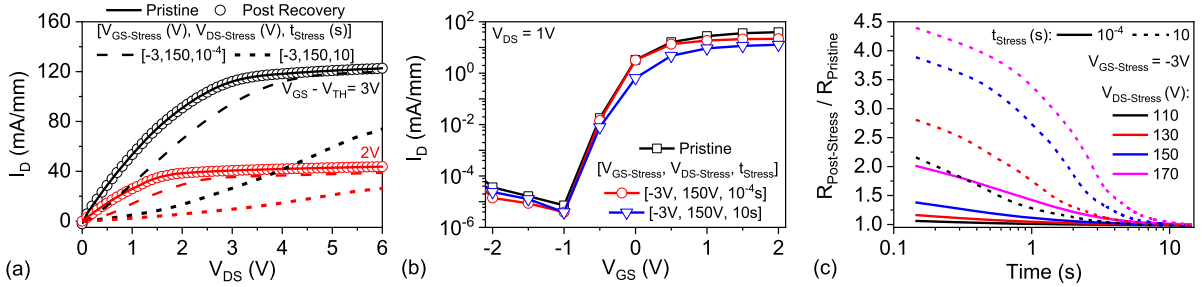

Fig. 2. (a) Typical $I_D - V_{DS}$ characteristic of the Schottky-gated HEMTs, as a function of V_{GS}, extracted after different stress or pristine/recovery conditions. [$V_{GS\text{-}Stress}$, $V_{DS\text{-}Stress}$, t_{Stress}] define stress condition immediately after which the $I_D - V_{DS}$ characteristic was extracted. (b) Typical $I_D - V_{GS}$ characteristic of the HEMTs measured immediately after OFF-state stress depicts reduced ON current (high dynamic R_{ON}) but negligible threshold voltage (V_{TH}) shift. (c) Recovery transient of R_{ON} of the HEMTs, extracted from the I_D transient measured after the OFF-state stress, as a function of $V_{DS\text{-}Stress}$ and t_{Stress}. I_D was measured at $V_{GS} - V_{TH} = 2$ V and $V_{DS} = 0.4$ V. Here, device dimensions are: $L_{GD} = 15$ μm, $L_{FP} = 4$ μm and $t_{passi} = 20$ nm.

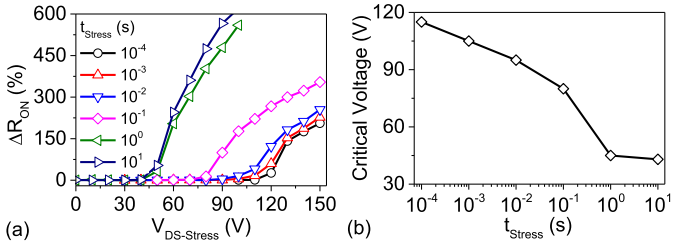

Fig. 3. (a) Dynamic R_{ON} of the HEMTs as a function of drain stress voltage for different OFF-state stress time. It shows a stress time-dependent critical voltage (V_{cr}) beyond which ΔR_{ON} increases significantly. (b) Reduction in V_{cr} with increase in stress time. V_{cr} is however seen to saturate for t_{Stress} beyond 1 s. The device parameters are $L_{GD} = 15$ μm and $L_{FP} = 4$ μm.

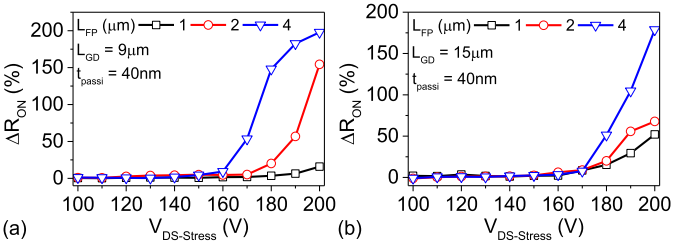

Fig. 4. Dynamic R_{ON} characteristics as a function of field plate length (L_{FP}) for a gate–drain distance (L_{GD}) of (a) 9 μm and (b) 15 μm. A dependence of V_{cr} on lateral device design parameters can be observed. These HEMTs had a 40 nm SiN_x passivation and were stressed for 100 μs.

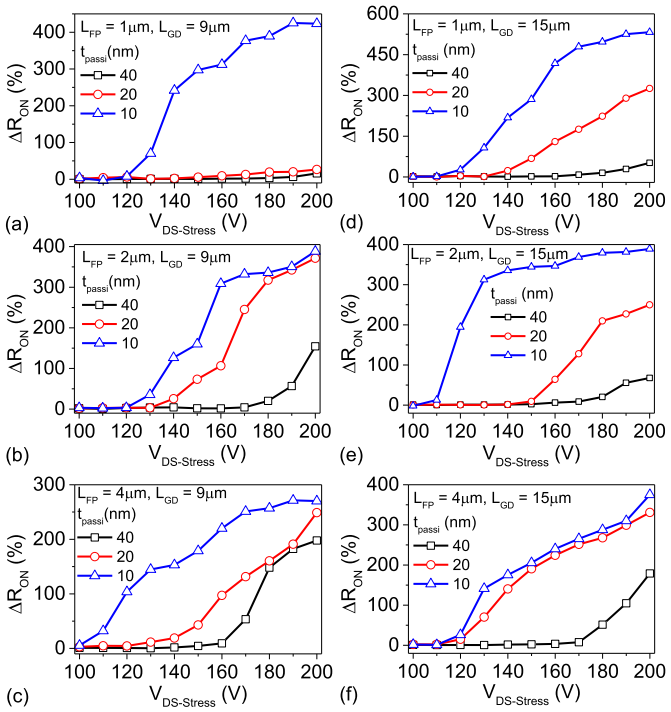

Fig. 5. ΔR_{ON} extracted for devices as a function of passivation thickness (t_{passi}) for L_{GD} (μm), L_{FP} (μm) values of (a) 9, 1, (b) 9, 2, (c) 9, 4, (d) 15, 1, (e) 15, 2, and (f) 15, 4. The dynamic R_{ON} and V_{cr} show a distinct dependence on t_{passi}, irrespective of L_{GD} and L_{FP}. The HEMTs were stressed for 100 μs.

the next stress pulse arrives. A complete recovery of the device during this wait period was observed irrespective of the drain stress voltage, as depicted in Fig. 2(a), which shows overlapping $I_D - V_{DS}$ characteristics of the virgin device and the same measured after a wait period of 180 s post-stress. This is also seen from Fig. 2(c), which shows that $R_{Post\text{-}Stress}$ completely recovers to $R_{Pristine}$ with the recovery time ranging in the order of a few 10's of seconds.

III. Experimental Observations

A. Critical Drain Stress Voltage and Stress Time Dependence

Fig. 3(a) shows ΔR_{ON} extracted as a function of drain stress voltage ($V_{DS\text{-}Stress}$) for different stress times. The characteristics show a negligible ΔR_{ON} for lower values of $V_{DS\text{-}Stress}$, which however has a steep increase in ΔR_{ON} as $V_{DS\text{-}Stress}$ is increased beyond a critical value (V_{cr}). Fig. 3(b) quantifies stress time dependence of V_{cr}, which depicts that V_{cr} drops significantly ($\sim$2.5$\times$) when stress time was increased (by 4 orders), showing a power law like dependence. The V_{cr} was however seen to saturate at $\sim$45 V, even though the t_{Stress} was increased from 1 s to 10 s.

B. Device Design Parameters vs. V_{cr}

To study the impact of electric field distribution, dynamic R_{ON} behavior was studied as a function of lateral device design parameters. Fig. 4 shows ΔR_{ON} extracted as a function of $V_{DS\text{-}Stress}$ for devices with different L_{FP} and L_{GD}. For HEMTs

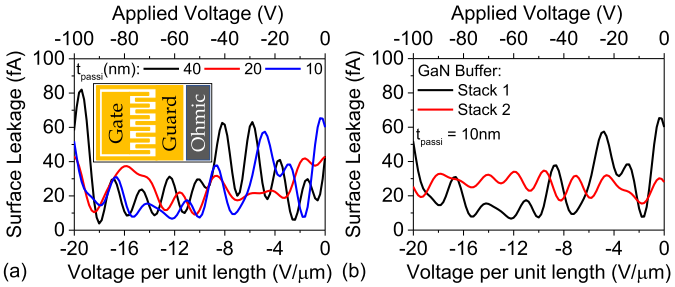

Fig. 6. Surface leakage measured using a specifically designed test structure (shown in inset), as reported by Tan *et al.* [22]. It shows negligible dependence on (a) passivation thickness (t_{passi}) and (b) C-doping in GaN buffer. The distance between the gate and guard structure is 5 μm.

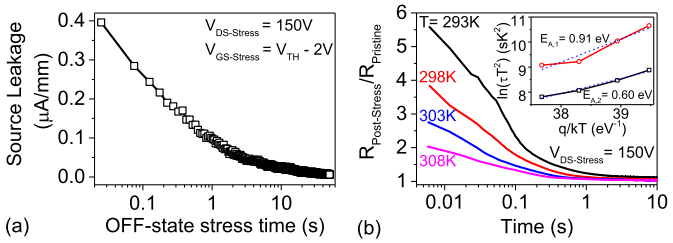

Fig. 7. (a) OFF-state source current (leakage) measured with respect to stress time. A reduction in source leakage current with stress time indicates carrier trapping in the GaN buffer. (b) Recovery transient of R_{ON} of the HEMTs measured after 100 μs OFF-state stress, as a function of temperature (T). (Inset) Arrhenius plot extracted from the R_{ON} transients showing the activation energies (E_A) of traps governing the R_{ON} recovery process. Device parameters are L_{GD} = 9 μm, L_{FP} = 1 μm & t_{passi} = 10 nm.

with shorter L_{GD}, dependence of V_{cr} on L_{FP} was found to be higher when compared to HEMTs with larger L_{GD}. For larger L_{GD}, while the V_{cr} was not reduced significantly when L_{FP} was increased, ΔR_{ON} for a given $V_{DS\text{-}Stress}$ was found to be considerably higher for higher L_{FP} designs. Furthermore, to study the impact of field magnitude acting on the channel, dynamic R_{ON} behavior of devices with different t_{passi} was studied. It should be noted that t_{passi} determines the strength of electric field modulation by gate-connected field plate [23]. Fig. 5(a)–(f) show that t_{passi} or field magnitude in the field plate region significantly affects ΔR_{ON} and V_{cr} irrespective of L_{GD} and L_{FP} values. In all cases, V_{cr} was found to reduce as t_{passi} was reduced i.e. when field magnitude in the field plate region was increased. Impact of t_{passi} on electric field is validated later in detail using TCAD simulation. These observations indicate a significant influence of channel electric field profile on ΔR_{ON} and V_{cr}.

IV. What Governs Dynamic R_{ON} and Critical Voltage?

Previous section indicated that the V_{cr} possibly depends on channel electric field profile as well as stress time. The physical mechanism responsible for the observed V_{cr} and ΔR_{ON} of the device is discussed in this section. Before we probe deeper into the impact of electric field and stress time, it is worth quantifying the impact of surface conditions or surface traps, which has been argued to be a possible root cause for ΔR_{ON} in some of the earlier works [7]–[10]. Fig. 6(a) and (b) show surface leakage measurements using specially designed test structure [shown in inset of Fig. 6(a)], as reported by Tan *et al.* [22], for different t_{passi} and different GaN buffers, respectively. In previous section, we have seen that the ΔR_{ON} and V_{cr} have strong dependence on t_{passi}. In the later section, we will see that ΔR_{ON} and V_{cr} is missing in buffers with low carbon doping. In both the cases, depicted in Fig. 6, surface leakage had negligible dependence on (a) passivation thickness and (b) doping in GaN buffer, even though the applied lateral electrical field was much higher than the critical field required to observe V_{cr}. This shows that the observed V_{cr} was not dependent on surface conditions. Besides, negligible V_{TH} shift immediately after stress, as seen in Fig. 2(b), rules out trapping underneath the gate as the source of ΔR_{ON} degradation in the HEMTs.

While above observations show that V_{cr} is independent of surface and barrier condition, gradual drop in OFF-state source (leakage) current with increasing stress time, which saturates at longer stress times, as depicted in Fig. 7(a), are signatures of dominant trap-assisted transport (TAT) and presence of Poole Frenkel (PF) emission, respectively, in the GaN buffer [24]. A temperature-dependent R_{ON} recovery analysis, using the multi-exponential transient analysis technique [19], also revealed two distinct trap activation energies ($E_{A,1}$ = 0.91 eV and $E_{A,2}$ = 0.6 eV) involved in the process, as seen in Fig. 7(b). These states are attributed to two distinct C-doping induced defect states (E_V +0.9 eV and E_C −0.6 eV) present in the C-doped GaN buffer [17]–[19]. Fig. 7 therefore signifies the presence of carrier trapping in the GaN buffer. Moreover, as the available trap centers for trap-assisted conduction reduces with subsequent trapping in the GaN buffer, the buffer current falls as a function of stress time [25], as seen in Fig. 7(a). At longer stress times PF emission balances the carrier trapping, which leads to saturation of source current as a function of stress time. PF emission however becomes comparable to carrier trapping at much longer stress times (>1 s) than the typical stress times used (100 μs–1 s), which signifies carrier trapping to dominate under these stress conditions. This observed carrier trapping up to 1 s will lead to an accumulated trap ionization in the GaN buffer as devices are stressed for longer time duration. As a result, even for smaller values of $V_{DS\text{-}Stress}$, for which no dynamic R_{ON} is observed for a stress time of 100 μs, a significant dynamic R_{ON} can be observed for higher stress duration, as seen in Fig. 3. Moreover, the subsequent balancing of trapping and PF emission results in saturation of V_{cr} beyond 1 s of stress as observed from Fig. 3. These observations suggest interaction of channel electrons with traps in GaN buffer to be responsible for the observed ΔR_{ON}. As t_{passi}, L_{GD} and L_{FP} also affect V_{cr} and ΔR_{ON} (Fig. 4), we now need to understand the role of channel electric field in governing the interaction of channel electrons with GaN buffer traps.

Fig. 8 shows electric field profile, extracted using well-calibrated device TCAD simulations [4], [26], as a function of $V_{DS\text{-}Stress}$ for t_{passi} of (a) 40 nm, (b) 20 nm, and (c) 10 nm. The following observations are evident: 1) electric field peaks at the gate edge and field plate edge; 2) electric

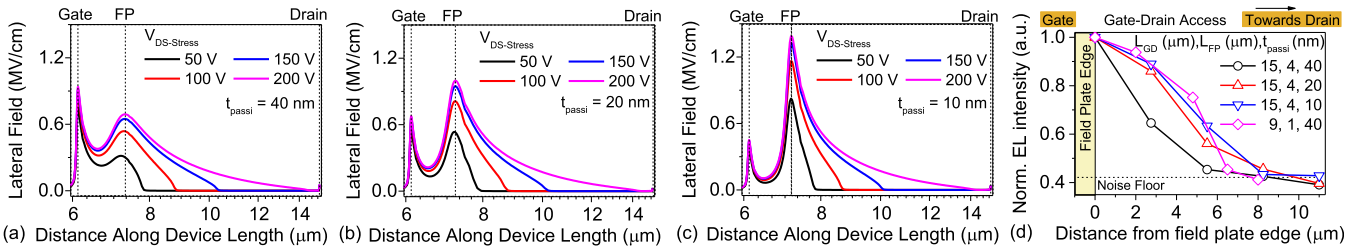

Fig. 8. Lateral electric field profile, extracted using device TCAD, as a function of $V_{DS\text{-}Stress}$ for t_{passi} of (a) 40 nm, (b) 20 nm, and (c) 10 nm. Device parameters are $L_{GD} = 9$ μm, $L_{FP} = 1$ μm. (d) Normalized electro-luminescence (EL) intensity experimentally extracted along the access region for different gate–drain distance (L_{GD}), field plate length (L_{FP}) and passivation thickness (t_{passi}) confirming peak electric field to be confined near field plate edge. The EL spectra were obtained at 170 V.

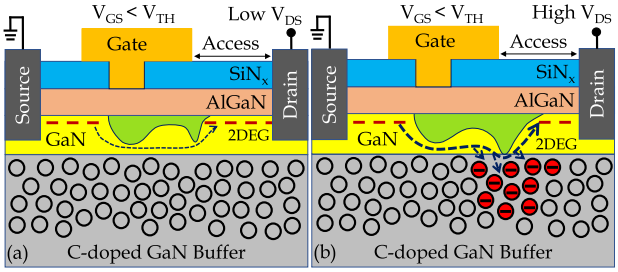

Fig. 9. Device schematic depicting the electron trapping phenomena leading to observed ΔR_{ON} characteristics. (a) Condition in which applied $V_{DS\text{-}Stress}$ is small enough to prevent carrier injection into the GaN buffer. This, supported by a lower ionization probability of buffer traps due to lower field across the GaN buffer, leads to negligible carrier trapping. (b) Condition in which applied $V_{DS\text{-}Stress}$ is high enough to cause sufficient carrier injection, which combined with increased buffer trap ionization probability results in significant carrier trapping and hence ΔR_{ON}. The estimated electron path is represented by a dashed line with linewidth representing the magnitude of leakage current.

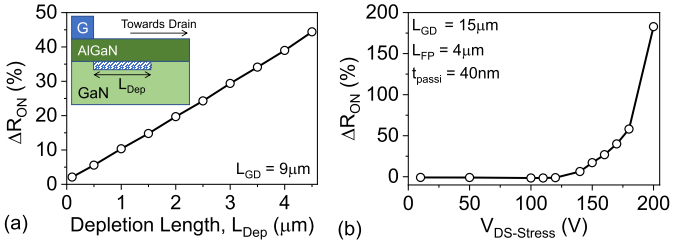

Fig. 10. (a) Impact of selectively depleting the 2-DEG, by emulating a localized charge sheet below 2-DEG, on the ΔR_{ON} performance of the HEMT. For the simulation exercise, the depleted region had 3 orders of magnitude lower carrier density as compared to the 2-DEG channel carrier density. (b) Results of TCAD simulations of the device with conditions similar to experimental setup and considering dynamic trapping of electrons in acceptor-type GaN buffer traps.

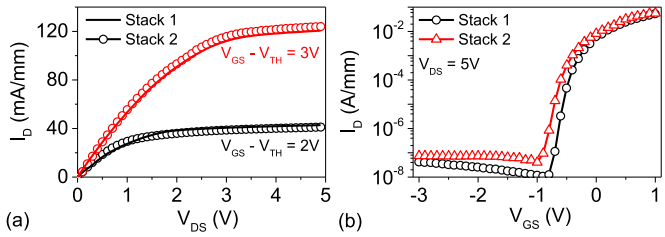

Fig. 11. Typical (a) $I_D - V_{DS}$, and (b) $I_D - V_{GS}$ characteristics of the Schottky-gated HEMTs fabricated on stacks with different C-doping (Stack 1 and Stack 2). It shows similar output and transfer characteristics for devices on both the stacks.

field at the field plate edge increases with increasing drain voltage; 3) moreover, the depletion region toward the drain contact widens with increasing drain voltage; and 4) peak electric field increases (decreases) at the field plate (gate) edge when passivation thickness was reduced. Presence of peak electric field at the field plate edge is confirmed using electro-luminescence (EL) measurement along the access region, as shown in Fig. 8(d), while using different device dimensions. Invariably for all the cases, the electric field was found to be maximum at the field plate edge. Earlier we noticed (Fig. 5) that V_{cr} reduces when t_{passi} was lowered. Fig. 8 shows that when t_{passi} was lowered, electric field strength near field plate edge increases. This signifies that V_{cr} lowers when electric field strength increases near the field plate edge. In other words, V_{cr} is attributed to a critical electric field, which is required to trigger ionization of trap centers in the GaN buffer and push carriers into the deep GaN buffer to cause carrier trapping. Here, the depletion region around the field plate edge would define the affected region. In general, no mobile charge must flow through the depletion region. However, these electrons may traverse through the path below the depletion region, through GaN buffer, potentially getting trapped in the trap centers of the GaN buffer. The GaN buffer being carbon doped is known to have several trap levels in the energy band [17]–[19], as also seen in Fig. 7(b). Carrier trapping in buffer would then depend on following three parameters: 1) time provided for the trapping process determined by stress time; 2) injection of carriers into the GaN buffer determined by source-drain leakage and field conditions; and 3) ionization probability of trap centers determined by trap energy level and electric field in the GaN buffer (electric field strength will define the bending of energy bands and position of Fermi energy level in reference to valence/conduction bands).

Fig. 9(a) and (b) summarize these observations. It shows that when $V_{DS\text{-}Stress} < V_{cr}$ [Fig. 9(a)], electric field strength was not enough to cause depletion region to penetrate the GaN channel. Moreover, the carrier energy was not sufficient to enable the carriers to travel deeper into the GaN buffer. Attributed to these effects, we do not observe any noticeable carrier trapping in the GaN buffer when $V_{DS\text{-}Stress} < V_{cr}$. On the other hand, for $V_{DS\text{-}Stress} > V_{cr}$ [Fig. 9(b)], when electric field was higher than the critical field, depletion region penetrated the GaN channel and pushed the hot carriers deeper in the GaN buffer. A higher field across the GaN buffer also increases the trap ionization probability in the region near the field

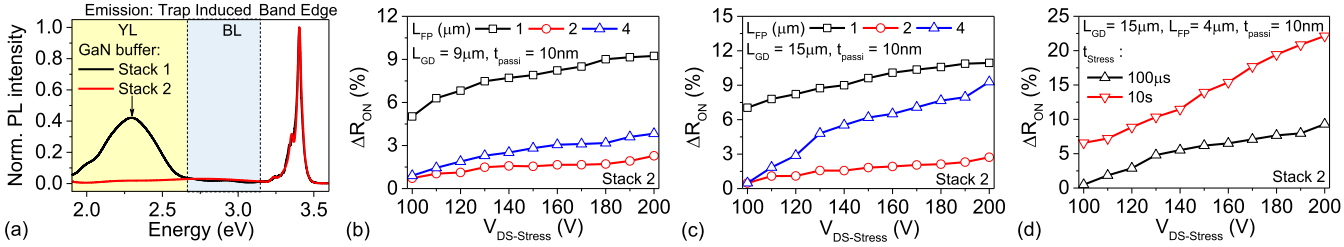

Fig. 12. (a) PL spectra of the GaN buffer obtained with 325-nm laser, showing the yellow (YL) and blue (BL) luminescence bands besides band-edge transitions. Stack 1 showed a distinct YL peak, which is attributed to radiative radiations from deep acceptor trap $[C]_N$ of a C-doped GaN buffer. No YL peak was observed in Stack 2 thereby establishing it to have a GaN buffer with very low C-doping. ΔR_{ON} for HEMTs, processed on Stack 2, as a function of field plate length (L_{FP}) for gate–drain distance (L_{GD}) of (b) 9 μm and (c) 15 μm showed no critical voltage for a stress time (t_{Stress}) of 100 μs. (d) ΔR_{ON} for HEMTs on Stack 2, as a function of stress time (t_{Stress}). It shows no critical voltage even for a 10 s stress. Device parameters are $L_{GD} = 15$ μm, $L_{FP} = 4$ μm and $t_{passi} = 10$ nm, for which HEMTs on Stack 1 showed the least critical voltage.

plate edge. Trap ionization can take place under the field plate, near the field plate edge and in the access region with a maximum ionization probability near the field plate edge. This leads to significant trapping of channel electrons in the acceptor traps in the GaN buffer near the field plate edge (around the depletion region). Any further increase in $V_{DS\text{-}Stress}$ increases the peak electric field near the field plate edge as well as increases the spread of depletion region in the lateral direction. This results in an increased injection of carriers in the GaN buffer and carrier trapping into a wider region between field plate edge and drain. Carrier trapping in the GaN buffer leads to depletion of 2-DEG above the trapped region. Its impact is depicted using TCAD simulations in Fig. 10(a), which shows that the change in ON-resistance is a linear function of depletion region length. Wider the depletion region, which can be due to carrier trapping in a wider area of GaN buffer, higher the ΔR_{ON}. Similarly, higher the carrier trapping, stronger the depletion, and higher the ΔR_{ON}. As a result of the phenomena explained through Figs. 6–10(a), a V_{cr} is observed beyond which ΔR_{ON} increases significantly. This is further confirmed by a similar increase in ΔR_{ON} observed in TCAD simulation of the device considering dynamic trapping of electrons in the GaN buffer, as shown in Fig. 10(b).

Above discussion establishes a complex interplay between the contributing parameters in determining dynamic performance of the device. This makes device design for optimizing dynamic performance a nontrivial task. A field redistribution technique to achieve maximized dynamic performance for HEMT devices is proposed in part II of this work.

V. Model Validation

As proposed above, V_{cr} is attributed to a critical field above which a finite electron trapping is observed in the GaN buffer. These trapped charges deplete the 2-DEG in the access region and cause ΔR_{ON}. To validate the mechanism proposed above, impact of buffer conditions (different carbon doping) and temperature on the V_{cr} and ΔR_{ON} are studied. If the behavior is associated with acceptor traps in the C-doped GaN buffer, then the buffer with low-carbon doping must show a significantly higher V_{cr}. Similarly, with reduced temperature, Poole Frenkel emission probability should reduce, which implies a higher carrier trapping during TAT, i.e. a lower V_{cr}. Furthermore, enhancing carrier injection, by external means, in the GaN

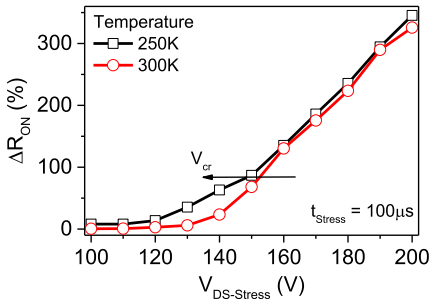

Fig. 13. Dynamic R_{ON} of the HEMTs extracted for different temperatures depicts a reduction in critical voltage for ΔR_{ON} as temperature is reduced. Device parameters are $L_{GD} = 15$ μm, $L_{FP} = 1$ μm & $t_{passi} = 20$ nm. Device was stressed for 100 μs.

buffer should also result into enhanced carrier trapping, which should lower the V_{cr} for a given stress time.

To validate the impact of buffer conditions, devices were fabricated over a GaN buffer with low carbon doping (Stack 2) while using the same fabrication and surface processing techniques as used for devices over carbon-doped GaN buffer (Stack 1). HEMTs on both the stacks have similar output ($I_D - V_{DS}$) and transfer ($I_D - V_{GS}$) characteristics, as seen in Fig. 11(a) and (b) respectively. Besides, the devices processed on both the stacks have similar surface conditions, as depicted in Fig 6(b), which shows similar surface leakage characteristics irrespective of the GaN buffer. To verify the GaN buffer condition, photoluminescence (PL) spectra were extracted using a 325-nm laser, to which SiN_x passivation as well as AlGaN is transparent, and therefore helps to selectively probe the GaN buffer. The PL spectra of Stack 1, as shown in Fig. 12(a), shows two distinct features: 1) broad yellow luminescence (YL) band with peak centered around 2.3 eV and 2) lower intensity ratio of blue luminescence (BL) to that of YL band (I_{BL}/I_{YL}), as compared to Stack 2. The YL peak is due to the deep acceptor state ($[C]_N$) introduced by carbon doping in GaN buffer [18]. Therefore, higher carbon concentration ($[C]_C$) leads to lower I_{BL}/I_{YL} [27]. Lack of a YL peak and an increased I_{BL}/I_{YL} in the PL spectra of Stack 2, as shown in Fig. 12(a), indicates a much lower C-doping in the GaN buffer of Stack 2, as compared to Stack 1. Fig. 12(b) and (c) show the ΔR_{ON} performance of HEMTs on Stack 2 for an OFF-state stress of 100 μs, which unlike to HEMTs on Stack 1, have very low ΔR_{ON} without any sign of

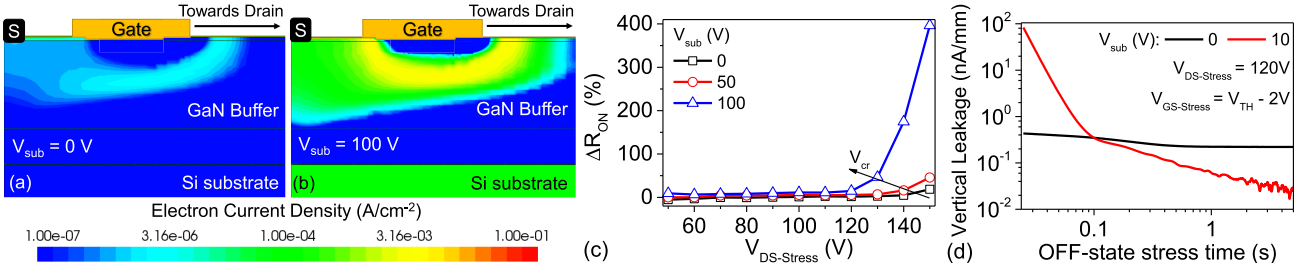

Fig. 14. Electron current density contours during the stress cycle for $V_{DS\text{-}Stress}$ of 200 V and a substrate bias (V_{sub}) of (a) 0 V, and (b) 100 V. It shows an increase in the injected carriers in the GaN buffer for a given $V_{DS\text{-}Stress}$ as V_{sub} is increased. Simulations used a 1.5 μm thick graded AlGaN stress-relieving layer. (c) ΔR_{ON} of the HEMTs experimentally extracted for different V_{sub} depicts a reduction in critical voltage as V_{sub} is increased. (d) OFF-state vertical leakage measured with respect to stress time as a function of V_{sub}. The vertical leakage significantly increases as the substrate is positively biased, indicating increased carrier injection and trapping in the GaN buffer. Device parameters are L_{GD} = 15 μm, L_{FP} = 1 μm and t_{passi} = 20 nm.

V_{cr} till 200 V. It is worth highlighting here that the HEMTs on Stack 2 did not show V_{cr} till 200 V even for a t_{passi} of 10 nm, for which HEMTs on Stack 1 had the lowest V_{cr}. Further, the HEMTs on Stack 2 did not show any V_{cr} till 200 V even for a t_{Stress} of 10 s, as seen in Fig. 12(d). Negligible ΔR_{ON} in the devices on GaN buffer with lower C-doping and absence of V_{cr} validates the proposed mechanism. Moreover, it further supports the argument that the V_{cr} in ΔR_{ON} is due to trapping in the C-doped buffer and is not directly dependent on surface conditions.

Further, to validate the impact of carrier trapping, ΔR_{ON} was measured as a function of device temperature. Fig. 13 shows that when temperature was lowered from 300 to 250 K, V_{cr} was reduced by 10%. This observation confirms the effective role of Poole Frenkel emission and TAT in governing the net trapped charge carriers across the GaN buffer, for a given stress time, which in turn governs V_{cr}. When Poole Frenkel emission was suppressed by lowering the substrate temperature, a net increase in trapped charge for a given stress time resulted in V_{cr} to appear at a lower $V_{DS\text{-}Stress}$, i.e. lower critical field.

Finally, in order to validate the impact of carrier injection into the GaN buffer, V_{cr} and ΔR_{ON} were extracted by forcing excess carrier injection deep into the GaN buffer by applying positive substrate bias (V_{sub}). The resulting current density profile extracted using TCAD simulations are shown in Fig. 14(a) and (b), which depicts an increase in the current injection in GaN buffer when V_{sub} was increased. Experimentally obtained ΔR_{ON} vs. $V_{DS\text{-}Stress}$ characteristics under such condition, as shown in Fig. 14(c), depicts a reduction in V_{cr} and an increase in ΔR_{ON} when V_{sub} was increased. Increased carrier injection is further confirmed experimentally in Fig. 14(d), which shows a higher vertical leakage when V_{sub} was increased under OFF-state stress. The vertical leakage falls as a function of time. This signifies a reduction in trap centers available for TAT, which indicates an increase in carrier trapping as a function of time. Besides, a crossover in the vertical leakage (for $V_{sub} > 0$ V) is seen, after which the vertical leakage for $V_{sub} > 0$ V falls below the $V_{sub} = 0$ V case. This shows a faster reduction in trap centers available for TAT for $V_{sub} > 0$ V, which validates increased rate of carrier trapping resulting into reduced critical voltage. This dependence of V_{cr} on temperature (Fig. 13) and substrate bias [Fig. 14(c)] is in contrast to that predicted by hole-emission theory [15]–[17]. Such a dependence can only be explained by trapping of injected electrons in buffer traps, as explained above. This establishes electron injection and trapping to be a dominant phenomenon, besides hole emission, controlling dynamic performance of the device at higher stress voltages. It is worth mentioning here that, in the absence of electron injection, hole emission from C-doping induced traps is expected to control the dynamic R_{ON} of AlGaN/GaN HEMTs, as discussed in detail in [15]–[17].

VI. Conclusion

Detailed OFF-state stress and dynamic R_{ON} (ΔR_{ON}) investigations of AlGaN/GaN HEMTs realized over carbon-doped GaN buffer have shown presence of stress time-dependent critical drain stress voltage (V_{cr}) above which a drastic increase in ΔR_{ON} of the device is seen. The V_{cr} drops significantly when stress time was increased. Interestingly, the devices were found to recover after removing the stress with recovery time constants in the order of 10's of seconds. Moreover, missing threshold voltage shift after OFF-state stress established negligible carrier trapping under the gate and ruled out V_{TH} shift as a possible reason for observed ΔR_{ON}. Extraction of ΔR_{ON} and V_{cr} as a function of lateral design parameters and passivation thickness hinted toward a strong role of electric field distribution within the GaN buffer. V_{cr} was found to reduce when field magnitude near the field plate edge was increased. Similarly, ΔR_{ON} was found to increase when lateral electric field was increased or when lateral depletion was widened. Similar surface leakage for different device dimensions and different carbon doping in GaN buffer confirmed observed V_{cr} to be independent of surface conditions. This is true as far as surface conditions do not seriously change the electric field profile in the buffer region, which we will see in Part-II of this work. On the other hand, reduced source current as a function of stress time indicates presence of TAT and carrier trapping into the trap states present in the GaN buffer. Moreover, the V_{cr} was found to be related to a critical electric field, which triggers the ionization of trap centers in the GaN buffer. As a result, stressing the device above critical drain voltage leads to significant trapping of channel electrons into the acceptor traps in the GaN buffer (around the depletion region) in the gate–drain access region. Carrier trapping in the GaN buffer leads to depletion of 2-DEG above the trapped region. Higher the carrier trapping, stronger the depletion,

and higher the ΔR_{ON}. As a result of these phenomena, a V_{cr} is observed beyond which ΔR_{ON} increases significantly. Any further increase in $V_{DS\text{-}Stress}$ results in an increased injection of carriers in the GaN buffer and carrier trapping into a wider region. Wider the depletion region, higher the ΔR_{ON}. Finally, the applicability of the proposed mechanism over the hole-emission model for higher stress voltages is validated by studying the impact of buffer conditions (with different carbon doping), device temperature, and substrate bias on V_{cr} and ΔR_{ON}. The role of acceptor traps in the C-doped GaN buffer was confirmed by demonstrating negligible V_{cr} and minimal ΔR_{ON} in buffer with lower carbon doping. Similarly, with reduced temperature Poole Frenkel emission probability was reduced, which was apparent from higher carrier trapping during TAT and lower V_{cr} observed. Finally, role of carrier injection was confirmed by forcing excess carrier injection in the GaN buffer by applying a positive substrate bias, which resulted into enhanced carrier trapping, thereby lowering V_{cr} for a given stress time.

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