Contact and Junction Engineering in Bulk FinFET Technology for Improved ESD/Latch-up Performance with Design Trade-offs and its Implications on Hot Carrier Reliability

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***Abstract*— In this work, the role of contact and junction engineering to improve ESD, Latch-up robustness as well as hot carrier reliability is discussed using 3D TCAD simulations. A FinFET technology calibrated to published data of a 14 nm technology is investigated. S/D contact and junction engineering in FinFETs can boost the ESD robustness by a factor of 6x compared to the basic process, however, adversely affects the hot carrier reliability. The trade-off of the essential technology guidelines for maximizing the overall reliability behavior and ESD/LU robustness are derived. Based on these guidelines, a hybrid contact/junction technology is proposed.**

***Index Terms*—Bulk FinFET, Electrostatic Discharge, Hot Carrier Induced (HCI) Degradation.**

I. Introduction

Bulk FinFETs have replaced their counterpart owing to improved scalability without seriously affecting the cost [1]. ESD, Latch-up and Hot Carrier Induced (HCI) reliability of these devices have been studied in detail in the past [3] – [10], however often without any correlation between them. Recent investigations have shown the key parameters, as impact ionization location and intensity along-with trapping immunity, affecting the HCI behavior for bulk FinFETs, can be controlled by various process optimizations and gate oxide quality [3]. Detailed analysis on the self-heating effects over the HCI degradation characteristics of FinFETs were elaborated in [4], [8], [10]. The impact of fin width quantization over the hot carrier energies, described the increase of HCI degradation for larger widths [7]. However, a thorough design and technology investigation correlating the ESD and HCI reliability of FinFETs is required to explore newer device design architectures and guidelines to achieve a robust FinFET technology. Improving the efficiency of the parasitic bipolar has been a well-known technique to improve the ESD robustness of FinFET devices [11]. Our recent work has shown that, by exercising contact silicidation and junction engineering, one can improve the bipolar efficiency of Bulk Fin-based SCR ESD protection devices [12]. However, it's implications on HCI reliability is not known yet, which is relevant for I/O and core devices in the same technology. In general, hot carrier implications of technology optimization for ESD robustness was not explored for a FinFET technology. This work addresses this missing aspect and attempts to derive contact/junction engineering and design guidelines for an overall reliability improvement.

II. Simulation Methodology

3D electro-thermal simulations, using 3D TCAD, were performed for both ESD and HCI investigations [15]. To accurately account for realistic thermal boundary conditions, back-end of the line (BEOL) metal interconnect stack was incorporated in the simulation setup. ESD simulations were performed using a 100ns pulse stress, whereas for HCI simulations, stress pulses of 1000s were used with I_D-V_G extraction in between the stress routine at log scale time durations. To account for hot carriers and hot carrier induced

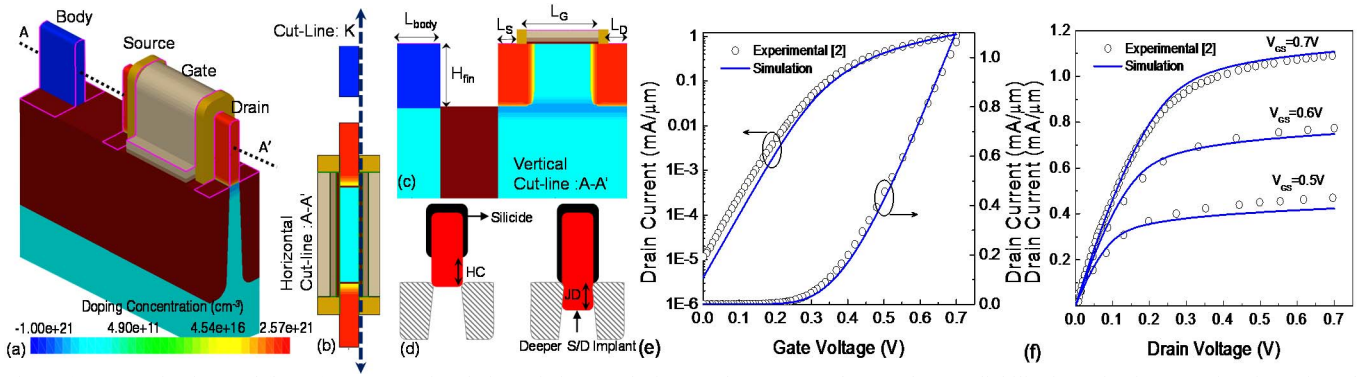

Fig. 1: (a) Isometric view and (b) & (c) cross-sectional view of FinFET platform under ESD, Latch-up and HCI reliability investigations. Devices investigated in this study are simulated to mimic the I/O functionality with an EOT of 2nm. (d) Contact engineering by partial silicidation as a function of contact height (HC) and junction engineering by using deeper junctions (JD) for improved ESD robustness [8], (e) and (f) TCAD calibration of mobility models and fin confinement effects in MOS operation [2].

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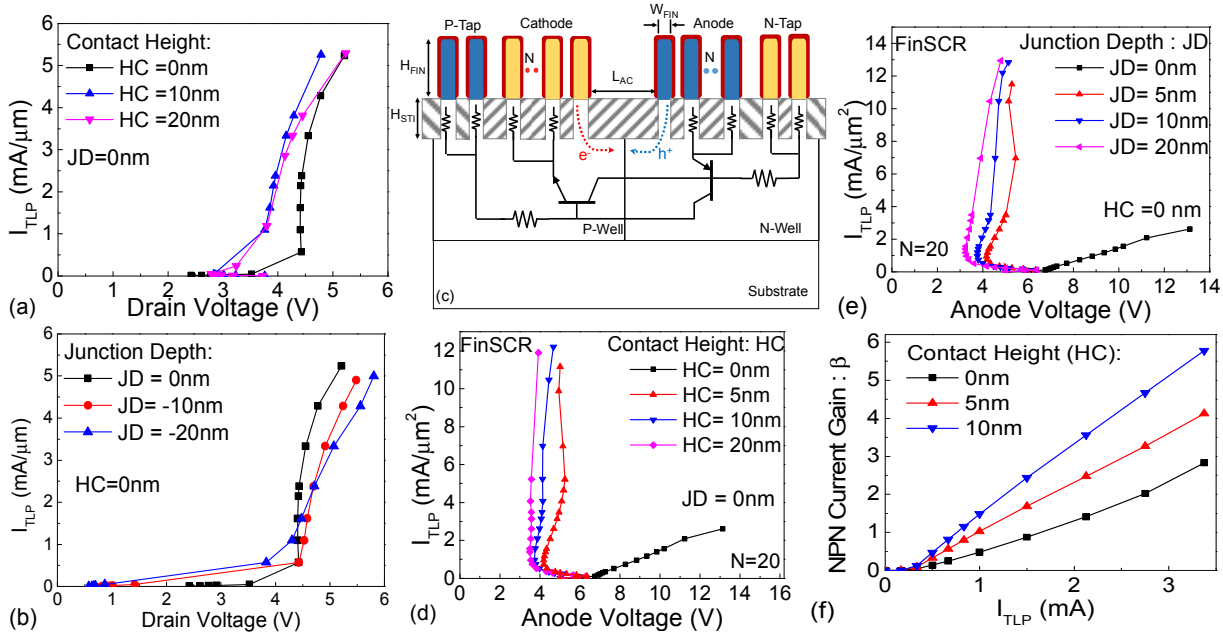

Fig. 2: TLP IV characteristics of (a)-(b) ggFinFET and (d)-(e) SCR with contact and junction engineering respectively. (f) Increasing contact height makes the parasitic bipolar efficient. Case with HC<JD is a promising option for mitigating latch-up.

degradation, Monte-Carlo simulations with Spherical Harmonic Expansion of Boltzmann Transport Equation was used with stress equivalent to maximum allowed drain voltage (V_D) and gate bias = $V_D/2$. The stress voltage levels were so chosen to establish maximum hot carrier induced degradation in accordance with a recent analysis on HCI behavior of bulk FinFETs [3]. Integral degradation models were applied to accurately reflect the physics of interface trap generation process, through the de-passivation of hydrogen (H) and subsequent H transport towards the interface [15].

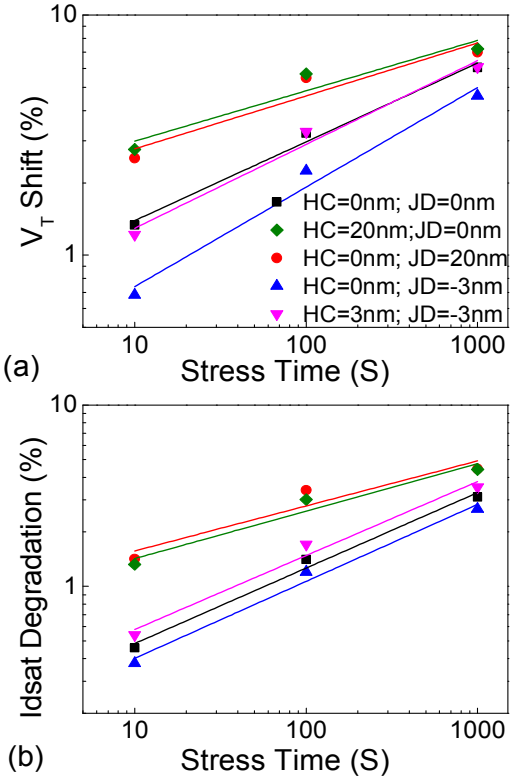

Fig. 3: Hot carrier induced (a) threshold voltage (V_T) shift and (b) ON current (Idsat) degradation with respect to stress time, as a function of contact/silicide height and relative junction depths.

III. ESD Robustness and HCI Reliability Trade-off

Fig. 1a-c shows the isometric and cross sectional views of bulk FinFET device, with key parameters such as Junction Depth (JD) and Contact Height (HC) (shown in Fig. 1d, e) which are considered for contact/junction engineering [12]. A well calibrated TCAD simulation setup was used for this investigation [2], the results of which are illustrated in Fig. 1e, f. The TLP I-V characteristics of grounded gate FinFET (Fig. 2a & b) and Fin-SCR (Fig. 2d & e) show improved ESD robustness for HC>0 and/or JD>0. Fin-SCR (Fig. 2c) with HC>0 and JD>0 offers higher It2 and deeper snapback when compared to design with HC=0nm & JD=0nm, which is attributed to improved parasitic bipolar efficiency gained (Fig. 2f) through contact/junction engineering. On the other hand, least bipolar efficiency and missing SCR action for HC=0nm and JD=0nm depicts highest Latch-up robustness of this case, which gets even better with HC>-JD. These trends are attributed to fall in the minority carrier conduction through the emitter-base junction of the parasitic bipolar, which recovers in the presence of contact/junction engineering and improves ESD/snapback behavior (Fig. 2c & d) [12]. This apparently was found to affect the channel field profile and hot carrier distribution, which favorably or adversely affects the hot carrier degradation, as discussed in detail below.

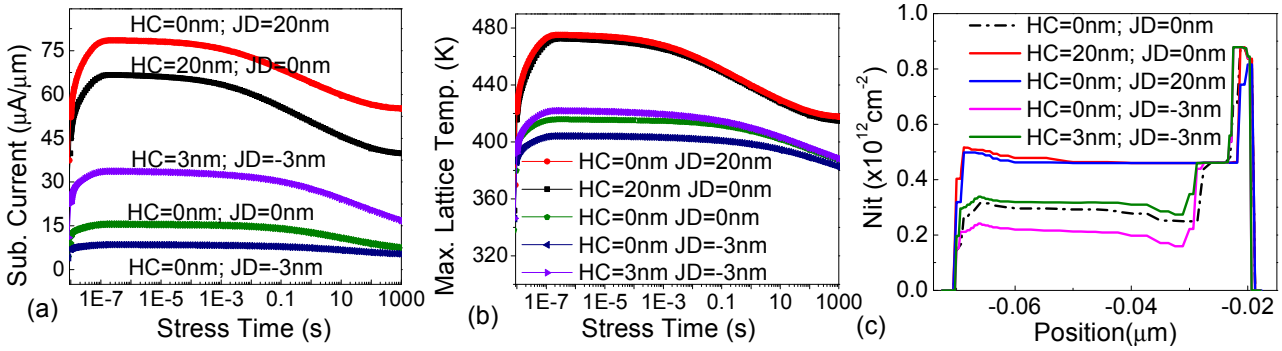

Fig. 4: (a) Normalized Substrate current per unit layout width & (b) maximum lattice temperature with respect to stress time and (c) interface trap concentration extracted along the channel after 1000s of stress cycle, as a function of contact/silicide height and relative junction depths.

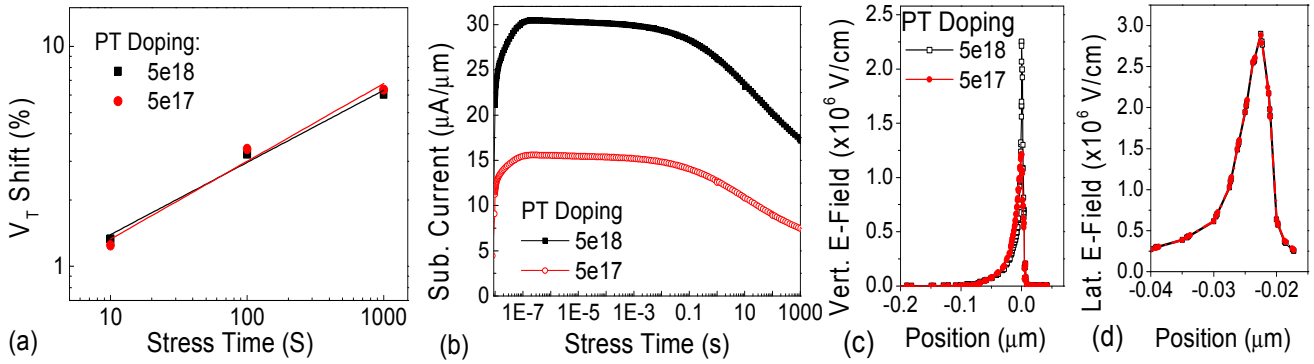

Fig. 5: (a) HC induced threshold voltage and (b) extracted normalized Substrate current per unit layout width with stress time for different punch-through doping. (c) Vertical and (d) lateral electric field profile for different punch-through doping.

A. Contact/Junction Engineering

Partial silicidation (HC>0) lowers the contact area over the S/D region, which increases the thermal resistance and leads to enhanced lattice heating. It is worth highlighting that in FinFET technology, most of the heat is taken away from the BEOL metallization and hence any change in the contact scheme is expected to affect the heating behavior [13]-[14]. Fig. 3 shows the HCI degradation as a function of HC and JD. It is to be noted that, three cases are compared here: silicide edge aligned to S/D junction (HC=-JD); silicide edge above S/D junction (HC>-JD); and silicide edge crossing S/D junction (HC<-JD). In general, devices with HC>0 and/or JD>0, which offers improved ESD robustness, leads to a faster and higher degradation when compared to the standard contact silicidation and junction profile scheme (HC=0nm and JD=0nm). This is attributed to the enhanced impact ionization and regenerative action, as evident from the higher substrate current (Fig. 4a). For the same case, lattice temperature was found to be highest (Fig. 4b), which is due to increased thermal resistance between S/D contacts and bond pads. This increases the hot carrier density in the channel region as evident from increased interface trap density (N_{IT}) along the channel (Fig. 4c), which leads to faster device degradation. On the other hand, when silicide edge overlaps or aligns with the S/D junction (HC≤-JD), impact ionization was mitigated as well as thermal resistance was lowered. This is evident from reduced substrate current and mitigated lattice heating, which leads to slower device degradation for the design with HC≤-JD.

B. Punch Through Doping (PT)

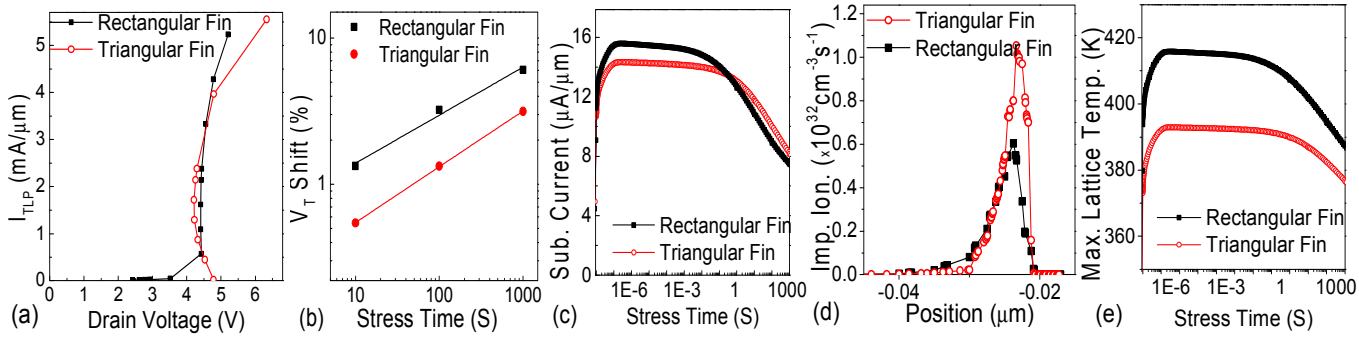

Fig. 6: (a) TLP I-V characteristics, (b) Hot carrier induced threshold voltage shift, (b) & (d) extracted normalized Substrate current per unit layout width and maximum lattice temperature with stress time, and (c) Impact Ionization profile extracted along the channel, for rectangular and triangular Fin Shape.

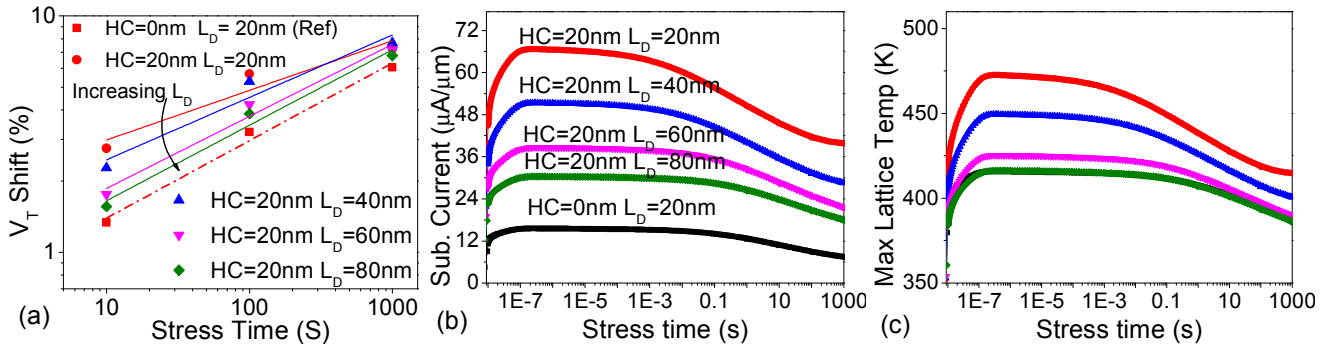

Fig. 7: Hot carrier induced (a) threshold voltage (V_T) shift, (b) extracted normalized Substrate current per unit layout width and, (c) maximum lattice temperature with respect to stress time for increasing drain contact length (L_D) with different contact heights.

V_T adjustment and low leakage transistors are designed using controlled doping under the active Fin, isolating the S/D regions. Fig. 5a shows no difference in the rate of degradation, as the punch through doping (PT) is varied, despite the fact that, higher doping results in higher impact ionization, which is evident from the higher substrate current (Fig. 5b). This is attributed to the unaltered lateral electric field profile, Fig. 5d (and thereby lattice heating), which leads to unaffected interface trap generation (N_{IT}). However, higher substrate current is due to increased vertical field (Fig. 5c), under the drain junction, which does not alter the hot carrier degradation.

C. *Fin Shape*

Fig. 6a shows enhanced ESD performance for the Triangular fin shaped devices due to their efficient parasitic bipolar. It is worth highlighting that, despite having similar substrate current (Fig. 6b) and relaxed electric field profile along the channel and lower impact ionization (Fig. 6c), a rectangular fin degrades faster. This is attributed to increased lattice heating (Fig. 6d), which is due to higher current per unit Silicon area. Contrastingly, Triangular Fin consists of smaller Si volume compared to the rectangular Fin, which allows an improved heat dissipation through the gate. This mitigates the hot carrier induced trap generation and effectively improves the hot carrier integrity of these devices.

D. *Drain Contact Engineering*

Fig. 7a depicts the effect of drain contact length (L_D) on the hot carrier induced degradation characteristics. It is observed that, with enlarged drain contact length, the peak electric field along the channel gets relaxed which suppresses the impact ionization and hot carrier generation, as evident from lower substrate current (Fig. 7b). This mitigates the maximum lattice temperature (Fig. 7c) across the device under stress. As a result, attributed to suppressed hot carrier generation and mitigated lattice heating, increasing L_D improves the hot carrier reliability.

E. *Silicide Blocking SB*

Silicide blocking allows the bipolar efficiency to improve which enhances the ESD performance, as illustrated in Fig. 8a. At the same time, this technique allows to stretch out the peak channel electric field, which is visualized by lower impact ionization and thereby lower substrate current (Fig. 8d). This relaxes the lattice temperature (Fig. 8c) and mitigates the hot carrier generation, which explains slower hot carrier induced device degradation of silicide blocked devices (Fig. 8b).

IV. Hybrid Contact and Junction Engineered Technology

Fig. 9 shows a proposal for unique contact/silicide height and junction depth for different device types on the chip, depending on their application, along-with a proposed process flow. The cases discussed in Fig. 3 can be deployed for various blocks in a chip. For instance, silicide edge above S/D junction (HC>-JD) with deeper junction profile is recommended for ESD SCR and diodes. Here, partial silicidation and deeper junction improves the diode and SCR action. The deeper junctions can be realized by the Anti-Punch Through (APT) Implants, which are used for the threshold voltage control in

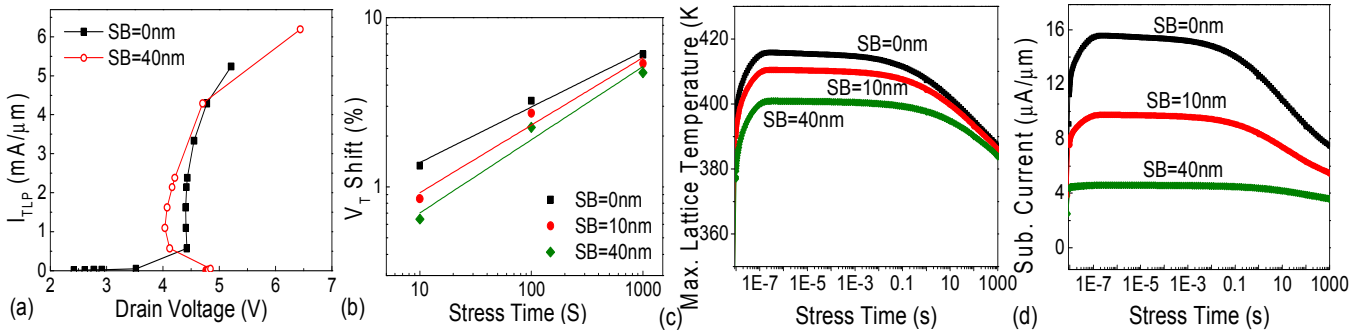

Fig. 8: (a) TLP characteristics of silicided and silicide blocked (SB=40nm) grounded gate FinFET device. (b) Hot carrier induced threshold voltage shift, (c) maximum lattice temperature and (d) extracted normalized Substrate current per unit layout width as a function of stress time, for different silicide blocking lengths.

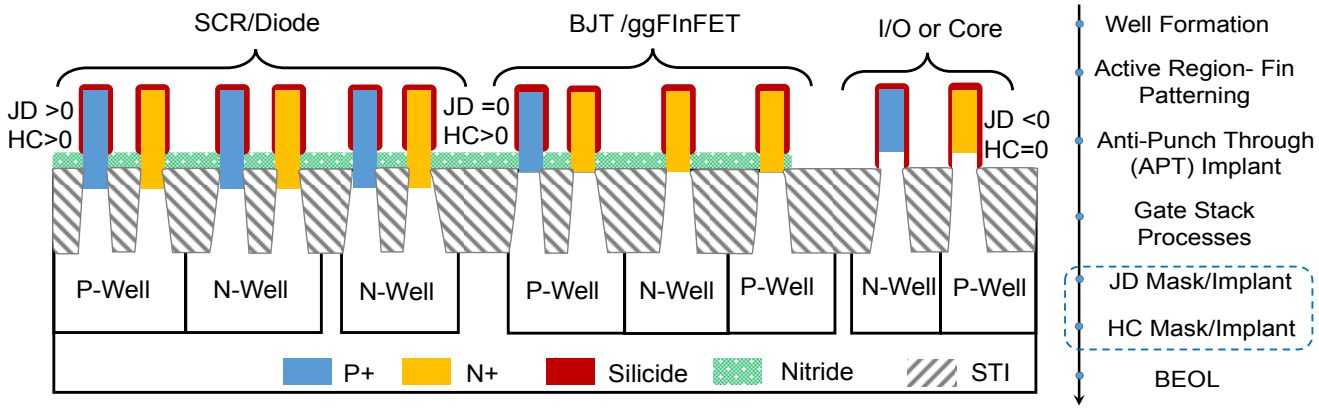

Fig. 9: Proposed hybrid contact/silicide and junction profiles with the process flow for FinFET technology, as a solution towards improved ESD robustness for protection devices while achieving reliable I/O and core devices.

baseline FinFET processing. It is worth highlighting that, this approach does not add any additional processing complexity. Having the same silicide edge above the S/D junctions, without the deeper junction is proposed for ESD BJT and grounded gate FinFET (ggFinFET) devices. Here, partial silicidation improves the parasitic BJT turn-on. On the other hand, silicide edge crossing S/D junction (HC<-JD) with shallower junction or at least aligned to S/D junction (HC<-JD) with standard junction is proposed for the I/O and core FET devices. Here, silicidation or contact region crossing S/D junction suppresses the hot carrier generation and mitigates lattice heating, which minimizes the hot carrier induced degradation. It is to be noted that, in order to achieve partial contact silicidation (HC>0) and shallower junction (JD<0), additional processing steps are to be incorporated. The respective JD and HC Implant steps can be performed prior to the BEOL metallization loop. Using this method, by integrating selective contact silicidation and junction profile engineering, robust ESD protection devices as well as reliable I/O or core devices can be achieved in FinFET technology.

V. Conclusion

We revealed the impact of contact and junction engineering on the ESD and HCI reliability of Bulk FinFET devices. With increasing distance of the salicided contact region from the fin base (HC) and/or the distance of the S/D p/n-junction to the Fin base (JD), the ESD robustness can be improved. However, long term HCI degradation characteristics have shown to get worse. This was found to be due to a pronounced thermal effect and a higher impact ionization when HC>0 and/or JD>0. However, this can be mitigated by keeping the junction encapsulated within the silicide region (i.e., HC <-JD). It was found that an increased punch-through doping, though it affects the ESD behavior, doesn't change the HCI trends. A triangular fin cross-section was found to be better in terms of ESD robustness, due to its efficient bipolar and also HCI degradation, due to its efficient heat dissipation. Silicide blocking and drain contact length, which improves the ESD robustness, were found to improve the HCI behavior simultaneously. Finally, a proposal for hybrid technology with mix of contact/junction profiles are made to optimize ESD/Latch-up as well as HCI robustness of a FinFET technology.

TABLE I. Summary Chart of ESD and HCI Robustness for Different Device Design Guidelines

Design Parameters	ESD Robustness	HCI Reliability
Contact/Junction Engineering	↑	↓
Punch-Through Doping	No Change	No Change
Fin Shape- Triangular	↑	↑
Drain Contact Engineering	↑	↑
Silicide Blocking	↑	↑

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