Defect-Assisted Safe Operating Area Limits and High Current Failure in Graphene FETs

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Abstract— **In this work, a unique measurement setup, involving integration of transmission line pulse tester with Raman spectrometer, is used to investigate the pulsed safe operating area (SOA) boundary of graphene field effect transistors (GFETs). Physical insight into various SOA boundaries, i.e., near-electrical, electro-thermal and thermal, is given. Unique defect-assisted degradation in channel and its correlation with the carrier transport as well as failure is revealed, with the help of electrical as well as Raman spectroscopy based investigations during well controlled pulse-stressing of GFETs. The SOA and power to fail dependency on carrier concentration and nature of carrier transport is addressed.**

***Index Terms*— Graphene, Electrostatic Discharge, Safe Operating Area (SOA).**

I. Introduction

The prospects of employing graphene as a channel material for high frequency RF transistors has recently garnered interest of the fraternity [1-3]. Although the material enjoys high thermal conductivity and boasts gate controlled high current density [4-5], there exists challenges to make Graphene FETs work in their theoretical limits (THz). Several works have demonstrated reduction in graphene-metal contact resistance, a major bottleneck for RF applications [6-7]. Obtaining saturating output characteristics for high voltage gain [8-9] and use of 2D gate dielectrics [10] have been vital breakthroughs. However, its practical deployment mandates a full investigation of potential reliability issues and recursive changes at material and process fronts. In this regard, there have been efforts from different groups to understand the long-term reliability [11-12] and electrostatic discharge (ESD) reliability [13-15]. However, due to limited understanding of failure of the novel material, the electrical limits and material properties specifying safe operating area for Graphene FET is still not precisely explored. Unlike silicon, which fails via temperature-induced melting, a mechanism involving oxidative damage dominates the failure of graphene. Arguably, failure characterization unique to graphene should be employed for all reliability investigations. Being a 2-dimensional material any change in the lattice of graphene can be precisely captured and investigated through Raman spectroscopy. In this contribution, we employ Raman spectroscopy in conjunction with electrical/TLP stress to explore the SOA limits of GFETs and investigate the mechanism of both material and device failure. The obtained insights are useful in designing ESD protection strategies in this technology.

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II. Device Fabrication & Measurement Technique

SOA investigations were performed on Graphene FETs processed on CVD-grown monolayer graphene. The process flow involves transfer of graphene from initially grown copper to Si/SiO_2, e-beam patterning of channel and contacts, followed by palladium/gold evaporation. Post-metallization annealing (300°C) enabled contact improvement, while HfO_2

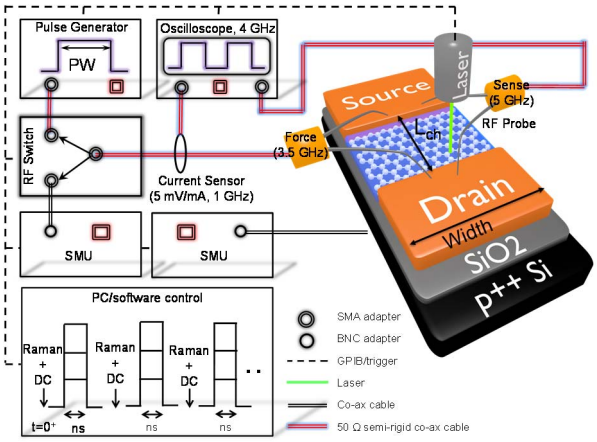

Fig. 1: Unique measurement setup showing the integration of Transmission Line Pulsing (TLP) with Micro Raman Spectroscopy and DC I-V measurement setup after every stress cycle. To understand SOA boundary which is limited by setup after every stress cycle. To understand SOA boundary which is limited by different degradation phenomenon a unique setup is required, that integrates material characterization with electrical (both pulse and DC).

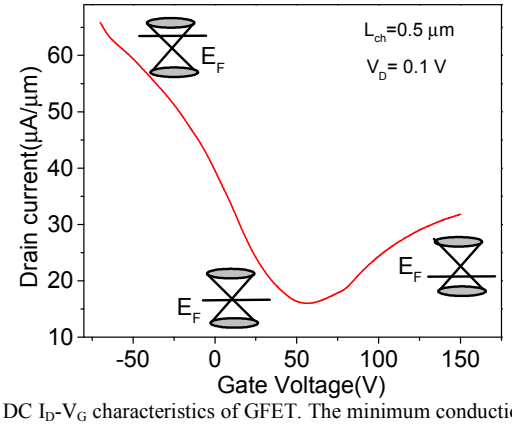

Fig. 2: DC I_D-V_G characteristics of GFET. The minimum conduction point is Dirac Point where the Fermi level coincides with the center of Dirac Cone (inset). Left side of Dirac point conducts because of holes, whereas right side conduction is due to electrons.

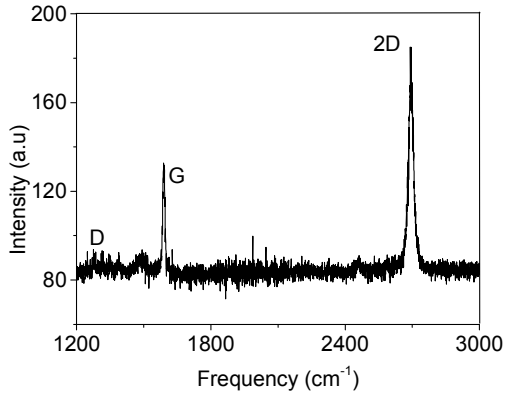

Fig. 3: Raman Data of the pristine graphene used in this work. 2D/G>1 and suppressed D peak shows the monolayer coverage by large grain CVD Graphene.

passivation was done to ensure field integrity of the gate electrode and minimize the environmental degradation. Unique measurement set-up that integrates Transmission Line Pulsing (TLP) system, DC sweep and micro-Raman spectroscopy (Fig.1) was deployed to investigate SOA of Graphene FETs and on-the-fly degradation/failure analysis of the channel. Employed TLP system can generate voltage pulses of duration ranging from 1 ns to 1.5µs. The setup can sense ultra-low currents up to 50 µA, with 5mV/mA current sensor and mixed domain oscilloscope with a resolution of 1 mV/dec. The low bias DC measurement (similar to the leakage current measurement in conventional silicon technology) is performed after every pulse to track the device degradation electrically. Micro-Raman spectroscopy captures the vibrational modes in the material besides structural changes. Raman setup in this work uses a 532nm laser source and spot size of 1 µm. The spectroscopy is used to study the defect evolution and its density in graphene channel after application of set of electrical pulses.

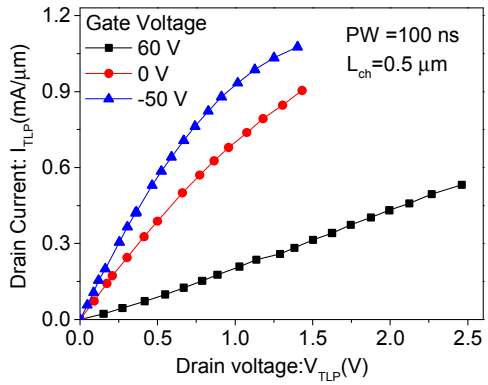

Fig. 4: Pulse I-V characteristics of GFET at different gate voltages stressed with 100 ns pulses to obtain the electro-thermal SOA boundary. Failure current increases with increase in the gate bias, while the failure voltage falls. The three gate voltages are chosen in the hole dominated conduction region (left side of the Dirac point). Last point in the TLP plot is the failure point, the line which connects them is the SOA boundary.

III. Safe Operating Area (SOA)

Three different types of SOA are defined based on the type of stress-near-electrical (PW=10 ns), electro-thermal (PW=100 ns) and thermal (PW=1000 ns). The time-scales are chosen to account purely thermal/electrical effects or a combination of both. The term near-electrical is used as the thermal diffusion time for a typical micron-long graphene is few nano-seconds, due to which a precise boundary for electrical SOA cannot be defined. All three SOA measurements are done at gate voltages below Dirac-point, where the hole current dominates (Fig. 2). From the electro-thermal and near-electrical SOA (Fig. 4 and 5), it can be observed that increase in gate bias results in increased failure current and decreased failure voltage. Failure thresholds for near-electrical stress are higher than the electro-

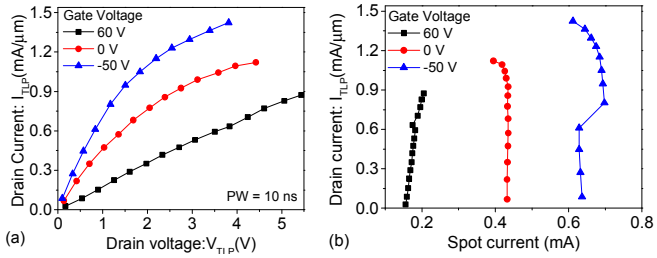

Fig. 5: Pulse I-V characteristics of GFET stressed with 10 ns wide pulses. Short duration pulse stressing mitigates thermal effects, and defines the near-electrical SOA. Near electrical failure thresholds are higher than the electro thermal and thermal failure. (b) DC spot current measured after each pulse.

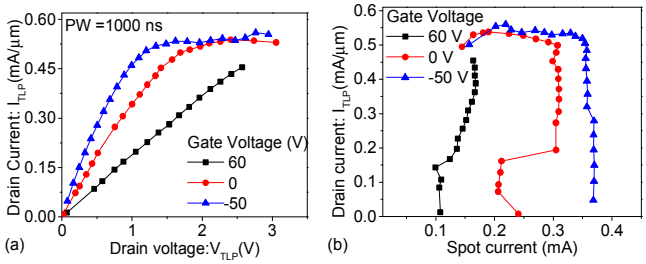

Fig. 6: (a) Pulse I-V characteristics of Graphene FET stressed with 1000 ns pulses to obtain the thermal SOA. Channel degradation at high gate-bias shrinks the thermal SOA. (b) The DC spot current data shows fall in drain current with increasing stress.

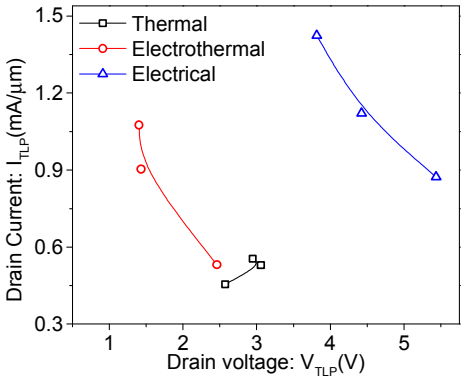

Fig. 7: Summary of thermal, electro thermal, near-electrical SOA in graphene transistors. Severe channel degradation shrinks the thermal SOA, However, reduced heating in channel improves the electrical SOA boundary.

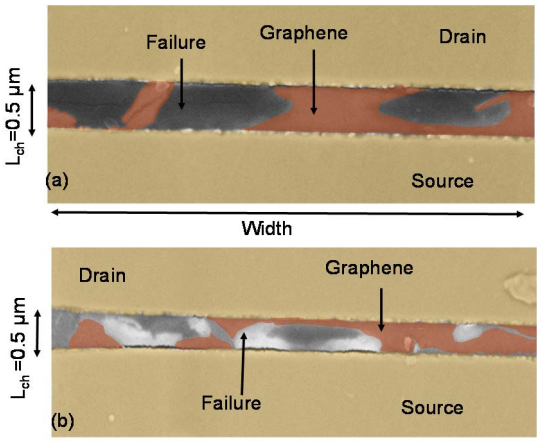

Fig. 8: False color SEM image of GFET showing the signature of (a) electrothermal failure (PW=100 ns) (b) thermal failure (PW=1000 ns). Electro-thermal failure results in local oxidative breakdown of graphene, whereas the thermal failure not only results in oxidative damage, but also results in degradation of gate oxide.

thermal. At a constant drain voltage, reduction in gate voltage, relative to Dirac-point, induces more charge carriers in the channel, and reduces the channel resistance resulting in higher failure current. Stressing with short pulses reduces the population of out-of-equilibrium optical phonons, resulting in reduction in lattice temperature. Consequently, failure thresholds are higher for near-electrical SOA. Thermal SOA investigations in Fig. 6 reveal that pulse drain current saturates with corresponding reduction in the DC spot measured drain current for higher gate voltages, which is the signature of device degradation. Fig. 7 summarizes various SOA boundaries in graphene FETs. Post failure SEM images (Fig. 8) reveal that the electro-thermal failure leads to local oxidative breakdown of graphene, whereas the thermal failure not only results in oxidative damage, but also results in gate oxide degradation

IV. Device Degradation and Defect-Assisted Failure

The failure mechanism governing the SOA boundary is discussed in this section. The investigation is carried out through a repeated cycle of stress-measure-spectroscopy events, where high-field electrical pulses are used to induce defects in the device, which in turn are probed, first through low-bias DC sweep, and then through Raman spectroscopy. Graphene FETs with short (0.5µm) and long-channel lengths (10µm) are discussed separately, where channel dimensions are compared with thermal healing length of Graphene, which is around 300 nm. The long-channel devices show discrete and monotonous decrease in low-bias DC spot as depicted in fig.9b after every stress cycle, while preserving the Dirac-point (minimum conduction point) as in fig.9c. The discrete drop in low-bias DC spot with successive stress-probe cycles indicate an increase in defect density across the graphene channel. The effective device width for ESD current conduction decreases with every stress probe cycle. The increase in defect density is further corroborated by post-stress Raman mapping of the

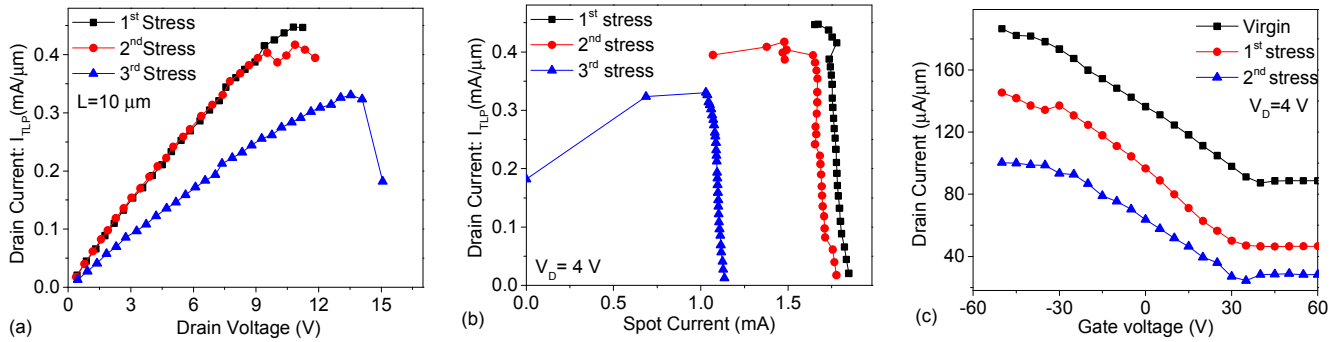

Fig. 9: (a) Pulse I-V characteristics of a long channel GFET. The device is stressed to high fields and stressing is aborted when a change in the device spot current is observed, which is again restarted to observe the accumulative behavior of stressing. (b) The spot current data for the consecutive stress levels. (c) The DC I_D-V_G characteristics extracted after one complete stress measurement. Clearly, the reduction in the channel current with every stress cycle is observed which is related to the degradation of the graphene channel with every stress cycles.

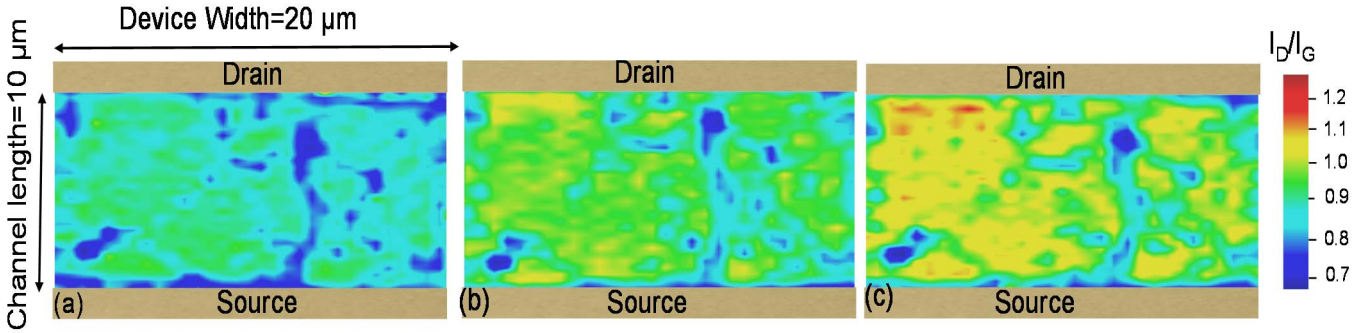

Fig. 10: The intensity ratio of D-peak to the G-peak (I_D/I_G) in the Raman spectra extracted for (a) pristine device (b) after the stress but before the catastrophic failure (c) post failure. The increase in D-peak to G-peak ratio with increase in stress shows an increased defect density across the graphene channel.

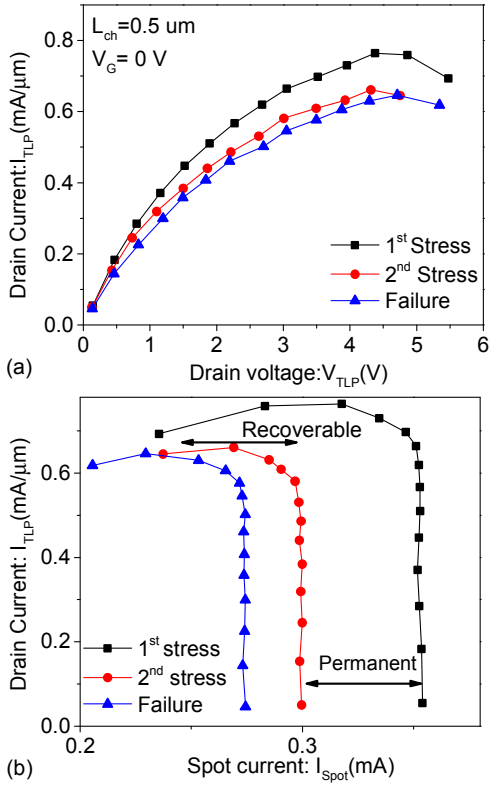

Fig. 11: (a) Pulse I-V characteristics of a short channel GFET for different stress cycles. The measurement routine is stopped and repeated when degradation in spot measured drain current is observed. (b) The spot current after every pulse. Unlike the long channel FETs, the degradation has both recoverable and permanent components. The recoverable portion is attributed to the interface traps between the graphene and SiO_2 at high source-drain fields, whereas the permanent component is due to the graphene channel degradation.

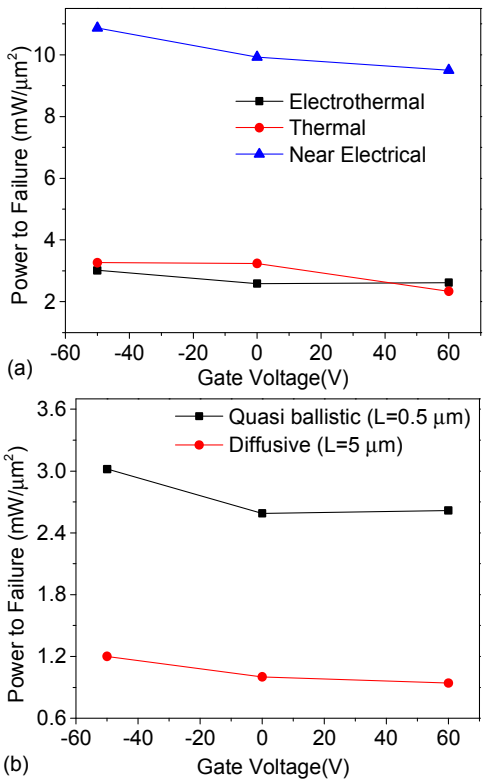

Fig. 13: Power-to-failure (PF) per unit area as a function of gate bias for (a) different stress conditions (near electrical, electrothermal, thermal) (b) different transport conditions. A 10% reduction in PF with decreasing gate bias is found, which is attributed to the increase in the channel resistance. For ultra-low pulse durations, higher PF is observed due to mitigation of channel heating. Quasi ballistic channel fails at high power levels because of mitigated scattering in the channel.

device, which shows an increase in the intensity of normalized defect peak (I_D/I_G) throughout the channel (Fig. 10). Interestingly, the intensity of defect peaks shows increment with each stress cycle, without showing any significant spatial change. This observation suggests a defect- mediated channel degradation and failure in Graphene FETs. A point vacancy or stones-wales defect in the channel acts as a scattering center, for channel carriers subsequently cause the localized heating near the defect sites. The local rise in the temperature induces oxidative removal of carbon atoms, whose spatial spread is found to increase with subsequent stress cycles. Contrary to long-channel devices, the analysis of short-channel devices shows partial recovery in DC spot current (fig.11) after every stress-probe cycle. DC spot current in n+1th stress cycle, do not match with the last DC spot current value, in nth stress cycle (fig.11b). Permanent degradation component is the defect assisted channel degradation as in long channel device case. However, recoverable degradation can be attributed to trapping/de-trapping in gate dielectric. High source-drain field in short-channel device causes the carrier trapping at the

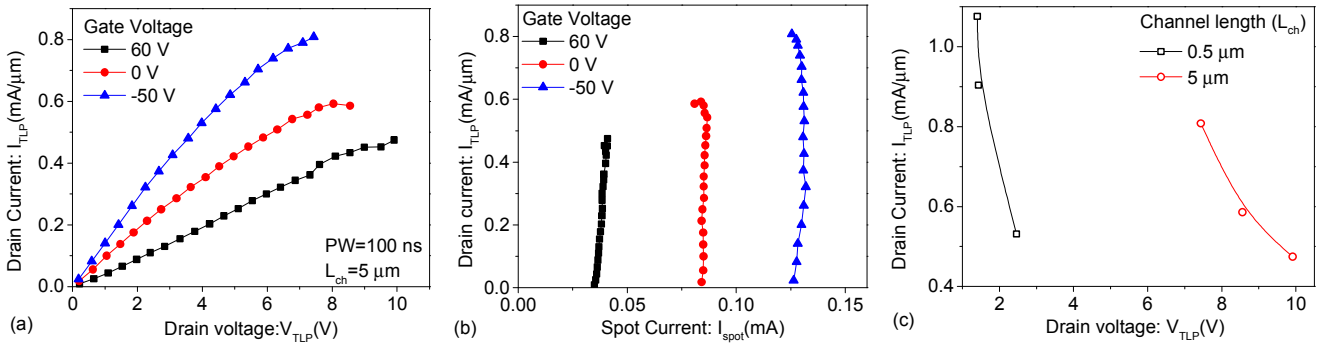

Fig. 12: (a) Pulse I-V characteristics of long channel (L=5 μm) GFET at different gate voltages stressed with 100 ns pulses. (b) spot current measured after each pulse (c) electro-thermal SOA boundary comparison of short and long channel devices. SOA improves with increase in channel length as the failure voltage increases, while failure current falls.

graphene and SiO_2 interface, which shifts the Dirac point and adds to the existing channel degradation. When the bias is turned OFF the de-trapping causes the recovery in measured drain spot current.

V. Carrier Transport and Associated Failure

Carrier transport dependency on the SOA boundary and failure power density under various stress and transport conditions are investigated. For long-channel FETs the electro-thermal SOA (Fig. 12) increases due to higher failure voltage. However, the failure current is found to fall with increasing channel length which is attributed to the diffusive nature of transport. In these devices, the carrier experiences excessive scattering as it traverses from source to drain and loses its energy continuously to the lattice, which in turn increases the lattice temperature and lowers the failure current. The failure power density is also observed to be a strong function of carrier transport and stress conditions but shows a weak dependence on gate bias (Fig. 13). The fall in power-to-failure (PF) for diffusive channels (long-channels) is mainly attributed to the higher probability of scattering / localized heating induced defect generation.

VI. Conclusion

The safe operating area boundary for graphene FETs is investigated in conjunction with Raman spectroscopy. Increase in gate induced channel carrier concentration decreases the channel resistance and was found to increase failure current however failure voltage was found to decrease. Electrical SOA is found dominate because of the reduction in channel joule heating attributed to the reduced optical phonons population. Unique approach used in this work for degradation analysis reveals that, in long channel devices, localization of the heat in the channel near defect sites causes permanent channel degradation. However, in short channel devices attributed to the high source-drain field, the interface carrier trapping between graphene-SiO2 also adds to the performance degradation, however this component of degradation is found to be recoverable when the bias is turned off. Thermal SOA shrinks because of the degradation and heat spreading in the channel region. Furthermore, failure power density significantly falls for diffusive transport dominated devices as the long channel FETs are more prone to defect induced localized heating and subsequent defect generation.

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