On the ESD Behavior of a-Si:H based Thin Film Transistors: Physical Insights, Design and Technological Implications

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Abstract— **In this work, we present detailed physical and technological insights into the ESD behavior of a-Si:H TFTs. Pre-Breakdown mechanism is investigated using Electron microscopy, Raman spectroscopy and on-the-fly I-V/ C-V measurements in between TLP stress. Competing mechanisms of device failure and effect of various performance parameters on failure threshold are investigated. Effect of channel dimensions on failure mechanism is thoroughly explored. For the first time, ESD behavior of a-Si:H display technology based Gated diodes and Resistors is reported. Detailed investigation on Drain Underlap devices and their possible usage as I/O protection device in a-Si:H technology is discussed.**

***Index Terms*—Amorphous silicon, Electrostatic Discharge, Thin film transistors, Degradation, Dielectric breakdown, Gated Diodes, Drain Underlap.**

I. INTRODUCTION

Thin-film transistors (TFTs) on glass form an integral part of display technology and constitute a vital element in liquid crystal displays. Presence of glass in the displays restricts the thermal budget of the fabrication process and demands the use of materials with low processing temperatures. Hydrogenated amorphous silicon (a-Si:H) is one such material, which can be processed with low thermal budgets (< 350°C) and, hence is suitable for glass-based display technologies. Hydrogenated amorphous silicon has been used for a variety of applications including sensing [1], [2] and in display driver circuits [3]. While preliminary work has been done to understand the instabilities in a-Si TFTs [4], [5] and their ESD behavior [6], [7], [8], a gap still exists in complete understanding of their ESD behavior, both from physics as well as technology point of view. This work provides a detailed physical insight into the failure mechanism, pre-breakdown degradation mechanism, change in material properties with stress and effect of various device design and performance parameters under ESD conditions by employing a plethora of measurements including on-the-fly I-V, C-V and Raman spectroscopy. This work, for the first time, provides insights into technological aspect of ESD behavior of a-Si:H technology, discussing ESD behavior of gated diodes, resistors and drain under-lap devices.

II. DEVICE FABRICATION & CHARACTERIZATION

Fig.1 shows the cross-section of back channel passivated and back channel etched TFTs used in this work. Corning glass, cleaned using Piranha Solution is used as the substrate. The fabrication process begins with e-beam evaporation of Al/Cr on corning glass, followed by its patterning using wet etching, which serves as a gate electrode. Post-metallization of gate electrode, a series of PECVD based processes are carried out to deposit 200nm thick SiN_x a 150nm thick a-Si:H layer and 300nm thick SiN_x, where the a-Si:H acts as channel, while SiN_x layers act as gate dielectric and channel passivation respectively. Following the patterning of passivation layer, a 30nm thick n-doped a-Si:H layer was deposited using PECVD. Subsequently, the active layer and the gate insulator were patterned using RIE. The source/drain electrodes (Mo/Al) were deposited using DC sputtering and patterned by wet etch. Finally, RIE was employed to etch-out the n-doped a-Si:H layer from the channel region. The devices were annealed at 423K for a period of 1hr before characterization. ESD characterization was done using a 50Ω TLP setup. A current sensor with a sensitivity of 0.5mV/mA and a 4 GHz Oscilloscope are used to capture waveforms. The setup was

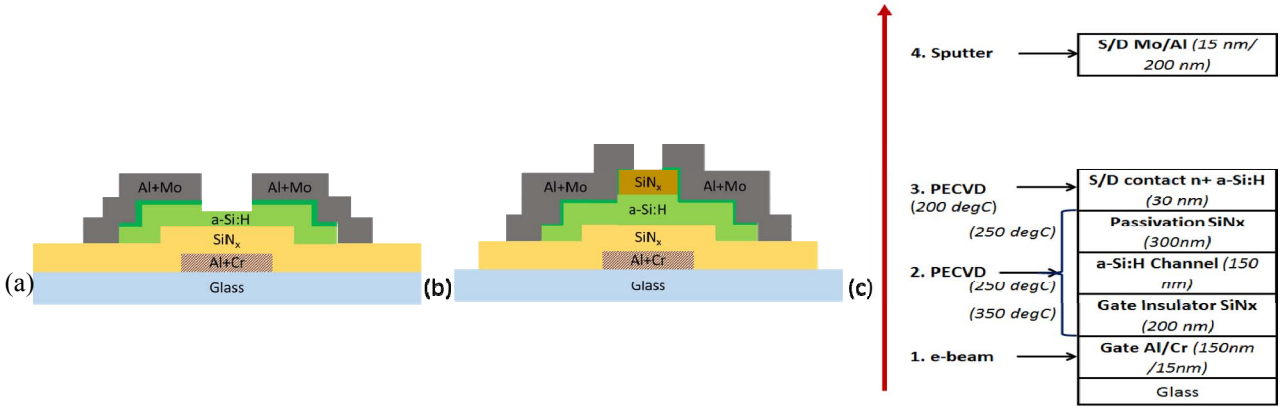

Fig.1: Cross-sectional view of (a) Back Channel Etched (b) Back Channel Passivated TFT used in this work. (c) Depicts the process flow followed in this work to realize BCP TFT devices under test.

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calibrated using a standard surface mount resistor and a zener diode. Unless stated otherwise, grounded gate devices were stressed with a pulse, of time period 100ns and rise time 10ns. To study failure, a low DC bias is applied after each pulse and drain current was monitored. Exploration of device degradation and changes in material properties was done by on-the-fly I-V, C-V and Raman Spectroscopy measurements after ESD stress pulses. DC I-V measurements between stress pulses were done for a lower voltage range so as to avoid device degradation. On-the-fly Raman spectroscopy was done using 532nm laser with a spot size of 1µm. Fig. 2 shows DC I-V characteristics of devices under test.

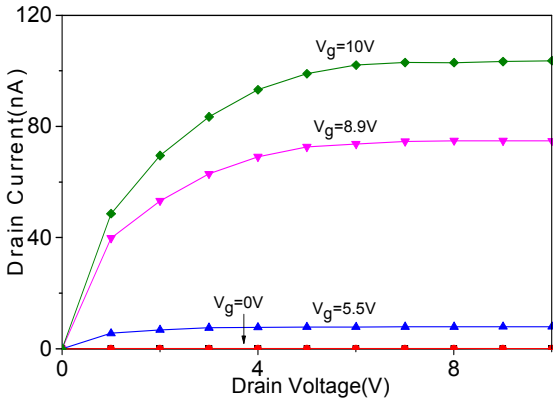

Fig 2: DC I-V characteristics of a-Si:H TFTs. S/D form ohmic contact with a-Si:H due to n^+ a-Si:H layer. On/Off ratio is $>10^4$ and threshold voltage is approximate 4V.

III. ESD BEHAVIOR OF A-SI:H TFTS

A. TLP characteristics

The TLP characteristics of a-Si:H TFTs shown in **Fig. 3** depicts two modes of operation – (1) sub-threshold conduction, where the device shows a linear operation with high on-resistance; (2) device failure, characterized by voltage snap-back and sudden increase in TLP current (**Fig. 4**). Due to high on-resistance, the drain current is immeasurably low. The device failure takes place in steps with localized failure spot spreading across the channel width. **Fig. 5** shows the SEM image of a failed device with localized failure spot. In some devices, complete channel failure is also observed. Spot measurements (**Fig. 3**) show that device degradation starts only after 60V, which forms the threshold of degradation.

B. Pre-Breakdown Degradatiion and Failure Mechanism

I-V, C-V and Raman characterizations were performed to understand the pre-breakdown degradation mechanism. Following changes can be observed after a stress voltage of 60V (**Fig. 6 and 7**): (i) degradation in drain current (ii) increase in threshold voltage (iii) a shift in C-V characteristics. These behaviors can be attributed to injection of charge carriers, i.e. electrons, into the gate dielectric. Injections of electrons lead to an increase in threshold voltage

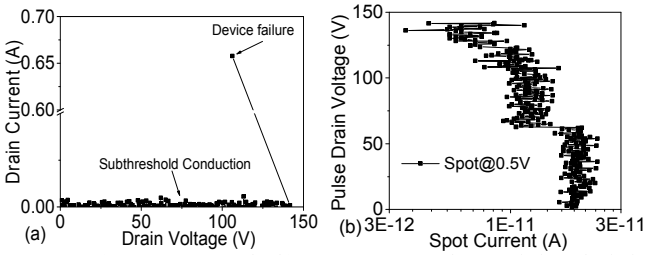

Fig. 3: (a) TLP I-V and (b) Spot current characteristics depicting breakdown and degradation behavior of TFTs. Due to low mobility of a-Si:H, TLP current is immeasurably low. Spot characteristics show that degradation sets in after 60V stress.

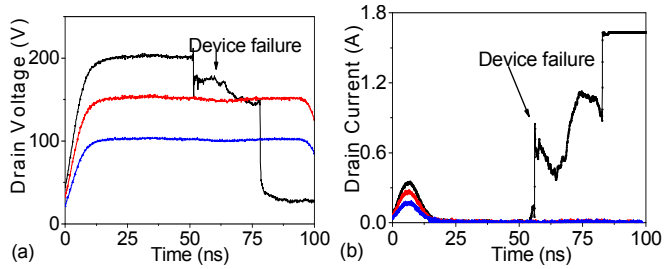

Fig. 4: Transient (a) TLP Voltage and (b) TLP current characteristics extracted from 100ns pulse stress. The device failure is characterised by transient drop in drain voltage and corresponding increase in drain current, which takes place gradually in steps until the channel experiences a completely failure.

and causes shift in C-V characteristics. It is also observed that as the stress increases to 120V, the gate-drain capacitance and drain current has turned around to initial values although a similar trend is not observed on source side. This can be explained by selective compensation of charge trapping in dielectric on the drain side of channel. Excess electrons generated during impact ionization are swept to drain and mask the effect of electrons trapped in dielectric. In the pre-breakdown regime, there is no change in the Raman signature, thus the device shows no material change in channel region (**Fig. 8**). The device failure occurs either due to avalanche breakdown in the channel or due to dielectric breakdown. Post-damage, it is observed that the Raman peak is shifted to 515 cm^{-1}, showing a shift towards higher

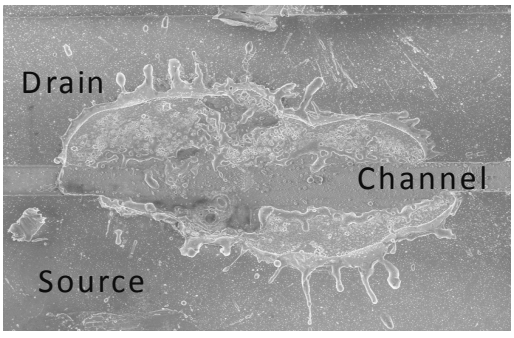

Fig. 5: Post failure SEM micrograph of TFT device with partially damaged channel. Damage occurs locally in the channel region which creates a short between source and drain. Due to excess current, post failure, contact melting also takes place.

crystallinity on account of channel heating during device failure.

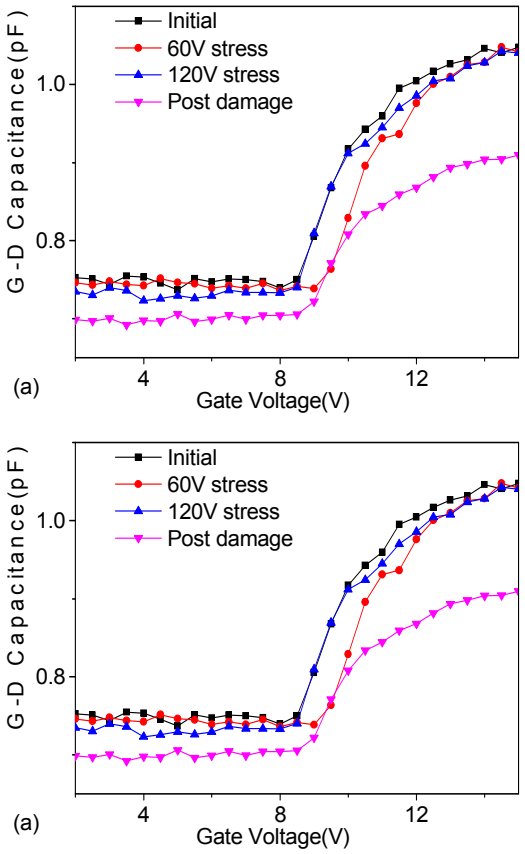

Fig. 6: C-V characteristics of a-Si:H TFTs before and after applying ESD stress. (a) Gate-Drain capacitance and (b) Gate-Source capacitance measured at 1MHz. A parallel shift in C-V characteristics, in both cases, is visible after 60V stress, which at the drain side recovers to initial value after 120V stress, while the source capacitance continues to shift in the same direction. This is due to generation of excess electrons near the drain contact at higher stress voltages, which masks the effect of charge trapping at gate.

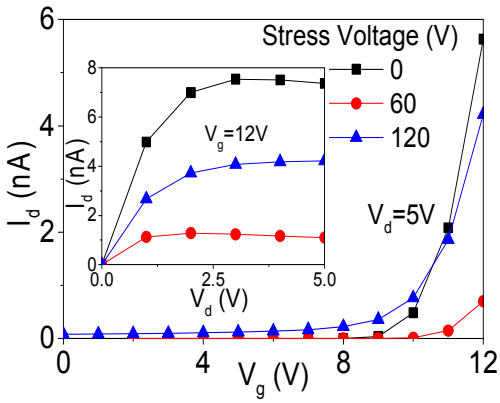

Fig. 7: DC I-V characteristics (I_d-V_d in Inset) depicting device degradation before permanent failure. Performance recovery from 60V to 120V takes place due to generation of excess electrons near drain contact.

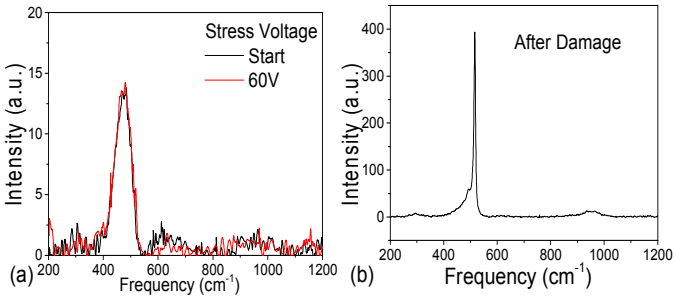

Fig. 8: Raman spectra (a) Before and (b) After, device failure. There is no shift in Raman signal with stress before the permanent device failure depicting absence of material change as a function of stress. Post damage, Raman peak shifts to 515cm^{-1}, depicting a change from amorphous to near-crystalline nature of Si, possibly due to excessive channel heating during device failure.

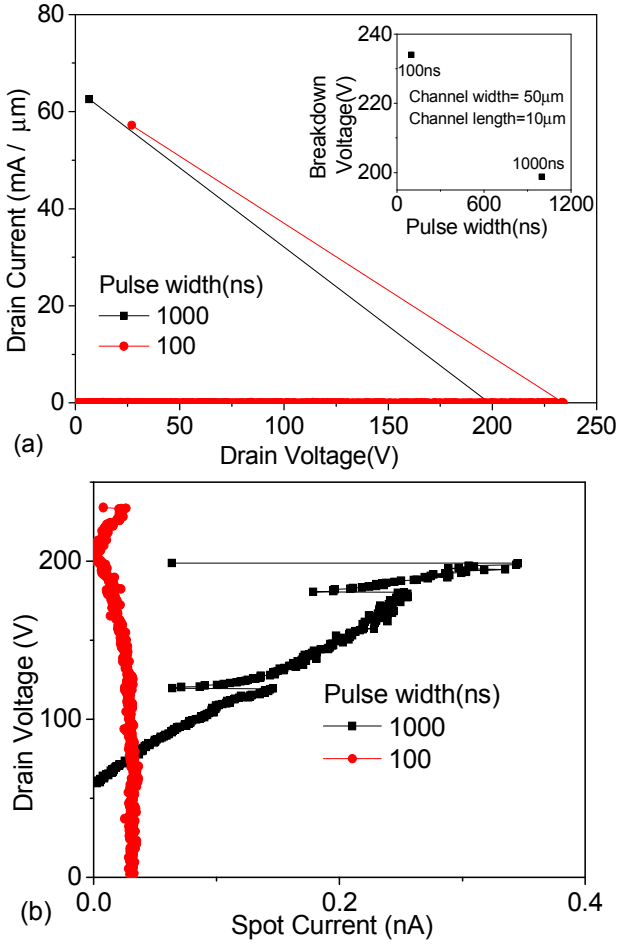

Fig. 9: (a) TLP I-V characteristics with different pulse widths and (b) spot measured drain current vs pulse/stress drain voltage. Fall in failure voltage with TLP pulse width (inset) depicts thermal nature of device failure. Increased device degradation in case of 1000ns pulse stress when compared with 100ns stress depicts self-heating assisted trap generation and device degradation during ESD stress.

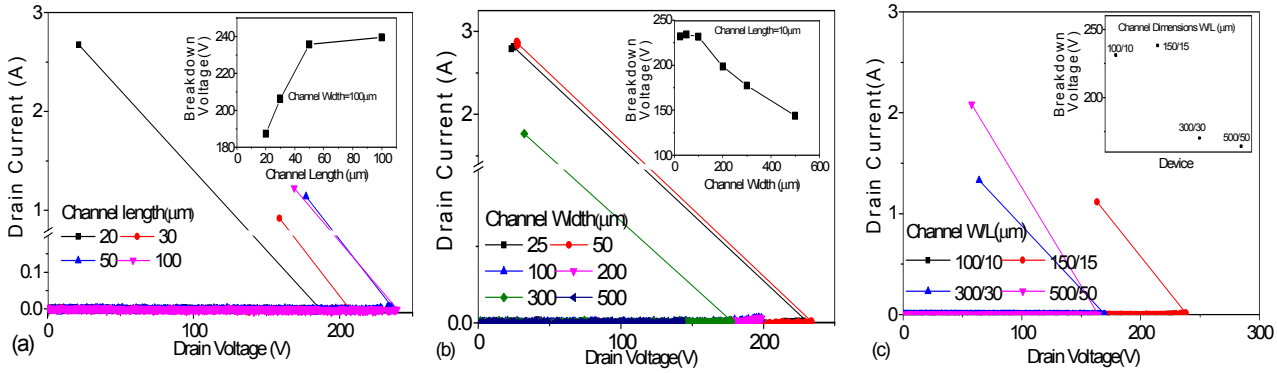

Fig. 10: TLP characteristics as a function of channel dimensions. (a) Variation of Channel length, (b) Variation of Channel width and (c) Variation of Width/Length ratio, while keeping the ratio constant. For smaller channel length punch through dominates the breakdown/turn-on and failure, while for larger dimensions dielectric breakdown dominates the catastrophic failure. For devices with constant Width/Length ratio, failure threshold didn't follow a unique trend. For smaller widths, it improves with channel length, however for larger widths it lowers due to increased probability of failure along the width.

IV. Factors Influencing ESD Behavior

To study the thermal nature of breakdown, devices were stressed with pulse widths of 100 and 1000ns. It is observed from **Fig. 9** that breakdown voltage reduces with pulse width.

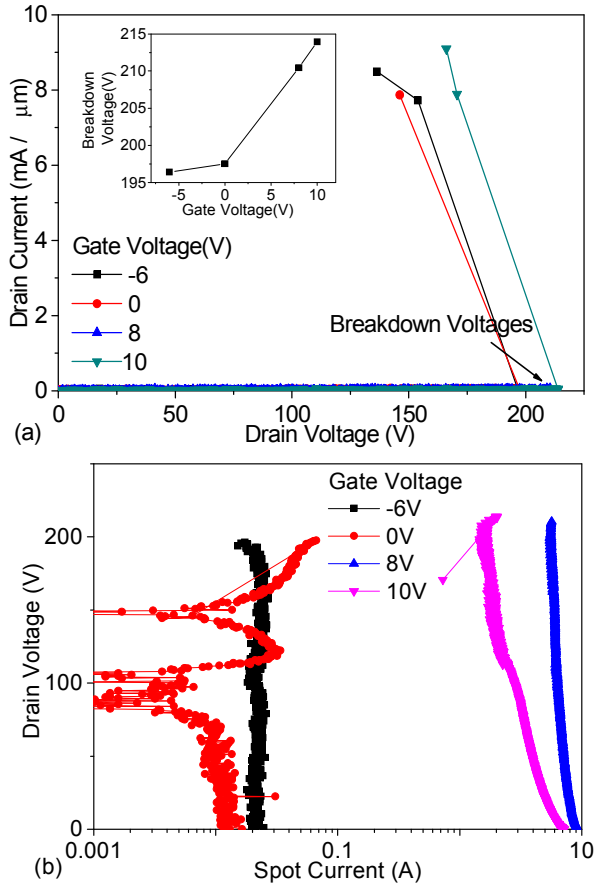

Fig.11: Effect of gate field on the ESD behaviour. With increase in gate bias, breakdown voltage increases in such a way that gate-drain field at breakdown remains constant. Device shows performance degradation and recovery only for V_G=0V as under accumulation hot electrons in the channel are repelled away from gate and under inversion condition, inversion charge masks the excess electron presence near drain.

Reduction in breakdown voltage with increase in pulse widths points towards thermally-assisted breakdown behavior Increase in channel temperature leads to de-trapping of electrons in a-Si:H, leading to an increased concentration of electrons in channel, thus favoring avalanche breakdown. Higher temperature also aids avalanche breakdown leading to a reduction in breakdown voltage with pulse width. Channel dimensions play an important role in determining the failure mechanism. To explore the effect of channel dimensions on breakdown, devices with varying device channel dimensions were characterized (**Fig. 10**). It is observed that as channel length increases, breakdown voltage initially increases and then saturates. It is also observed that as channel width increases, breakdown voltage initially remains constant and then decreases. These behaviors can be explained as follows: For relatively smaller dimensions, punch-through leads to device failure, leading to dependence of breakdown voltage on channel length but not channel width and for larger dimensions, dielectric breakdown dominates. Devices with a

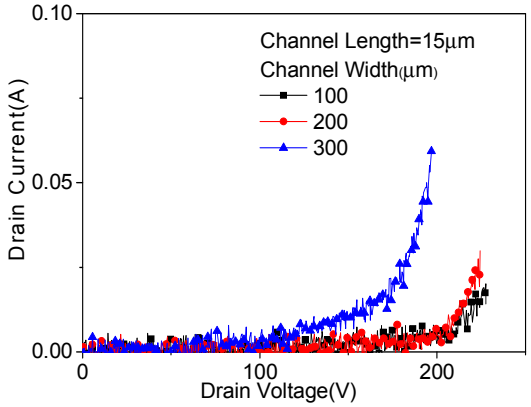

Fig. 12: TLP I-V characteristics of gated diode devices. Gate coupling leads to a lower failure voltage, although improvement in failure current is also observed. This is due to increase in carrier concentration in channel with drain voltage, thereby aiding avalanche breakdown.

constant width/length ratio have varying breakdown voltages. This is caused due to difference in actual device dimensions and hence, failure mechanism. Gate field dependency is studied by biasing gate voltage during ESD characterization. Observations in **Fig. 11** can be explained by dielectric breakdown mechanism in those devices.

V. GATED DIODES, RESISTORS AND DRAIN UNDERLAP DEVICES

ESD behavior of FinFet based Gated diodes has been well explored [9], [10] while a similar exploration is still lacking for a-Si:H based Gated diode. **Fig. 12** shows the TLP I-V characteristics of a-Si:H based gated diodes. Gated diodes offer higher failure current but a lower failure voltage as compared to a typical TFT. This is due to higher concentration of charge carriers in channel aiding avalanche breakdown. ESD behavior of drain underlap devices has been studied by measuring devices with varying dimensions. Two-terminal a-Si:H resistors play an important role in a-Si:H technology and have been used in a-Si:H based circuits [11]. **Fig. 13** shows the TLP I-V characteristics of a-Si:H based resistors. These devices undergo avalanche breakdown and the breakdown voltage shows saturation with channel dimensions **Fig. 14** shows the TLP I-V characteristics of drain under-lap TFTs. It can be observed that drain underlap devices provide improved ESD robustness as compared to typical TFTs. This behavior can be attributed to electric field relaxation provided by drain underlap region, which reduces the maximum electric field under the drain edge and hence improves ESD robustness. On account of their improved ESD robustness, drain underlap devices can be used as I/O protection elements in a-Si:H technology..

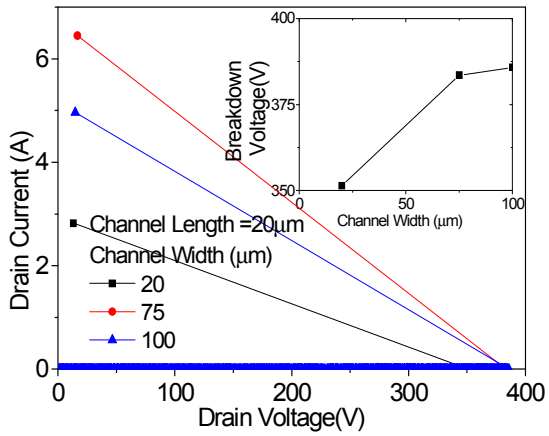

Fig. 13: TLP I-V characteristics of a-Si:H resistors. Breakdown voltage vs channel width (inset). Resistors fail due to avalanche breakdown occurring in the channel region. Breakdown voltage also increases up to a critical channel length and then saturates.

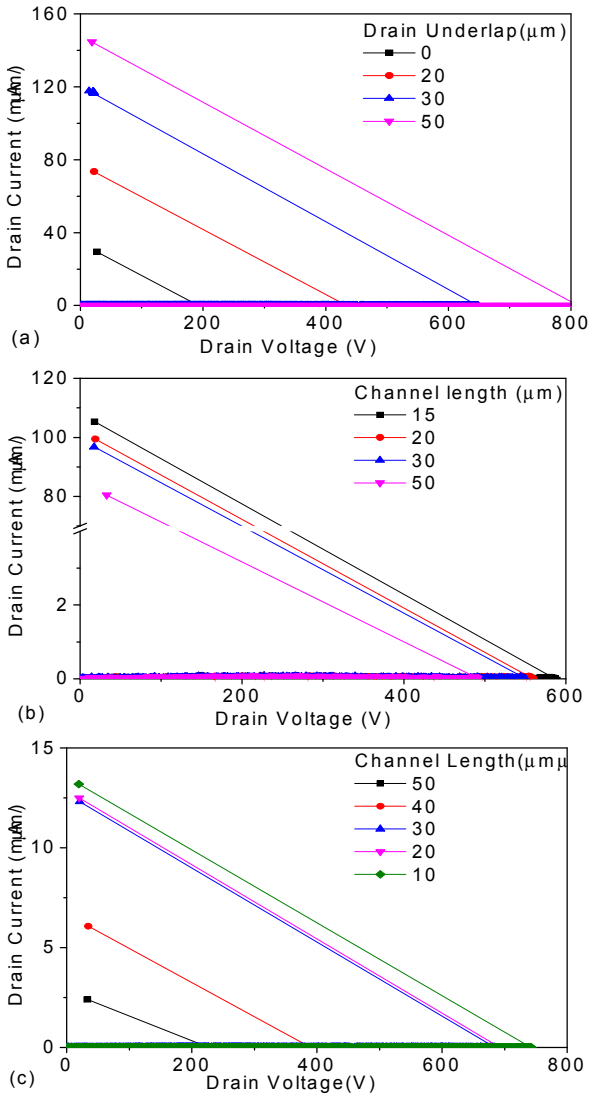

Fig.14: TLP I-V characteristics of various Drain Underlap device structures (a) Constant channel length, (b) Constant drain underlap length and (c) Constant Source-Drain length. Drain underlap devices provide high ESD robustness and can be used as I/O protection devices in a-Si:H technology.

VI. CONCLUSION

Detailed physical insights into the ESD behavior of a-Si:H TFTs has been presented. Two regions of operation are observed in the TLP characteristics: - 1. Sub-threshold conduction 2. Device failure. It is observed that device degradation starts at about 60 V due to charge injection into gate dielectric. Degradation recovery at the drain side is observed due to sweeping of excess electrons near the drain contact although a similar observation is not made for the source side. It is found that device failure occurs either due to avalanche breakdown or due to dielectric breakdown, with channel dimensions playing a crucial role in determining the failure mechanism. Stress induced change in material properties is observed with help of Raman characterization. Finally, ESD behavior of gated diodes, resistors and drain

under-lap structures are investigated in detail and it has been observed that drain under-lap devices provide better ESD robustness, hence paving the way for their use as I/O protection devices.

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