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On the ESD Reliability issues in Carbon electronics: Graphene and Carbon Nano Tubes

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Abstract—**In this work, we present experimental investigations and new physical insights into the ESD behavior and failure of large area CVD graphene RF transistors and Multiwall carbon nanotubes. Unique two stage defect induced failure in graphene transistors is reported for the first time. Detailed study on the self-heating and its implication on the failure current and carrier transport in graphene FETs is addressed with the transient analysis in ESD time scales. A unique power law like behavior is also reported in Multi wall CNT's.**

***Index Terms*— Graphene, Electrostatic Discharge, Multiwall Carbon Nano Tubes.**

INTRODUCTION

It's almost a decade since the carbon based materials like graphene and carbon nanotubes are being explored for electronic integrated circuit applications [1]. Graphene, the thinnest material reported till date, attributed to its superior electrical and thermal properties, is widely explored for RF transistor applications [2]. The other carbon allotrope, Carbon Nano Tubes (CNT's) with its extraordinary ability to carry current and immune to electro migration effects are potential candidates to replace copper interconnects in future applications. On the other hand, Electro Static Discharge (ESD) events are fundamental and major reliability threats to the IC. There were previous efforts to understand ESD behavior of graphene and CNT's, for example the very first demonstration on graphene was [3] reported using exfoliated material and then using Chemical Vapor deposition [4], more recently [5], a matured graphene technology was used for ESD explorations. The ESD physics of carbon nano tubes is also well explored [6-9]. In this work we are presenting unique failure mechanism in graphene transistors under ESD stress conditions. This work also addresses the self-heating effects in the both graphene and carbon Nano tubes that are critical under ESD like stress conditions.

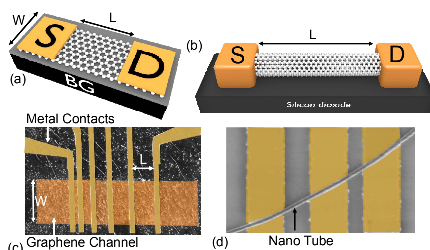

Fig.1 Atomistic view of the (a) back gated Graphene FET (b) Substrate supported Multiwall Carbon Nano Tubes. Here S&D are the source and drain metal pads. False color Scanning Electron Microscopic (SEM) image of (c) Graphene Transistors with different source to drain length (d) Carbon nanotubes.

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NEW INGIGHTS INTO THE ESD BEHAVIOUR OF GRAPHENE TRANSISTORS

Back gated GFETs (fig. 1(a) & (c)) and multiwall CNTs are stressed with commercial TLP testers. The technology details of this work can be found in [10].

1) *Unique Defect Induced failure*

Reported graphene failure modes are abrupt failure when channel is exposed to the ambient, gradual failure when graphene channel is encapsulated with the dielectric [8]. A unique failure signature is observed in this work along with the other reported types. Fig. 2 depicts the TLP IV characteristic of the back gated GFET with a channel length of 500 nm. The following observations can be made (a) The drain current increases linearly until the first collapse in the current (termed as first breakdown). (b) After first breakdown the drain current almost remain constant until the second or final breakdown /collapse in the current. (c) The two stage characteristic is also found in spot current data (Fig. 2(b)). The DC spot current after the first breakdown kept reducing with increase in the TLP stress. The reported two stage failure characteristics are unique. This behavior in graphene FET is attributed to the defect induced localized heating and consequent device degradation. If the graphene channel is prone to the severe defects, the localized heating near the defect causes the first failure. Increase in the TLP stress beyond this point will cause the graphene channel to degrade (no increase in the TLP current with increase in TLP voltage is observed). Increase in DC spot current during this stress range (after the first breakdown) confirms the device degradation near the defects induced failure.

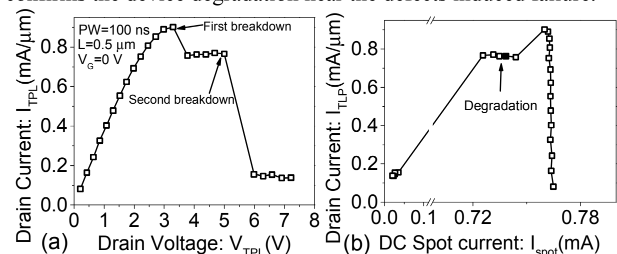

Fig. 2: (a) TLP I-V characteristics of short channel (L=0.5 μm) GFET device. (b) The corresponding DC spot measurement data. The device has shown unique two stage characteristic in both pulse I-V and spot data attributed to the defect induced localized heating and failure.

2) *Self heating effect on failure current in graphene*

Self-heating in graphene FET under ESD like stress conditions is not extensively discussed in the literature. In this work we use the transient voltage and current data for different stress durations with different power levels to understand the extent of self-heating and its implication on the device failure correlated with the carrier transport. Fig. 3(a) depicts the TLP IV characteristics of graphene transistors stressed with different pulse durations (25 ns-1500 ns). The following observations can be made. (a) Stressing with ultralow pulse widths (25 ns), the device current or failure current attain its maximum value, as the device self-heating is absent. (b) when

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increasing the pulse width, a saturating drain current characteristics are observed at sufficiently high fields (c) The onset of drain current saturation decreases with increasing pulse width. (d) The failure current scales down with increasing pulse width but the failure voltage almost remains constant. The observed drain current saturation in GFET at high enough fields, is attributed to the carrier scattering in the graphene channel with the substrate optical phonons. Though graphene has very large in plane thermal conductivity, the lower optical phonon energy of SiO_2 substrate (60 meV) dominates the optical phonon energy of graphene (180 meV). The substrate optical phonon modes cause the electron-phonon scattering in the graphene channel. As the pulse width increases electron phonon scattering increases, carrier mobility degrades

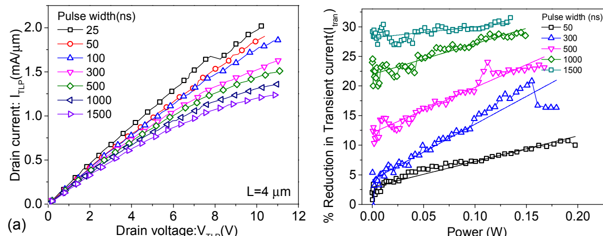

Fig.3: (a)TLP IV characteristics of back gated GFET stressed at different pulse duration ranging from 25 ns to 1500 ns (b) Percentage reduction in the transient drain current of plotted against the device power level.

Hence saturation in the drain current at sufficiently high fields, consequently reduction in the failure current. It's worth highlighting that device channel lengths used in this work are sufficiently large and are in the diffusive transport regime.

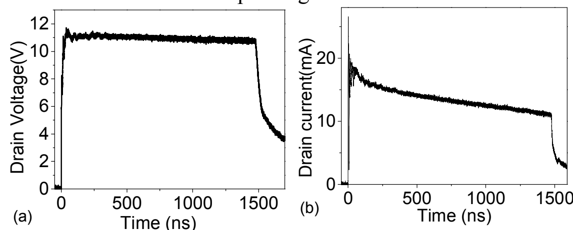

Fig.4. Transient (a) drain voltage and (b) corresponding drain current of graphene FET stressed under long pulse duration. The device channel length is 4 µm and width is 10 µm.

The severe substrate induced device self-heating can also be understand from the transient data presented in Fig. 4. At sufficiently high applied voltage, the transient current decreases with the time, a signature for self-heating. The degree of reduction in the transient current is a function of device power level and the stress duration. Fig.3(b) depicts the percentage reduction in the drain current as a function of stress duration and device power level. Increasing the device power causes more device heating, reduction in the drain current for a fixed pulse width. For a fixed power level, increasing the pulse width causes more electron-phonon scattering, Increase in device self-heating.

MULTIWALL CARBON NANOTUBES

The investigations carried in this work are single multi wall tubes with different lengths. Single multi wall tubes can either be resting on the substrate or can be suspended between the two electrodes depending on the length. When stresses under ESD conditions, both the inner shells and outer shells contribute to the current in multiwall CNTs, however during the low bias DC measurements the conduction only happens through the outermost shell. The spot measurements keep track of the outer most shell resistance.

Fig.5 depicts the TLP IV characteristics and the corresponding DC spot data of the substrate supported MWCNT with tube length of 1 µm are stressed with different pulse widths. It is found that (a) Under ultra-low pulse width conditions (25 ns) the device doesn't experience the exponential raise in the current before the onset of device failure. (b) The failure current and voltage scales with the increasing pulse width (c) The power law like characteristics can be observed in MCNTS. The exponential raise in MCNTS is because of the phonon assisted increased conduction channels and the increased band to band tunneling in the individual shells [12]. The missing exponential raise in the CNT current when stress under ultralow pulse width (25 ns) conditions is attributed to reduced phonon population from hot contact to the cold contact and hence no additional conduction channels formed during the ESD discharge. Increasing pulse width has shown the exponential raise clearly before the onset of device failure. The scaling of failure current and failure voltage and as a result the observed power law behavior is attributed to the thermal failure nature of the Carbon Nanotubes. Finally, the Scanning Electron Microscopic (SEM) images, after the ESD induced damages are presented in fig.6.

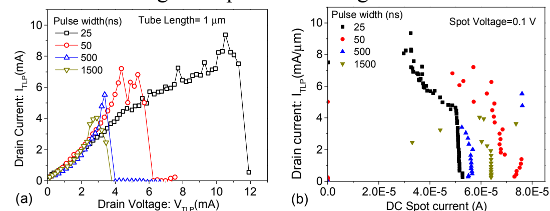

Fig.5 (a) The TLP IV characteristics of Multiwall Carbon nanotube with same tube length of 1 µm stressed with under different pulse durations. The observations are (i) The exponential increase in the tube current in the pre breakdown regime is absent under ultralow pulse widths. (ii) the failure current and failure voltage scales with increasing pulse duration and they follow power law like characteristics. (b) corresponding DC spot current data. The small variation in DC spot current for different devices is attributed to difference in the process induced charge surfactants in the outermost shell.

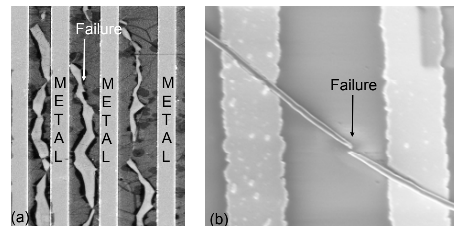

Fig .6. SEM image of (a) Graphene Channel with different channel length (b) CNT after the depicting the ESD induced damages.

CONCLUSION

A detailed physical insight into the ESD behavior of graphene transistors and CNT interconnects are presented. The unique two step failure in Graphene FETs, is because of the defect induced localized heating and further device degradation near the defects before the eventual failure. The self-heating in graphene devices studied through the transient analysis, found to reduce the drain current by almost 30%. The severe self-heating in graphene is attributed to the low energy substrate induced optical phonons scattering with the channel carriers. The reduction in the drain current because of self-heating is a function of pulse width and also the device power level. Finally, the investigations carried out on Multiwall CNTs have shown unique power law behavior which is attributed to the thermal failure nature of CNTs.

References: [1] Frank Schwierz, Nature Nano Technology, 2010. [2] G. Fiori, et.al, IEDM, 2012. [3] H. Li, et.al, TED,2014. [4] Q. Chen et al, TED,2016. [5] N. K. Kranthi, et.al, IRPS,2017. [6] M. Shrivastava, et.al, TDMR,2014. [7] M. Shrivastava, et.al, EOSESD,2014. [8] A. Mishra, et.al, IRPS,2016. [9] A. Mishra,et.al, EOSESD,2016 [10] Adil Meersha, et.al, IEDM, 2016.

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