FinFET SCR: Design Challenges and Novel Fin SCR Approaches for On-Chip ESD Protection

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Abstract – For the first time, physical insights into the missing SCR action in planar equivalent Fin SCR devices with the help of TCAD are presented, which has leveraged exploring challenges and fundamental roadblock in designing Fin SCRs. Key role of contact silicidation in Fin technology is discovered. The new understanding has allowed engineering conventional designs to resume SCR action. Finally, a novel Fin SCR design is disclosed, which offers an area efficient current conduction beside device scalability.

I. Introduction

Silicon Controlled Rectifier (SCR) based concepts have consistently offered efficient ESD protection solutions for several generations of planar Si technology, which is attributed to its lower parasitic capacitance and relatively smaller design footprint, lower holding voltage and faster turn-on when compared to other ESD device options [1] – [4]. Unlike planar, FinFET technology is still far away from getting the benefit offered by SCR-based ESD concepts due to unavailability of robust or planar equivalent Fin-based SCR devices [5]. ESD device design challenges and unavailability of ESD robust devices in FinFET technology makes FinFET and beyond FinFET technologies further susceptible to ESD events when compared to their planar counterparts [6] – [9]. In this work, for the first time, the challenges and fundamental roadblock in designing Fin SCRs are revealed. Using the new physical insights developed with the help of TCAD, this work demonstrates engineering approaches for conventional Fin SCR as well as discloses a novel Dual Fin SCR (DFSCR) device for efficient ESD behavior. The DFSCR device is structurally designed to offer an area efficient current conduction.

II. Overview of FinFET SCRs

SCR as an ESD protection element offers an excellent ON resistance with high failure current (It2) and low holding voltage (V_{Hold}). However, transfer of planar SCR design to FinFET technology, with a conventional approach has altered the indigenous ESD relevant metrics of the SCR, such as snapback, desirable It2, low V_{Hold} and ON resistance. Fig. 1(a) shows a planar equivalent Conventional Fin SCR (CFSCR) were the N+ or P+ Fins are by default fully silicided at the fin surface (and are termed like this throughout the paper). These Fins are used to contact N/P-Wells (base/collector taps) or form junctions with the same (emitter). In all investigations, number of fins used in N/P-tap region is 0.6N, where N

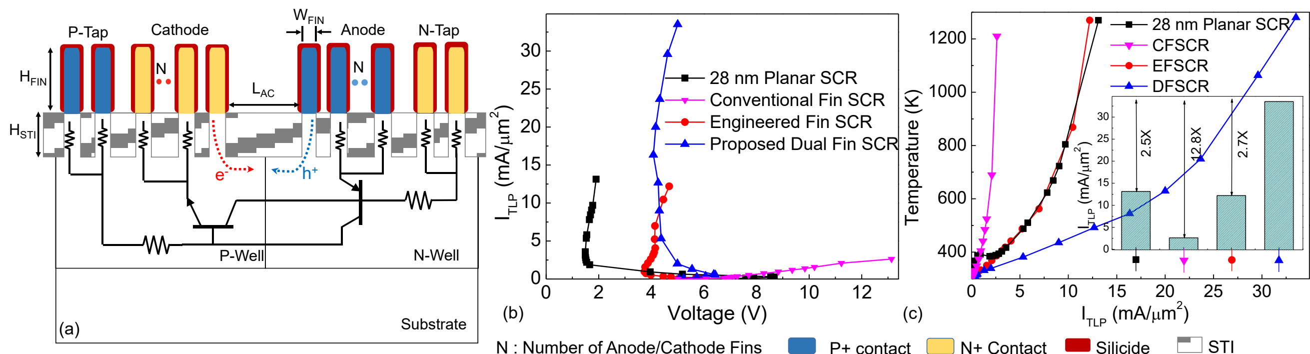

Figure 1: (a) Planar equivalent of Conventional Fin SCR (CFSCR). Here N is number of Anode/Cathode Fins. (b) TLP I-V characteristics of CFSCR, Engineered Fin SCR (EFSCR) and proposed DFSCR, extracted using 3D TCAD simulations. (c) Lattice temperature vs. TLP stress current of CFSCR, EFSCR and proposed DFSCR, extracted using 3D TCAD simulations. Inset of Figure (c) depicts significantly improved ESD robustness (It2) of the proposed DFSCR and EFSCR, which are ~13× and 5× higher than CFSCR, respectively.

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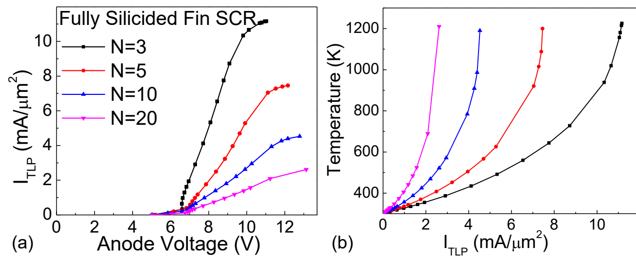

Figure 2: (a) TLP I-V characteristics and (b) Lattice temperature vs. TLP stress current characteristics of fully silicided Conventional Fin SCR (CFSCR) as a function of number of Anode/Cathode Fins (N).

represents the number of anode/cathode fins. Its TLP characteristics, as depicted in Fig. 1(b), reveals absence of SCR action, which is evident from missing snapback action, lower It2 and very high holding voltage. Note that the stress current is normalized with the unit layout area, in order to bring the fair comparison between 2D (Planar) and 3D nature of the various SCR designs. Physical insights into the missing SCR action are given in the next section, which allowed engineering conventional design to enable SCR action and leverage 28nm planar equivalent It2, as depicted in Fig. 1(b). Fig. 1(b) – (c) further depict TLP characteristics of proposed DFSCR, which offers ~13× improvement in ESD robustness when compared to CFSCR and ~3× improvement than Engineered Fin SCR. For 3D TCAD simulations, thermal boundary conditions were adopted from [4]. To encapsulate the heat dissipation mechanism inside and around the FinFET SCR, thermal resistance is added in order to mimic metal interconnect and interlayer dielectric thermal boundaries. TLP I-V characteristics were extracted using a TLP like setup with 100ns wide pulses. Pulse rise time was 10ns in all the cases. Devices were considered to fail at 1200K in accordance with an earlier failure analysis work on FinFETs [6] and considering a conservative estimate. For all investigations, H_{FIN}, H_{STI} and W_{FIN} was considered to be 42nm, 70nm, and 8nm respectively. The design challenges, proposed engineering approaches, physics

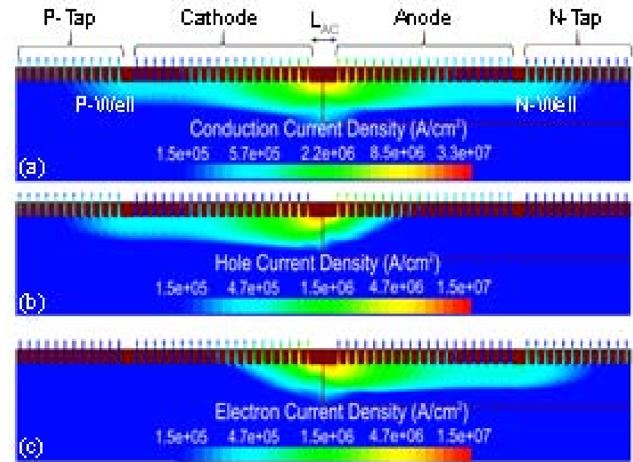

Figure 3: (a) Total, (b) Hole and (c) Electron current density across a fully silicided conventional Fin SCR extracted at 50% of It2.

of operation, design methodology and relative comparisons of the CFSCR, Engineered Fin SCR (EFSCR) and proposed DFSCR are presented in the subsequent sections.

III. Fin SCR Design Challenges & Engineering

In order to design efficient ESD SCR devices in FinFET technology it becomes imperative to address the root cause of the missing SCR action in conventional Fin SCR (CFSCR), as depicted in Fig. 1(b), which is further elaborated in Fig. 2 as a function of number of Anode/Cathode Fins (N). Fig. 2 shows that increasing N lowers It2 per unit area and doesn't affect the SCR action. An obvious reason for the missing SCR action is weak parasitic bipolar, which can possibly be attributed to an increased emitter resistance due to Fin shape or increased carrier recombination in the base region due to relatively higher doping in FinFET N/P-Wells. However, we found that none of these were responsible for a weaker bipolar action, which is discussed in Fig. 3-5. Fig. 3(a) shows majority of current to flow between Anode and Cathode terminals, which is in line with

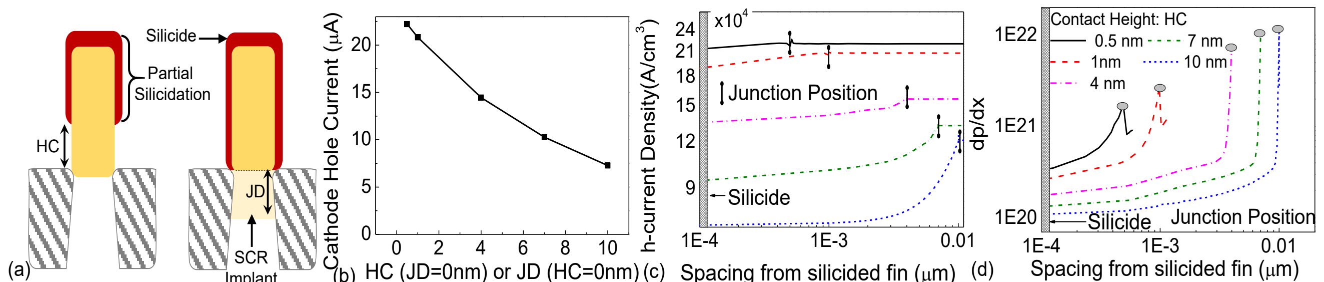

Figure 4: (a) Fin schematic depicting schemes for increasing spacing between fully silicided Fin region and base emitter junction. Conventional Fin has HC=JD=0nm (see Figure 1a). (b) Cathode Hole current vs. HC, JD. (c) Hole current density and (d) Hole density gradient (dp/dx) as a function of spacing between contact and base-emitter junction.

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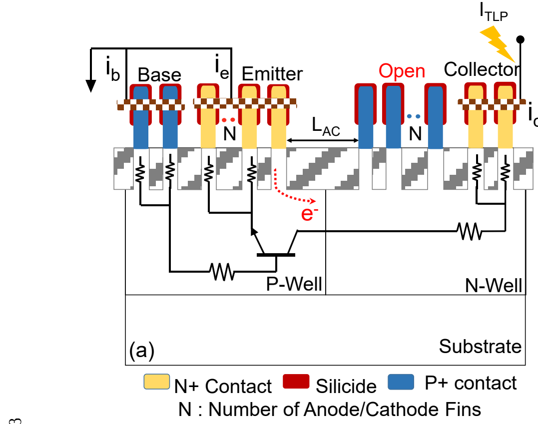

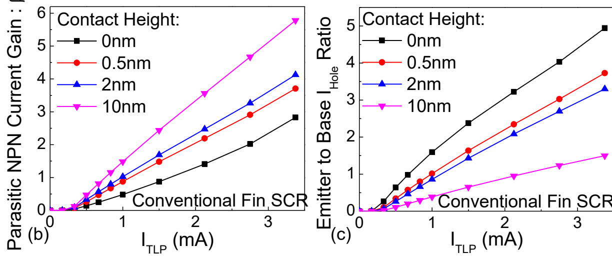

Figure 5: (a) Cross sectional view of the planar equivalent Fin SCR depicting parasitic NPN device. (b) Current gain (β) as a function of injected collector current. (c) Emitter to Base Hole current ratio as a function of pulsed collector current.

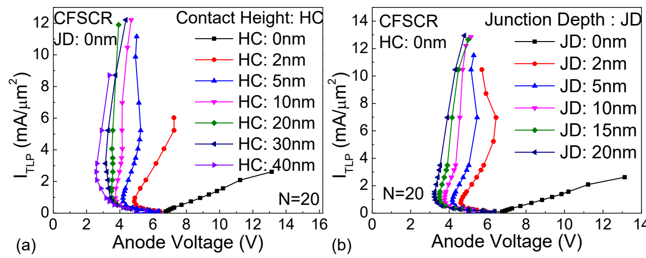

Figure 6: TLP I-V characteristics of planar equivalent Fin SCR with varying (a) HC (JD=0) and (b) JD (HC=0). Here N=20.

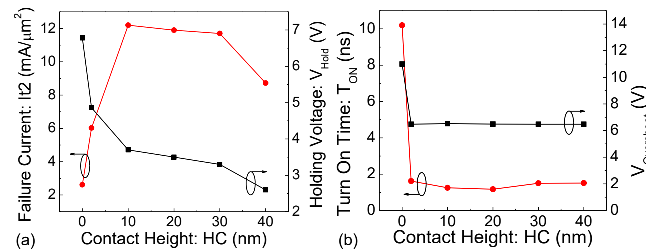

Figure 7: Failure current (It2), holding voltage (V_{Hold}), turn-on time (T_{ON}) and voltage overshoot ($V_{Overshoot}$) as a function of spacing between contact silicidation and base-emitter junction (HC) for JD=0nm. The trends were extracted at injected stress current equivalent to 90% of the respective It2.

conventional understanding of current transport across SCR device [2]. However, unlike minority carrier conduction in planar SCRs, in fully silicided Fin SCR we found significant amount of minority carrier

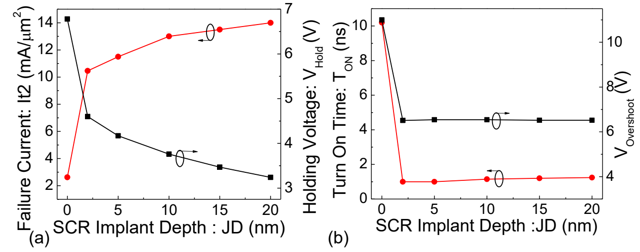

Figure 8: Failure current (It2), holding voltage (V_{Hold}), turn-on time (T_{ON}) and voltage overshoot ($V_{Overshoot}$) as a function of diffusion depth below active Fin (JD) for HC=0nm. The trends were extracted at injected stress current equivalent to 90% of the respective It2.

conduction through respective Cathode/Anode i.e. emitter contacts of Fin SCR (Fig. 3b & c). This minority hole (electron) conduction through the parasitic NPN (PNP) emitter contact, is expected to dominate through P (N)-Tap to trigger the SCR. This explains weaker bipolar action due to a significant loss of minority carriers through the emitter contacts. We found that high minority carrier conduction through emitter contacts is due to fully silicided nature of Fins, which is elaborated in Fig. 4. Fig. 4(a) shows single Fin schematic depicting parameters HC or JD to study impact of spacing between silicided portion of the Fin and base-emitter junction. In case of conventional (fully silicided) Fin SCR, HC=0 & JD=0, Fig. 4(b) shows gradual reduction in minority carrier conduction through the emitter contact as HC was increased from 0 to 10nm (JD=0). Same trends where found when JD was increased from 0 to 10nm for HC=0. This is attributed to minority carrier diffusion current (Fig. 4c) which strongly depends on minority carrier gradient between junction and the contact ($J_p = q.D_p.dp/dx$). Theoretically, for HC=JD=0, $dx \rightarrow 0$ and hence $dp/dx \rightarrow \infty$. Extrapolating this to situation when contact was placed next to the vertical junction in case of fully silicided Fin, it resulted in significantly higher carrier gradient (Fig. 4d) and minority carrier conduction through emitter (Anode/Cathode) contacts. When the same was relaxed by pushing silicided region away from the junction, either by increasing HC or increasing JD, parasitic bipolar action within Fin SCR was improved, as depicted in Fig. 5. Similar improvement in bipolar efficiency for planar nMOS devices was earlier experimentally validated with thin S/D salicides [10]. The efficiency of the parasitic bipolar in this study was studied using the scheme shown in Fig. 5(a). As the spacing between silicided portion of the Fin and base-emitter junction was increased, bipolar gain (β) was found to increase (Fig. 5b), which is attributed to reduced emitter to base hole current ratio (Fig. 5c). This has resulted in an efficient

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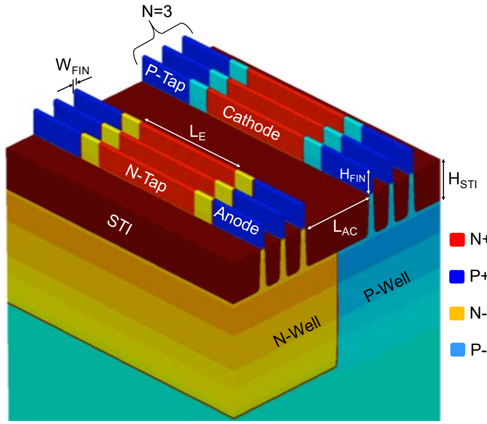

Figure 9: 3D view of proposed Dual Fin SCR design. The active portions of the Fin consist of Anode/Cathode and N/P-Taps, which forms a junction or contact with N/P-Wells. It's worth highlighting that Anode and Cathode diffusions are intentionally placed diagonal to each other. This has resulted in uniform current spreading which leads to lower current density for a given absolute current and therefore relaxes heat dissipation across the device.

SCR action with deeper snapback, as depicted in Fig. 6. An SCR action is clearly visible for HC > 2nm or JD > 2nm. Fig. 7 and 8 further depict impact of contact spacing, by increasing HC and JD respectively, on the ESD figure of merit parameters of SCR device. As HC or JD was increased, SCR's failure current and turn-on time was found to improve by an order of magnitude. Similarly holding voltage and voltage overshoot was found to scale by a factor of 3 and 2 respectively (V_{Hold} drops from 7 to 3V and $V_{Overshoot}$ drops from 11 to 6.5V in Figure 8). HC=10nm (for JD=0nm) and JD=10nm (for HC=0nm) were found to offer optimum performance for EFSCR, which are used in subsequent investigations.

IV. Novel Dual Fin SCR (DFSCR)

Fig. 9 depicts the proposed Dual Fin SCR (DFSCR) design. Here Anode and Cathode diffusions are intentionally placed diagonal to each other. This has

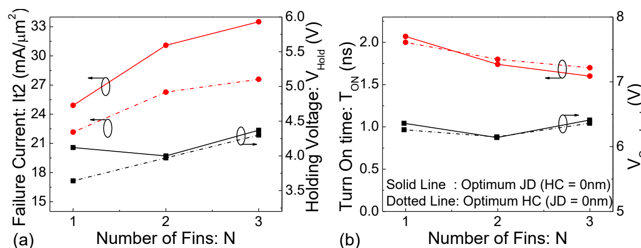

Figure 10: Failure current (It2), holding voltage (V_{Hold}), turn-on time (T_{ON}) and voltage overshoot ($V_{Overshoot}$) as a function of number of Fins (N) over N/P-Well in DFSCR. The trends were extracted using 3D TCAD simulation setup, at injected stress current equivalent to 90% of the respective It2.

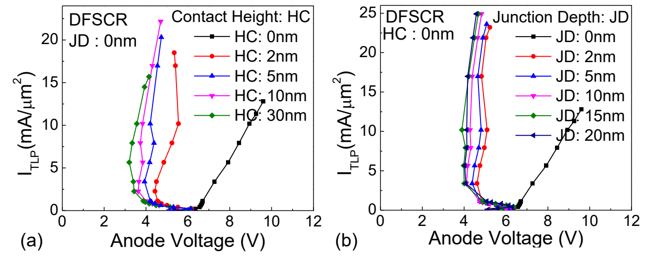

Figure 11: TLP I-V characteristics of DFSCR with varying (a) HC (JD=0) and (b) JD (HC=0). Here N=1.

allowed uniform current spreading and therefore lower current density for a given absolute Anode-to-Cathode current, which eventually relaxes the heat dissipation across the device and improves failure current per unit area (Fig. 1). The proposed DFSCR device can easily be used in cell based geometry to minimize its overall footprint.

The proposed design consists of two groups of Fins separately placed in N-well and P-well. Here each

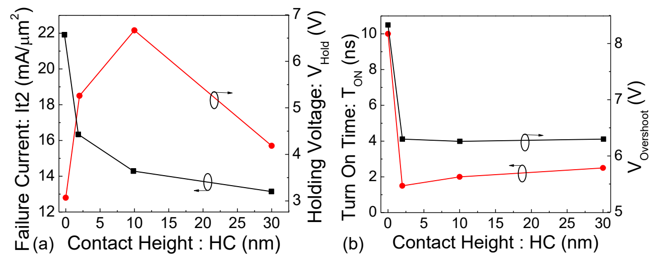

Figure 12: Failure current (It2), holding voltage (V_{Hold}), turn-on time (T_{ON}) and voltage overshoot ($V_{Overshoot}$) as a function of HC in DFSCR.

group may have one or more number of Fins (N). N/P-Taps are placed on both the sides of Anode/Cathode. Fig. 10 shows that increasing number of Fins in given group improves the area efficiency of the device without sacrificing the turn-on or holding voltage characteristics. Compared to optimum EFSCR (Fig. 7 & 8), the proposed device offers 3× higher It2 per unit area. Similar to EFSCR, Fig. 11 – 13 depicts the 3D TCAD analysis of the proposed DFSCR, which clearly shows improved SCR action when HC and JD were increased above 2nm. This validates the design challenges and proposed solutions in the previous section.

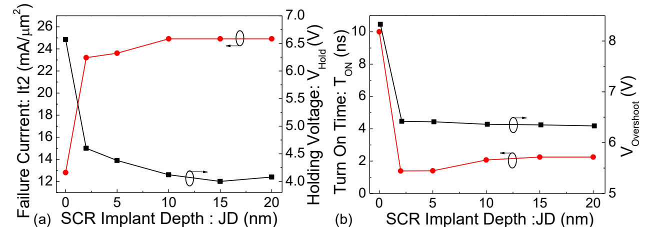

Figure 13: Failure current (It2), holding voltage (V_{Hold}), turn-on time (T_{ON}) and voltage overshoot ($V_{Overshoot}$) as a function of JD in DFSCR.

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Interestingly, unlike EFSCR, DFSCR with optimum JD exhibits higher failure threshold than the same with optimum HC, which validates presence of efficient current spreading in the proposed device compared to planar equivalent design. Scalability of the proposed DFSCR is present in Fig. 14. Fig. 14(a) shows 20% improvement in failure current per unit area when Anode/Cathode diffusion length (L_E) was increased by 4×. This can be achieved without sacrificing transient performance as depicted in Fig. 14(c). By scaling Anode to Cathode spacing (L_{AC}) by ~4×, It2 per unit area was found to improve by 3× with 25% reduction in holding voltage, 25% reduction in voltage overshoot and 2× faster turn-on. This was found to achieve without sacrificing OFF state leakage. Similar level of design scalability was missing in the conventional designs. Finally, Fig. 15b compares transient performance of EFSCR and DFSCR as a function of pulse rise time. Here, the turn-on time (T_{ON}) is extracted as the time when the voltage achieves a minimum holding state (Fig. 15a). Attributed to smaller design foot print (lower capacitance) and improved current spreading characteristics, DFSCR offers lower voltage overshoot at shorter rise times (tr < 2ns, emulating the vf-TLP conditions), without compromising with turn-on time, when compared to EFSCR. Similar trends were observed for optimum HC design too. This concludes an area efficient ESD robustness of DFSCR when compared to EFSCR.

V. Summary and Conclusion

We revealed missing SCR action in planar equivalent conventional Fin SCR devices. Minority carrier conduction through the Anode/cathode contacts was found to be the root cause of weak parasitic bipolar and missing SCR action in conventional Fin SCR device. This was found to be due to fully silicided

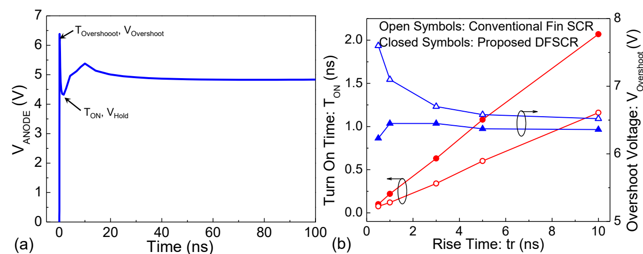

Figure 15: (a) Typical transient characteristics of DFSCR, depicting the extraction of T_{ON}, (b) Transient figure of merit comparison of engineered Fin SCR and DFSCR as a function of pulse rise time, extracted for optimum JD. The characteristics remain the same for optimum HC too. The trends were extracted using 3D TCAD simulation setup, at injected stress current equivalent to 90% of the respective It2.

nature of the Fins, which give rise to minority carrier diffusion current through parasitic bipolar's emitter-base junction. This was avoided (i) by pushing the silicided region away from the junction by introducing partial silicidation or (ii) by pushing the junction away from the silicided portion by introducing an SCR implant. This has resumed the SCR action with significantly improved performance. Finally, the novel Dual Fin SCR (DFSCR) design is proposed, which allows uniform current spreading, scalability and relaxed heat dissipation across the device. Attributed to this proposed design offers 3× higher failure current per unit area, 35% lower voltage overshoot without compromising with turn-on time, when compared to engineered Fin SCR device.

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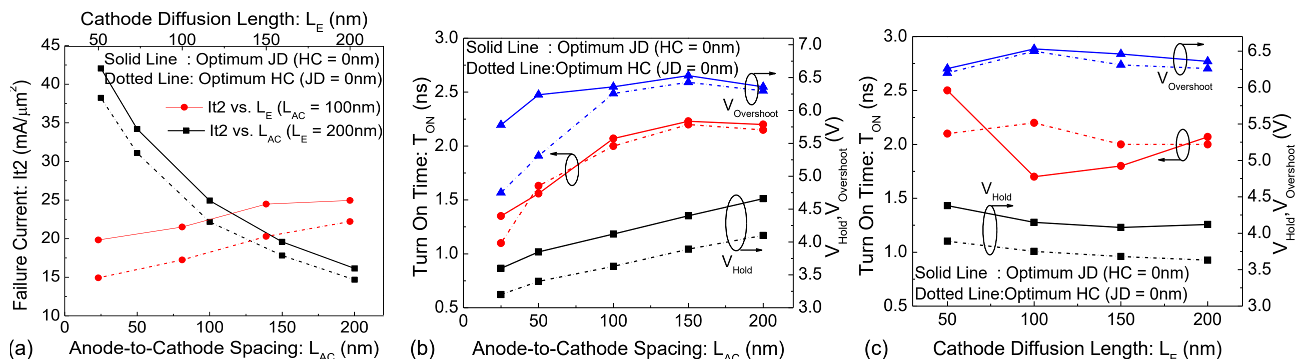

Figure 14: Design scalability of proposed DFSCR. Failure current (It2), holding voltage (V_{Hold}), turn-on time (T_{ON}) and voltage overshoot ($V_{Overshoot}$) as a function of Anode-to-Cathode spacing (L_{AC}) and Anode/Cathode diffusion length (L_E). The trends were extracted using 3D TCAD simulation setup, at injected stress current equivalent to 90% of the respective It2.

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