On the ESD Behavior of Pentacene Channel Organic Thin Film Transistors

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Abstract - Detailed physical insight into the ESD behavior and unique failure mechanisms of Pentacene Organic Thin Film Transistors (OTFTs) is reported. Orders of magnitude difference in channel current under ESD time scales, when compared to DC time scales, is discovered. Moreover, unique three stage TLP characteristics with snapback state and novel failure mechanism are reported. Finally, influence of channel field and Surface Assembled Monolayer (SAM) on the carrier transport and failure threshold is addressed.

I. Introduction

Organic electronics is offering new possibilities to the field of electronics. Although, inorganic semiconductors offer high performance, there are several technologies that can only be realized using organic materials. For example, flexible electronics [1] and low cost biomedical sensors [2], which require low cost, low temperature fabrication processes. Among various organic semiconductor options, Pentacene channel offers significantly better Organic Thin Film Transistor (OTFT) performance, with a mobility exceeding 1 $cm^2V^{-1}s^{-1}$ and an ON/OFF ratio of about 10^8 [3], which is on par with the best performing a-Si:H TFTs. With the advancement of organic electronics from a purely academic interest into industrial development, it is important to understand the reliability aspects of these transistors. While studies have been conducted to understand the long term reliability of these transistors [4]-[5], their behavior against ESD stress has not been completely explored [6]. This paper provides detailed physical insight into carrier transport and unique failure mechanism under ESD conditions, while keeping the technological implications in mind.

II. Device Fabrication and Characterization

Fig.1 depicts the 2D cross-section view of the fabricated Pentacene OTFT and the device fabrication process flow followed in this work. A high performance Pentacene OTFT with a bottom gate top contact structure was used in this work having a having a threshold voltage amplitude >10V and ON/OFF ratio >10^5. This performance is comparable to other Pentacene based OTFTs reported in the literature [3], [7]. A highly doped P-type Si wafer was used as a substrate. A 90nm thick SiO_2 layer was then grown thermally over the substrate to act as the gate insulator.

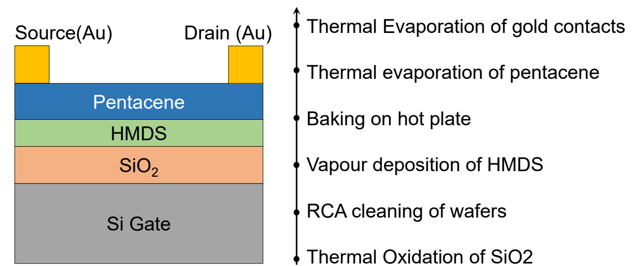

Fig. 1: 2D cross-sectional view of Pentacene based OTFTs along with the device fabrication process flow. HMDS was introduced to passivate the Si-OH traps at the oxide-Pentacene interface.

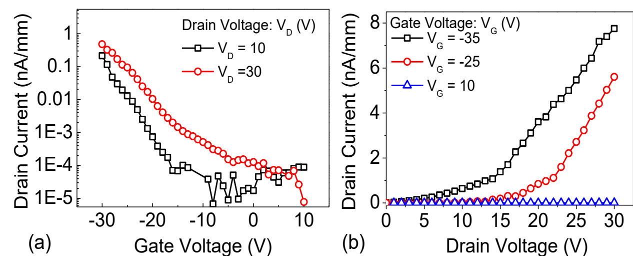

Fig. 2: DC I-V characteristics of Pentacene based OTFT (a) I_D-V_G characteristics and (b) I_D-V_D characteristics. This confirms the transistor action. Please note that the device is not in the saturation region at these voltage levels.

Optionally Hexamethyldisilazane (HMDS), acting as a self-assembled monolayer (SAM) was vapor deposited in a desiccator under vacuum for a period of 20 min and then baked on a hot-plate at 383 K. HMDS layer prevents the adsorption of water at Pentacene- SiO_2

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interface. The presence of water molecules at the interface depletes charge carriers and increases the effect of negative gate bias stress [8].Pentacene ($C_{22}H_{14}$) was then thermally evaporated at a pressure of about $3x10^{-8}$ bar using commercially available Pentacene to obtain an active/channel layer 80 nm thick. 100nm thick Gold contacts were thermally evaporated as Source/Drain (S/D) contacts. The ESD investigations were performed using a 50Ω TLP setup.

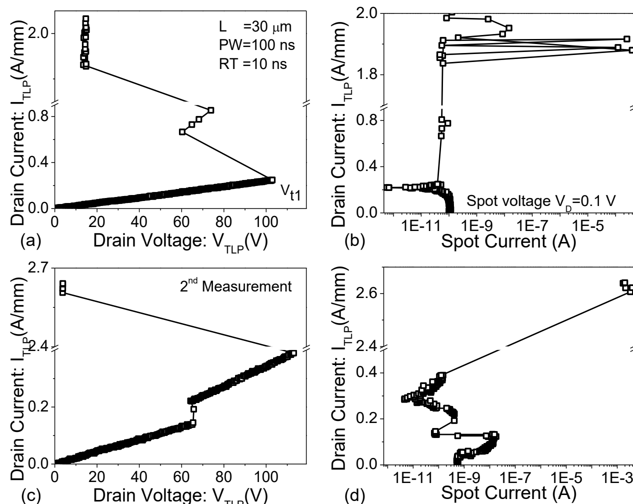

Fig. 3: (a) TLP I-V characteristics of Pentacene based OTFT. The device shows a low resistance snapback, due to diode turn on and subsequently a low voltage holding state. (b) DC spot current. (c) & (d) TLP I-V characteristics of the same device, post failure, at a different location on contact pads, which show pristine like TLP I-V characteristics.

A current sensor with a sensitivity of 0.5mV/mA and a 4 GHz Oscilloscope are used to capture waveforms. The setup was calibrated using a standard surface mount resistor and a zener diode. Unless stated otherwise, devices with a channel length of 30µm, channel width of 1mm, pulse width (PW) of 100ns and a rise time (RT) of 10ns is used for all the measurements. To study failure, a low DC bias of 0.1V is applied after each pulse and drain current was monitored.

III. ESD Behavior of OTFTs

Pentacene OTFT is stressed under ESD conditions in a grounded gate configuration. The TLP I-V characteristics, as depicted in Fig. 3, shows a three state behavior i.e. sub-threshold state, low on-resistance state and holding state.

A. Carrier Transport in Sub-threshold Region

In the off state, TLP I-V follows linear characteristics with high on-resistance until it experiences device turn-on, i.e. first snapback (V_{t1}). Post first snapback, the device sees a low on-resistance state. It is worth highlighting that the channel current at nanosecond time scales is orders of magnitude higher than the same observed under DC conditions at the same voltage levels. Moreover, it was observed that the channel current (Fig. 3b) reduces with increasing stress level. It is also observed from Fig. 4b that during the stress pulse, the current reduction takes place. To explore this, the fractional change in resistance from ambient value, the device temperature and temperature variation during the sub-threshold region is studied. The power dissipated during a stress pulse causes the temperature to increase which causes the device resistance variation given by equation

$$R(T) = R(T_{amb})\,[1+\alpha\,[T-T_{amb}]] \qquad (1)$$

where α is the thermal coefficient of resistance. T_{amb} is the ambient temperature and T is the temperature of device [9]. The quantity α is measured by variation of resistance as the device is heated using a thermal chuck. The device resistance at the start of the stress pulse is taken as $R(T_{amb})$. It is observed from Fig. 4c that the device resistance increases during the pulse. This increase in resistance is caused due to an increase in temperature (Fig. 5) due to self-heating in organic semiconductors. As the temperature increases, the effective mass of charge carriers in Pentacene increases exponentially which, when coupled with the narrowing of valence band width, causes mobility degradation [10]. Above 300K, the thermal conductivity in Pentacene decreases with temperature [11] due to increased scattering of charge carriers with optical phonons,

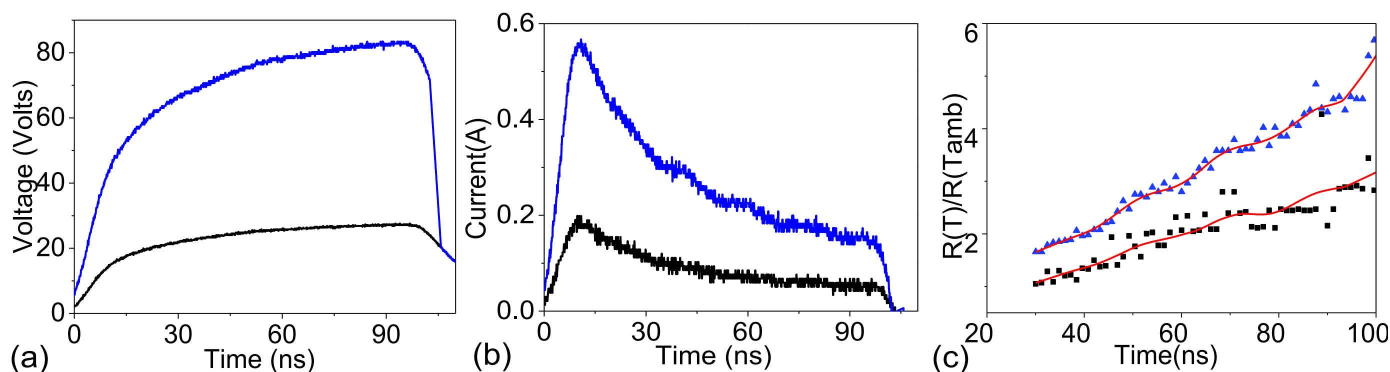

Fig. 4 (a) Voltage across device versus the time (b) Device current versus time. (c) The fractional change in resistance during the stress pulse. The voltage pulses were applied using a 50Ω TLP setup. Calibration was done so as to ensure that the measured resistance is device resistance.

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leading to a decreased mobility. This leads to a degradation of charge transport in Pentacene with increasing stress and temperature. The effective mass of charge carriers at a temperature T is given by the expression

$$m_{eff} = m_o \exp(T/T_o) \qquad (2)$$

where, for Pentacene in c' crystallographic direction is To is 77K and m_o is 18.7 times the electron rest mass for vacuum sublimed films [10]. It is also observed from Fig. 5 that the maximum temperature achieved during a pulse increases with the voltage stress. It is worth highlighting that the maximum temperature observed does not damage the device and resistance increase is reversible.

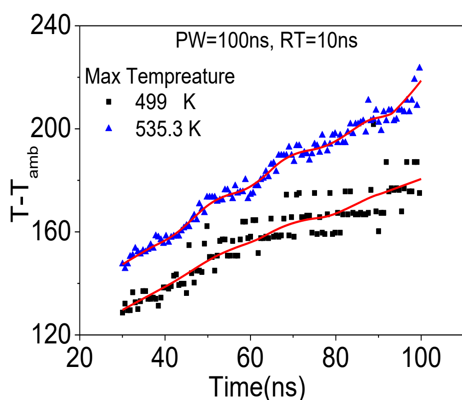


Fig. 5: The change in temperature during the stress pulse. The temperature was measured after 30ns so that the voltage reaches a steady state value and current overshoots do not lead to faulty results.

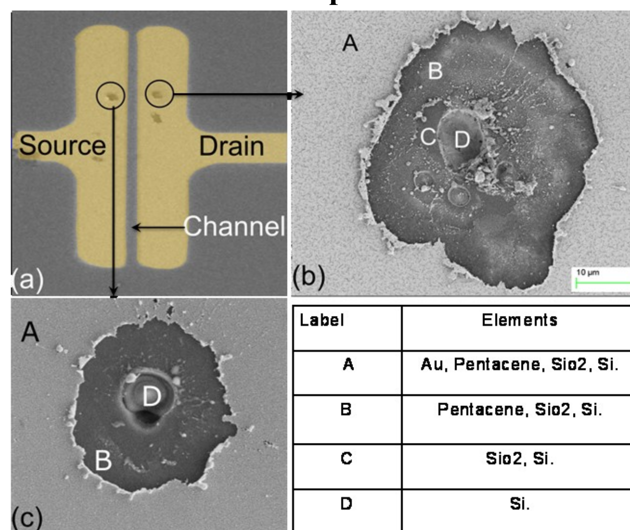
B. Impact of Pulse Width

To understand the orders of magnitude difference in TLP vs. DC current, as highlighted above, pulse widths ranging from 25ns - 1000ns were applied to explore device behavior as a function of stress time. The following observations can be made from TLP I-V characteristics (Fig. 6): (i) With an increase in pulse width, the device on-resistance increases and (ii) an early channel current degradation with increasing pulse width, which signifies accumulative nature of degradation.

C. Device Turn-On

Gold and Pentacene form a Schottky contact at the metal–semiconductor interface which impedes the hole injection from Gold, leading to a higher on-resistance at low stress levels. However, it is observed that (Fig. 3), the devices experience a voltage snap back and move into a low on-resistance state as the stress level increases beyond V_{t1}, without a corresponding change in the DC spot (channel) current. The snapback state seen in Pentacene OTFT's is attributed to a reduction of the Schottky barrier height at the interface causing a higher tunneling probability of Holes into the channel. This leads to excess carriers entering the semiconductor, which eventually leads to device turn-on and deep snapback.

D. Catastrophic Failure



Label	Elements
A	Au, Pentacene, Sio2, Si.
B	Pentacene, Sio2, Si.
C	Sio2, Si.
D	Si.

Fig. 7: (a) False color SEM image of Pentancene OTFT (Top view). (b) & (c) Zoomed SEM view of the damaged sites. Formation of a current path from Si substrate takes place inside SiO_2 due to the longitudinal field causing high current. Peeling off of various layers takes place due to current crowding at the contact region. Table concludes EDAX results extracted at various regions.

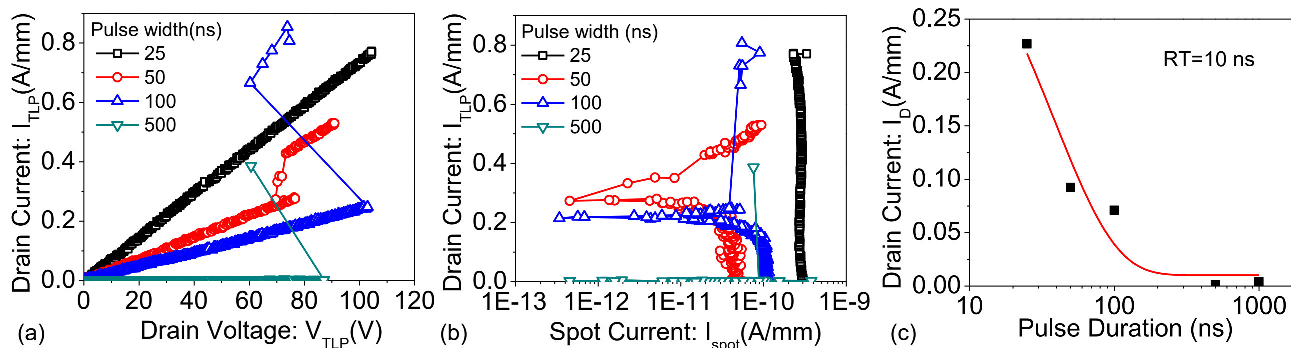


Fig 6: (a) TLP I-V characteristics of Pentacene based OTFT's stressed using pulses with different pulse times. (b) DC spot characteristics. Higher Pulse width contributes to higher ON-Resistance attributed to higher self-heating. (c) The Drain current showing a power law behavior with respect to the pulse width.

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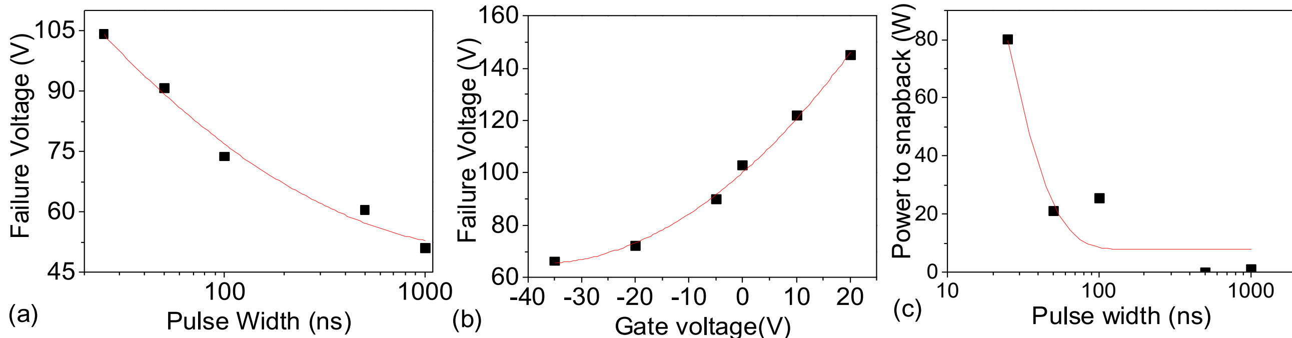

Fig. 8 (a) Failure voltage with pulse width. The failure voltage reduces with pulse width as stress timing is increased (b) Failure voltage with gate voltage. Failure voltage reduces as gate voltage becomes more negative. (c) Power to snapback with Pulse Width following an exponential decay function.

Further increasing the stress, post device turn-on, causes the device to experience a holding state and eventual failure (Fig. 3), resulting in an abrupt increase in the leakage current seen in DC spot measurement (Fig. 3b). The damage is observed to take place under both the source as well as drain pads, hence the failure is not just a result of electrical overstress between gate and drain or thermal failure, which is expected to happen only near drain. Failure under both pads signifies a field as well as current driven phenomenon. Failure analysis reveals dielectric breakdown under the source and drain pads, exposing the Si substrate below (Fig. 6).The failure occurs at localized points in the device. The high current also leads to burnout of contact pads due to current crowding (Fig. 7). The device in Fig. 3 reveals a failure current of 0.8A/mm. It must be highlighted that the Pentacene channel was found to be quite robust and no damage was observed in the channel, instead damage takes place under the gold contacts. This observation can pave the way for usage of Pentacene as a channel material for ESD robust TFTs. Fig. 8(a) shows the variation of failure voltage with pulse width and gate voltage respectively. The dielectric breakdown has a thermodynamic time constant which leads to an increase in the probability of failure due to increased stress, leading to a reduction in failure voltage. Fig 8(b) plots the failure voltage versus gate bias due to a change in vertical field i.e. field between contacts and the bottom gate. Fig. 8(c) plots snapback power versus pulse width. When stress is applied for longer time, increased number of charge carriers is injected resulting in a lower snapback voltage.

E. Gate Field Dependency

The influence of Gate field on the ESD behavior and failure thresholds of Pentacene OTFTs is explored by biasing the gate in different regions of transistor operation. It is observed that (Fig. 8(b)), as the gate bias varies from sub-threshold to saturation region, an early device turn-on and device failure takes place. Lowering of V_{t1} (Fig. 9a) is attributed to the reduction of tunneling distance for the carriers in the Drain reservoir into the channel. Whereas, failure threshold under higher negative gate bias is reduced due to increase in the field across the dielectric.

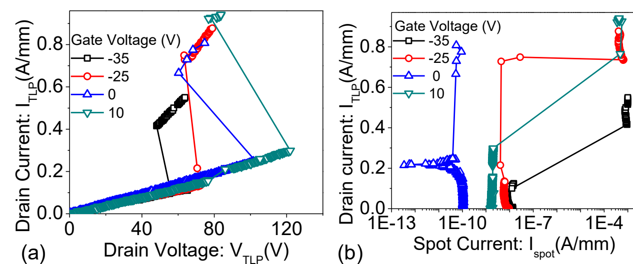

Fig. 9: (a) TLP I-V characteristics and (b) DC spot characteristics showing variation in turn-on and failure voltage with gate bias. The change in the failure voltage with gate bias is consistent with the proposal of field driven dielectric breakdown.

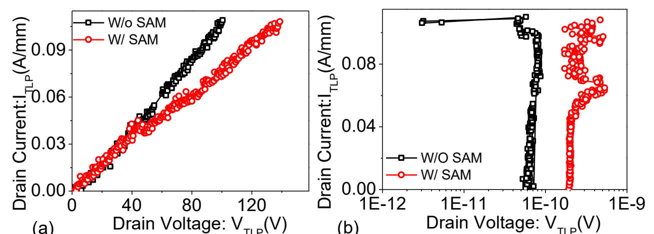

Fig 10 (a) TLP I-V characteristics and (b) spot measurements of devices with and without SAM layer. Device with SAM layers fails at a relatively higher voltage, which is attributed to increase in thickness of dielectric and passivization of interface traps.

IV. Technology and Design Implications

A. Effect of SAM layer

Coating surface assembled monolayer (SAM) over dielectric prior to semiconductor deposition offers multiple advantages, one of these being passivation of Si-OH traps at the dielectric-semiconductor interface [8]. This improves the charge transport in organic semiconductors and offers better electrical characteristics. For this reason, SAM coating has become an important part of OTFT fabrication [8]. Fig.

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10 shows the effect of surface assembled monolayer coating on the ESD robustness of the OTFTs. The devices with SAM coating are found to offer better ESD performance than the ones without SAM coating. This is due to increase in thickness of dielectric, with SAM layer also acting as a dielectric. There is also a reduction of trap states which assist in oxide breakdown. It is observed from Fig. 9 that the device with SAM carries lower current as compared to one without the SAM layer even though it carries higher DC spot current. This can be attributed to the presence of fast traps present on HMDS treated SiO_2 other than SiOH traps, which are passivized by SAM coating [12].

B. Channel Length Variation

Devices with different channel lengths were tested (Fig. 11). With increasing channel length, the on–resistance of the device was found to come does, however, systematic trends in terms of failure threshold were missing which could be attributed to device to device variation.

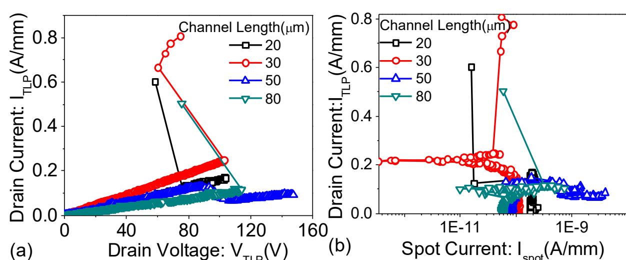

Fig. 11: (a) TLP I-V characteristics of Pentacene based OTFT's with varying channel lengths. (b) DC spot characteristics. Larger channel length contributes to higher ON-Resistance. The variation in failure voltage is due to device to device variations.

V. Conclusion

Detailed physical insight into the carrier transport of Pentacene OTFTs under ESD conditions has been presented for the first time. Orders of magnitude difference in the channel current under ESD conditions, when compared to DC condition is discovered. This was attributed to the self-heating induced degradation of charge transport. During nanosecond stress pulses, heating is localized and heat diffuses to surrounding material. The extremely high channel current reveals the robustness of Pentacene as a channel material against the ESD stress. Pentacene OFETs devices under ESD stress conditions were found 3 stage characteristics, i.e. sub-threshold conduction, snapback/holding state and device failure. Voltage snapback was attributed to the turn-on of metal – semiconductor Schottky diodes at high-stress levels, which drives the devices into a low on-resistance state. Unique field driven defect induced failure via pinhole formation under both source & drain contact pads was observed in Pentacene channel devices. Further, turning on the channel view gate field was found to lower the failure threshold by influencing the barrier height and field in the Source/Drain Schottky diodes. Finally, the introduction of SAM layer was found to enhance the ESD robustness of these transistors, by passivation of the interface trap states.

VI. Acknowledgement

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