Physics of Current Filamentation in ggNMOS Revisited: Was Our Understanding Scientifically Complete?

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Abstract—**Serious flaws in conventional understanding related to current filamentation and failure in ggNMOS is addressed. The conventional theory is revisited with new physical insights toward current filamentation. Filament dynamics under electrical and thermal instabilities is discussed while correlating it with stress time and current, silicide blocking and S/D doping.**

Keywords- Electrostatic Discharge (ESD), ggNMOS, filamentation, electrical and thermal instability, silicide blocking.

I. INTRODUCTION

Electrostatic Discharge (ESD) reliability and the silicon real estate required for ESD protection are growing concerns, which directly affect the tremendous pace required for CMOS scaling and integration [1]. Silicide blocked grounded-gate NMOS (ggNMOS) based ESD protection concepts are well established in advanced CMOS nodes with its potential extension to FinFETs [2]. In advanced CMOS nodes silicided devices suffered from filamentation and early failure, which was conventionally attributed to non-uniform parasitic bipolar turn-on [3] [4]. The non-uniform turn-on is believed to be suppressed by introducing silicide blocking in the drain and source region. Silicide blocking has consistently shown significant improvement in failure currents (It2) for a number of CMOS nodes [5] - [6]. A current ballasting theory is often discussed to support It2 increase with silicide blocking length (DOP). It is believed that the added S/D resistance, due to silicide blocking, helps in ballasting current across the device width. However, this theory was never supported by extensive 3D TCAD results, except some preliminary investigations reported in [4] [5] [7]. Based on experimental observations of silicide blocked ggNMOS ESD behavior from over 5 CMOS generations (Fig. 1), authors have come-up with several pertinent questions (discussed in the next section), which challenge the conventional theory of current ballasting due to increased S/D resistance. This work, while addressing the contradicting aspects of conventional theory and questions rose, revisits the physics of current filamentation in ggNMOS devices.

II. IS OUR UNDERSTANDING SCIENTIFICALLY COMPLETE

One may argue that why ggNMOS should be discussed when planar technologies are quite matured and already in production. It is worth highlighting that as far as the development of advanced CMOS technologies like FinFET is concerned, a lot of understanding is borrowed from previous generations. To avoid surprises in newer technologies like FinFET or Nanowire, complete understanding of scientific aspects from previous technology nodes is highly desired. Fig. 1(a) shows experimentally extracted It2 trends with technology scaling [8]. The same is depicted in Fig. 2 and Fig. 3 using 2D and 3D TCAD simulations.

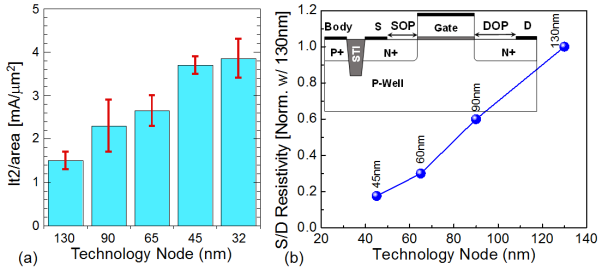

Figure 1: (a) Failure Threshold (It2) trends of ggNMOS device with technology scaling [9] [8]. (b) ggNMOS device schematic and S/D resistivity trend with technology scaling.

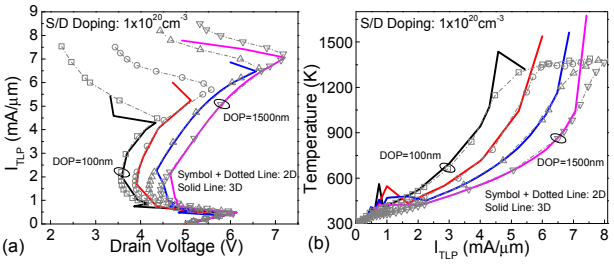

Figure 2: TLP characteristics of ggNMOS devices for different DOPs extracted from 2D and 3D TCAD simulations. No major difference in the 2D device characteristics can be noticed when compared to characteristics extracted using 3D TCAD simulations.

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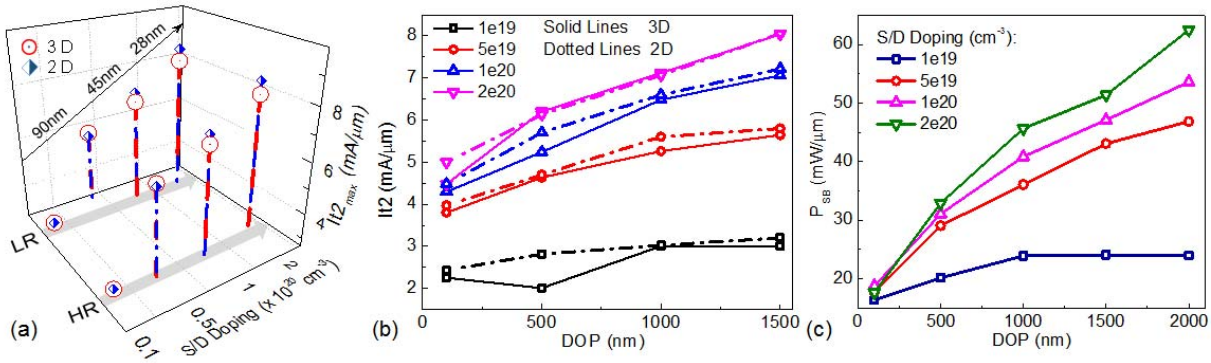

Figure 3: It2 and power to fail as a function of S/D doping extracted from 2D and 3D simulations: (a) It2 vs S/D doping extracted from 3D TCAD simulation for substrates with different resistivity, (b) It2 vs DOP extracted from 2D and 3D TCAD simulations for different S/D doping; and (c) Power to fail vs. DOP extracted from 2D and 3D TCAD simulations for different S/D doping.

It is interesting to note that the It2 of a silicide blocked device improves with the technology scaling, given the fact that S/D sheet resistance falls with technology scaling (Fig. 1 (b)) due to increased S/D doping. It is worth highlighting that the power to fail also increases with technology scaling (Fig. 3).

Fig. 2 further shows that there is no change in TLP characteristics predicted using 2D and 3D TCAD simulations; except the pulse to pulse instability after the first snapback, which is clearly evident in 3D simulations, unlike smooth NDR region predicted by 2D simulations. Fig. 3(a) depicts It2 improvement with technology scaling, i.e., increase in S/D doping, which is independent of substrate resistivity.

Two extreme cases are studied here: high resistive substrate with doping ~ 1 x 10^{15} cm^{-3} (HR) and low resistance substrate with doping ~ 1 x 10^{18} cm^{-3} (LR). Finally, Fig. 3(b) and (c) show It2 and power to fail improvement with increasing silicide blocking length, which surprisingly is independent of 2D or 3D geometry simulated. This signifies that It2 improvement due to silicide blocking is not due to current ballasting, which indeed should be a 3D phenomenon. These observations are contradicting to the conventional theory of current ballasting and role of S/D ballast resistance. These contradictions give rise to following questions:

1. If conventional theory is correct, then why It2 improves when S/D resistance was lowered? Can we say that the current ballasting / uniform conduction are not related to S/D resistance?
2. Why power to fail increases with technology scaling and falling S/D resistance?
3. If non-uniform conduction along the width plays a critical role, why It2 extracted using 2D and 3D simulations are the same?
4. If conventional theory is believed, then why It2 improvement with respect to silicide blocking is evident from 2D simulations as well?

Furthermore, while keeping these concerns in mind, authors see following open questions, which must be addressed for complete understanding of current filamentation and physics of ESD failure in ggNMOS devices:

1. What triggers instabilities or filamentation in ggNMOS device and why these are suppressed by silicide blocking or technology scaling?
2. What are the dynamics of such instabilities as a function of stress current, DOP and technology node or S/D doping? When the instability survives failure and when it becomes critical?
3. What leads to failure in ggNMOS devices? What leads to It2 improvement with DOP and S/D doping?

Answer to these questions are disclosed and discussed in the next section.

III. Electrical & Thermal Instabilities

The observations reveal that the device undergoes an electrical instability right after first snapback and thermal instability around second snapback at higher currents. Moreover, it was noted that these two are two distinct events, but can have an interplay in some specific conditions, which is discussed in this section.

A. Electrical Instability

A thorough investigation of devices transient behavior while establishing the failure physics reveals that in principle the device undergoes following distinct events (Fig. 4) when stressed with current higher than It1.

(i) An electrical instability causing non-uniform turn-on and filament formation;

(ii) Filament spreading and uniform conduction; and

(iii) Thermal instability leading to failure.

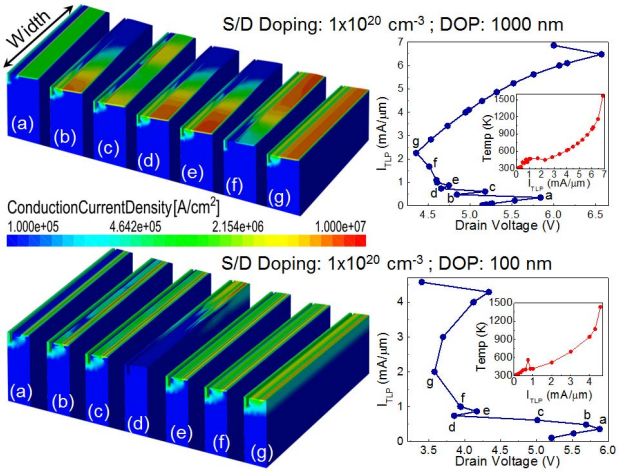

Figure 4: Conduction Current Density and TLP characteristics extracted for different DOP values. Figure depicts current filaments attributed to electrical instability across the ggNMOS device.

The electrical instability causing non-uniform turn-on can be explained as follows: at the verge of snapback, the non-uniform impact ionization (II) at the drain side leads to non-uniform base-emitter junction potential (V_{BE}) drop. A slight change in V_{BE} (Fig. 5 (b)) could perturb an exponential change in emitter current (Fig. 5 (c)), which in turn boosts further localization of impact ionization rigorously (Fig. 5 (d)). This phenomena set up a stage for regenerative / positive feedback, which causes electrical instability and leads to formation of current filament. Presence of this instability and formation of filament in isothermal 3D simulations confirmed that this instability is truly electrical in nature. For a given technology node, as the pulse current increases, the time required to trigger filament instability falls significantly. During this instability, the device may see significant increase in temperature attributed to localized flow of current (Fig. 4 & Fig. 6a), which depends on technology node and DOP as explained in the next sub-section (Fig. 6). If the temperature is higher than the critical temperature, it may directly trigger events causing thermal failure (discussed in next sub-section), otherwise device sees a filament spreading state (Fig. 5).

At currents higher or close to the holding current, device gets enough time to see filament spreading, which relaxes the temperature across the device before uniform self-heating across the device till end of stress pulse. Filament spreading is attributed to fall in impact ionization (II) inside the filament due to self-heating, which extends filament width by triggering adjacent bipolar. For the sake of simplicity, the time steps considered in this work were such that, the filament was statistically stable.

B. Thermal Instability: Current Filamentation Leading to Device Failure

Further exploration of device behavior reveals (Fig. 6) that the peak electric field at the junction falls as the silicide

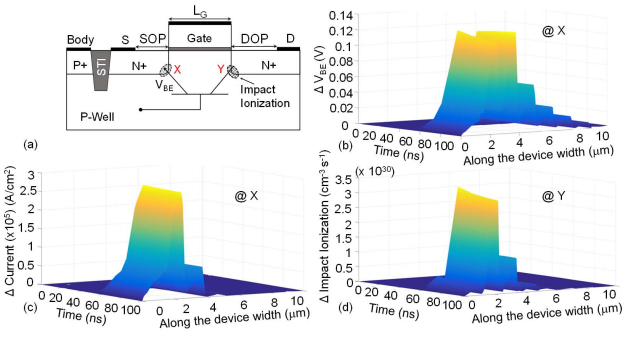

Figure 5: (a) ggNMOS device schematic and critical probe locations; (b) V_{BE} at location X vs. stress time and device width, (b) Conduction Current Density at location X vs. stress time and device width, and (c) Impact Ionization at location Y vs. stress time and device width.

blocking length is increased, however the electric field and impact ionization (II) increases while increasing S/D doping density. Silicide blocking increases the effective junction area, which relaxes the space charge density and hence electric field. The electrical instability, which was triggered by non-uniform impact ionization (II) along the width, becomes more severe with increased S/D doping or reducing silicide blocking length, which explains formation of dense filament after first snapback in case of silicided devices in ultra scaled technologies. However the same is mitigated when DOP increases for any given S/D doping due to reduced electric field and relaxed current density at the drain-substrate junction.

Fig. 7(a) shows a typical lattice temperature vs. time response of a silicide blocked device. Here T_{FI} is the peak temperature after electrical instability, T_C is the critical temperature required for thermal instability, t_1 is the time at which filament instability achieves an equilibrium state, and thereafter device sees a spreading state from t_1 to t_2. t_3 is the time when maximum lattice temperature across the device exceeds critical temperature, which causes formation of thermal filament.

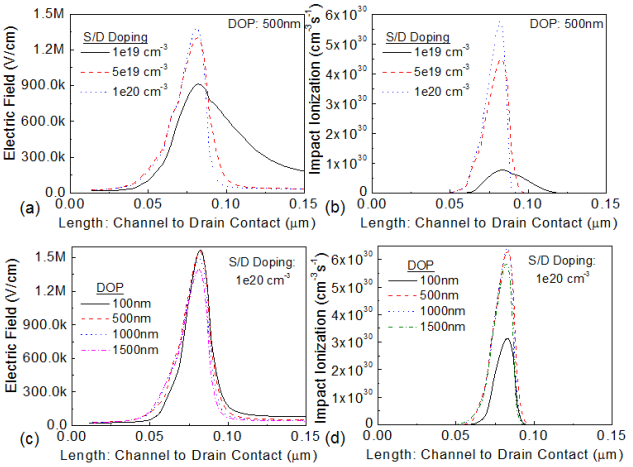

Figure 6: Impact of DOP and S/D doping density on the electric field and impact ionization closed to drain to substrate junction.

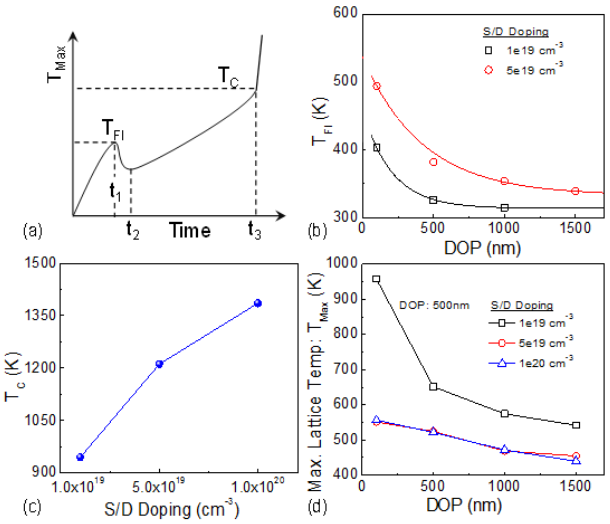

Figure 7: (a) Dynamics of maximum lattice temperature across the device as a function of time and key parameters defining filament dynamics example, T_{FI} and T_C; (b-c) T_{FI} and T_C as a function of DOP and S/D doping, (d) Maximum lattice temperature as a function of DOP and S/D doping.

As the T_{FI} depends on extent of filament instability, T_{FI} falls with increasing silicide blocking length, however increases with increased S/D doping (Fig. 7(b)). T_C solely depends on S/D doping and increases with drain doping concentration (Fig. 7(c)). When $T_{FI} > T_C$, device directly jumps from electrical instability to thermal instability, which leads to formation of thermal filament right after first snapback. Otherwise the device gets into filament spreading state. Finally, it is worth noticing that the maximum lattice temperature in the 2D plane for a given current falls as S/D doping is increased (Fig. 7(d)). These observations explain (i) why electrical instability becomes severe with technology scaling (increased S/D doping), (ii) why silicide blocking mitigates electrical instability and (iii) why It2 increases with increasing doping and/or DOP.

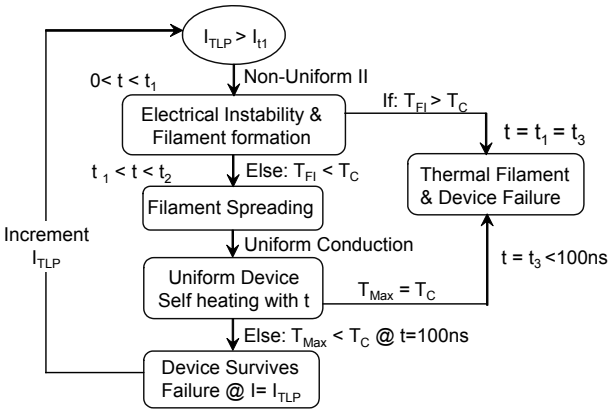

Figure 8: Flow chart explaining filament and failure dynamics.

IV. Summary And Conclusions

This paper highlights findings which contradict with conventional theory of current filamentation in ggNMOS devices. Physics of electrical as well as thermal filament formation and its dynamics with stress time, DOP and S/D doping is explained in detail (Fig. 8). The three states of filamentation are distinguished: electrical instability leading to electrical filament formation, filament spreading, and thermal instability causing thermal filament to form. One can clearly conclude from this work that the current ballasting / uniform conduction in silicide blocked devices is not related to increased S/D resistance. Increased silicide blocking length suppresses peak electric field and impact ionization, which in turn mitigates electrical instability and avoids early instabilities and fail. Moreover, as the critical temperature for thermal instability increases with background doping, increasing S/D doping improves It2 for a given DOP, unlike what conventional theory would have predicted. Finally, it was found that increasing silicide blocking length delays electrical instability, whereas increasing S/D doping delays thermal instability. Therefore, a combination of both increases gap between electrical and thermal instabilities and improves ESD robustness of silicide blocked ggNMOS devices in advanced CMOS technologies.

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