Technology Scaling Effects on the ESD Performance of Silicide-blocked PMOSFET Devices in Nanometer Bulk CMOS Technologies

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Abstract – We present technology scaling effects on the ESD performance of silicide-blocked PMOSFET devices. Stress elements and their effects are characterized using TLP and analyzed with the help of TCAD. Stress liners show no significant effect on ESD performance, whereas the source/drain eSiGe reduces on-resistance by up to 20% and failure current by up to 14%.

I. Introduction

Advanced CMOS technologies use both conventional dimension scaling and disruptive technology innovation at each new generation, in order to achieve projected performance improvement [1][2]. This is even more important in nanometer technologies since conventional scaling of junction depth, gate length and gate oxide thickness, is approaching some physical limits. One of the major process breakthroughs in advanced CMOS technologies is the introduction of numerous stress elements into both NMOSFETs and PMOSFETs (Figure 1) for performance boost. In particular, PMOSFET devices have received more attention because of the readily available SiGe technology that is well understood and fully compatible with the base silicon process. These process elements such as source/drain eSiGe are successfully integrated into the high performance PMOSFETs from 45nm [3] to 32nm [4][5] and beyond. Other stress elements such as the compressive or tensile stress liners are beneficial to either PMOSFETs or NMOSFETs, depending on the stress polarity of the silicon nitride liner.

Although extensive literatures are available on how conventional scaling and different stress elements affect MOSFET performance, it is less known on their effect to devices operated at high current levels, e.g, under ESD-like pulse conditions [6]. It was reported that the failure current of ESD NMOSFETs is not significantly affected by tensile liner process [7], due to the shielding effect of large drain/source contact to gate spacing. The authors found that the on-current improvement of the ESD NMOSFETs is not significant either. However, none of the previous publications discussed the ESD performance of PMOSFETs, which have the most stress elements integrated into the device structure. Silicide-blocked PMOSFETs are usually used in self-protected I/Os in conjunction with silicide-blocked NMOSFETs; or in applications where tolerant I/O is required. As the trigger voltage of PMOSFET drivers becomes smaller in newer generations, it is even more important to make PMOSFET devices in I/O circuits to be self-protected by using the silicide blocking layer.

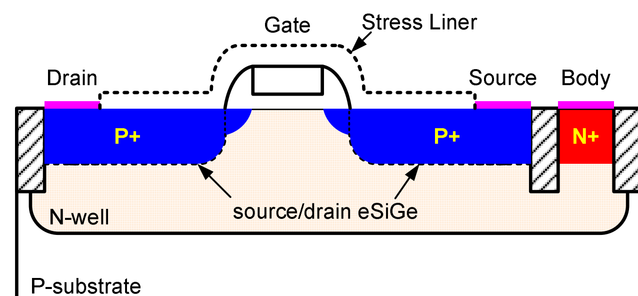

Figure 1. Technology scaling elements in nanometer silicided PMOSFETs: stress liner; source/drain eSiGe; for both high performance and low power technologies

In this paper, we present electrical data, as well as TCAD simulation results to systematically study the effects of technology scaling on PMOSFET devices operated under ESD conditions. Both conventional scaling effect and stress elements effects are presented

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for evaluation of the ever more important PMOSFET devices in nanometer technologies.

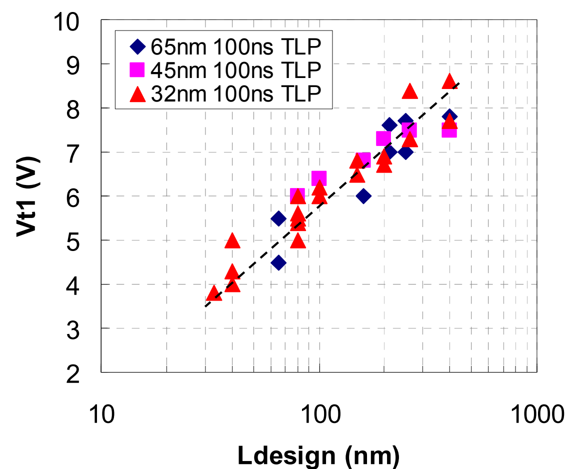
II. Overview of Scaling Effects

General PMOSFET technology scaling effects are plotted in Figure 2 (a), (b) and (c). Electrical data of both thin and thick oxide PMOSFETs are extracted from three generations of bulk CMOS technologies: namely 65nm, 45nm, and 32nm. TLP measurements with 100ns pulse width and ~8ns rise time were used throughout this study. During the DC leakage test, a bias voltage (VDD) was applied, and a 5x shift in leakage current was defined as device failure. Note that these results show the comprehensive scaling effects from three generations of advanced technologies (described in Table 1). For example, 65nm ESD PMOSFETs have a single stress liner; whereas 45nm devices have single or dual stress liners. None of them have junction eSiGe. For 32nm, both thin and thick oxide ESD PMOSFETs have stress liners. In addition, some 32nm thin oxide devices studied in this paper also have source/drain eSiGe process integrated, for improved device performance.

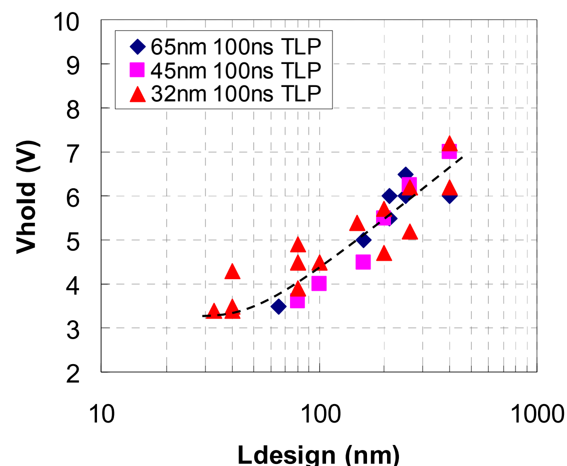
Table 1: Stress elements in 65, 45 and 32nm technologies

Node	65nm	45nm	32nm
Stress liner	Single	Single or Dual	Single or Dual
Junction eSiGe	No	No	Available

Figure 2 (a) and (b) show that the trigger voltage (Vt1) and holding voltage (Vhold) of the lateral PNP transistor (LPNP) decrease linearly with the designed gate length (Ldesign) plotted in log scale. It is clear that technology scaling continues to shrink the ESD design window when PMOSFETs breakdown failure is the limiting factor. However, when Ldesigns are below 80nm, Vhold is approaching Vt1 and no longer decreases, i.e., LPNP shows shallow or no snapback behavior. Figure 2 (c) shows the scaling trend of LPNP failure current per width. For thin oxide devices, the failure current per width is relatively insensitive to gate length, due to little changes in Vhold; whereas for thick oxide devices, the failure current per width improves as gate length decreases because of continuous Vhold scaling. This is consistent with the results reported in [8]. Lower failure current per width is seen in 32nm devices partly because of the shrunk junction depth; however, when normalized per total area, failure current of PMOSFETs are relatively the same from generation to generation, a trend that is similar to ESD NMOSFETs [9].



(a)



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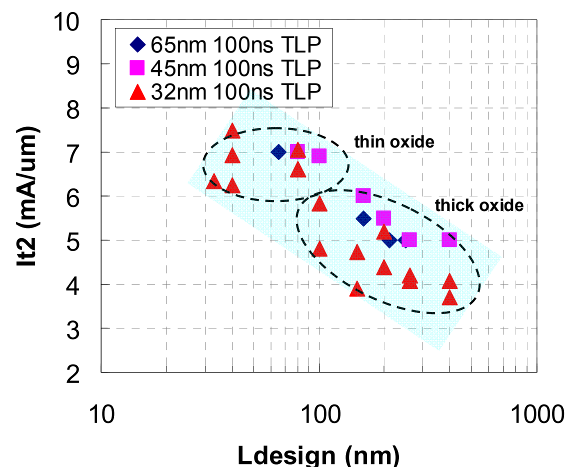

(c)

Figure 2. Extracted 100ns TLP testing data of silicide-blocked ESD PMOSFETs from three generations of nanometer CMOS technologies (a) trigger voltage (Vt1) (b) holding voltage (Vhold) (c) normalized failure current per width (It2)

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III. Stress Liner Effects: Neutral, Tensile or Compressive

This section discusses the effects of stress liners that are implemented to boost MOSFET performance.

Stress liners are silicon nitride materials that are deposited onto the devices to induce stress into the source, drain and channel regions, as shown in Figure 3. It is known that the tensile stress improves electron mobility, and at the same time degrades hole mobility. Therefore, if a tensile stress liner is applied across the entire wafer, it improves NMOSFET drive current, and reduces PMOSFET drive current. This is true for compressive liners too, albeit they affect device performance in the opposite direction. Sometimes a single stress liner process is used to boost performance of only one type of transistors, in order to maximize the total performance per cost for certain applications. In high performance technologies, both compressive and tensile stress liners can be implemented onto the same wafer to benefit both NMOSFETs and PMOSFETs.

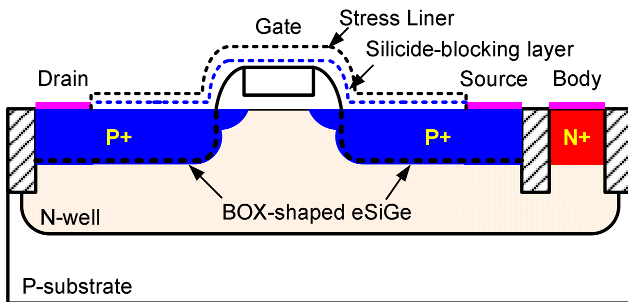
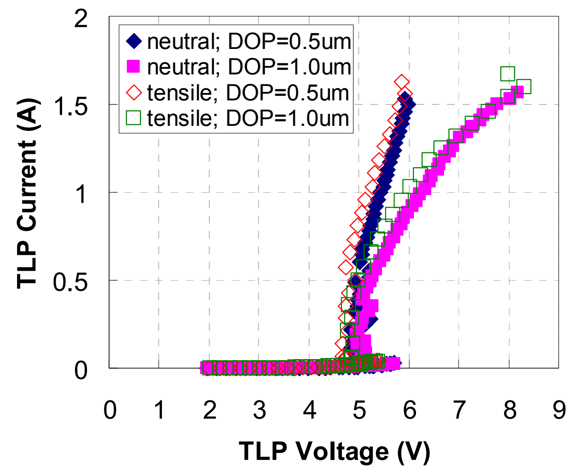
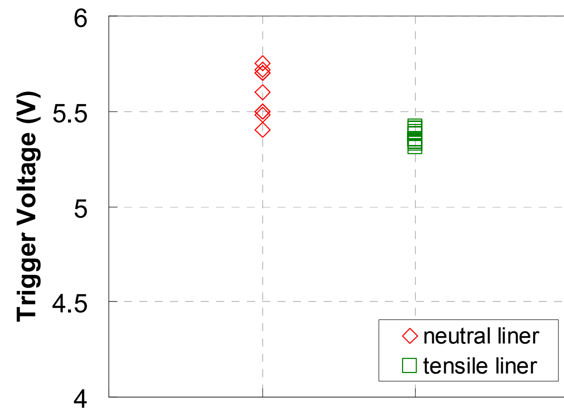


Figure 3. ESD silicide-blocked PMOSFETs device showing both silicide-blocking layer and stress liner

Figure 4(a) and (b) show 100ns TLP data of 32nm ESD PMOSFETs for two different cases: neutral stress liner, i.e., no stress effect; and tensile stress liner. It is seen that there are no significant changes to the key TLP metric numbers such as Vt1, Vhold and It2. This is not surprising. Since all ESD PMOSFETs already have nitride silicide-blocking layers with neutral stress covering the drain, source and gate areas, as shown in Figure 3, the stress effects created by stress liners on top of the silicide-blocking layer are damped by as much as ~70% simulated through TCAD, resulting in very similar ESD performance in both cases. Measured P+ diffusion and N-well sheet resistance results (with or without stress liners) confirmed this finding. In addition, even if the hole mobility is slightly modulated by the stress liner, its effects would only show in low current regions such as where the triggering of the LPNP happens; at high current regions, e.g., where the device operates at close to its failure point, the hole mobility is largely dominated (degraded) by thermal scattering, rather than by stress modulation.



(a) 100ns TLP I-V data



(b) Extracted 100ns TLP Vt1 data from multiple chips

Figure 4. silicide-blocked ESD PMOSFETs with neutral or tensile stress liners. The drain silicide-block lengths (DOP) are 0.5um and 1.0um. The source silicide-block lengths are 0.2um

TCAD results confirm this analysis, as shown in Figure 5. The 100ns TLP simulation is performed for neutral liner, tensile liner, and compressive liner (over silicide-blocking layer) cases. There are no significant changes in Vt1, Vhold, or current characteristics in general. However, the simulation does indicate that if larger stress is transferred to the transistor, the case when the slicide-blocking layer is absent, the device with tensile liner would show ~0.4V lower Vhold, due to the combined effect of both LPNP beta and LPNP base resistance.

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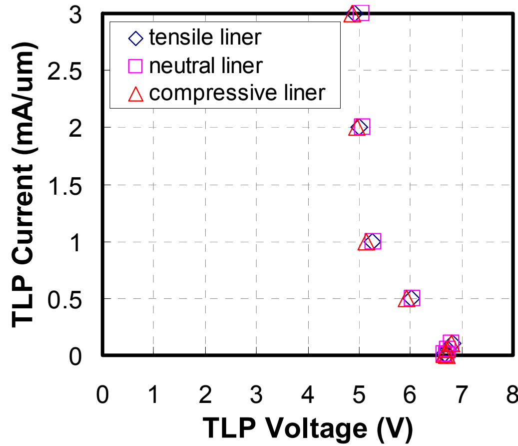

Figure 5. TCAD simulation results of 100ns TLP for silicide-blocked ESD PMOSFETs with neutral, tensile and compressive liners. The drain silicide-block lengths are 0.5um.

IV. Source/Drain eSiGe Effects

Source/drain eSiGe is introduced into PMOSFETs for performance boost. The effects of eSiGe source/drain compared to a conventional silicon source/drain are studied in this section.

Figure 6 shows the 100ns TLP I-V data of PMOSFET devices with or without eSiGe. It is seen that the devices with eSiGe show up to ~20% lower on resistance. This is mainly because the eSiGe LPNP has in-situ source/drain P+ dopants in addition to the source/drain dopants, implanted for both cases. However, since the eSiGe P+ diffusion region has higher self-heating effect than the silicon one, the on-resistance difference becomes smaller for devices with larger silicide-blocking length. For example, the devices with largest DOP length (2.0um) show smaller clamping voltage differences at 1A than the devices with DOP of 1.0um. Also the devices with DOP of 2.0um show even smaller clamping voltage differences at 1.5A than at 1.0A. This is because self-heating effect becomes dominant at higher current regions. On the other hand, the SiGe LPNPs also show ~6%-14% lower failure current at the same time, possibly due to the higher thermal effects of the SiGe material. For maximum failure current performance, the conventional silicon-based ESD PMOSFETs show more advantages.

Another interesting study is on the eSiGe effects to ESD PMOSFETs when the eSiGe process is changed from a conventional BOX shape to a SIGMA shape [10], as shown in Figure 7. The SIGMA-shaped eSiGe process is designed to induce more mechanical stress into the channel region by making an angled source/drain etch followed by eSiGe epitaxial growth. The tipped region inside the eSiGe trench produces higher stress onto the channel region than a conventional BOX-shaped eSiGe, therefore greatly improve the hole mobility.

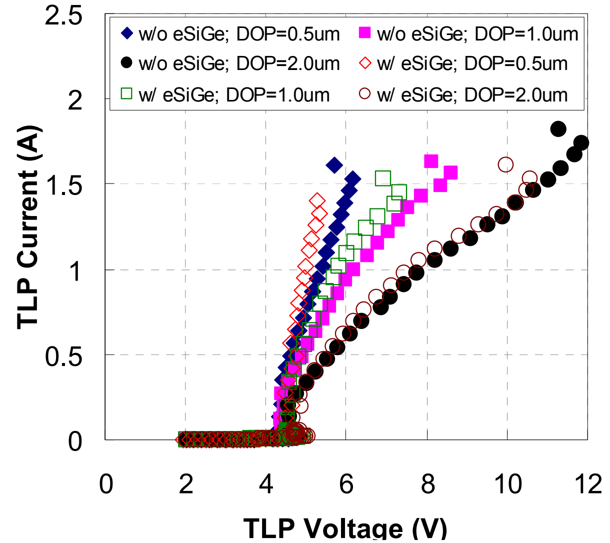

Figure 6. 100ns TLP I-V data of ESD PMOSFETs with or without source/drain eSiGe. The drain silicide-block lengths are 0.5um, 1.0um and 2.0um.

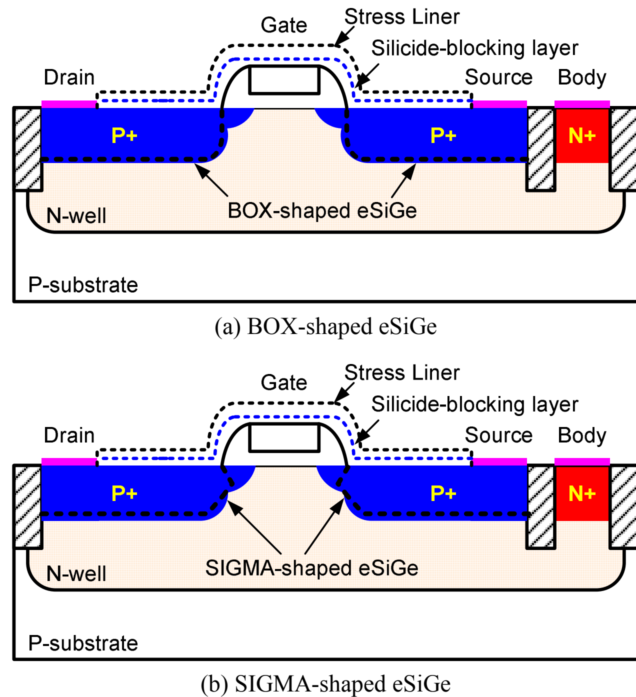

Figure 7. Cross-sections of the PMOSFETs with eSiGe source and drain that are (a) BOX-shaped and (b) SIGMA-shaped

The 100ns TLP I-V data of both devices are shown in Figure 8. It is seen that the PMOSFETs with SIGMA-shaped eSiGe show ~0.5V less Vt1 and Vhold, but similar failure current. This is due to the higher stress

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effects induced by the SIGMA-shaped eSiGe source and drain design (~1.6X higher than BOX-shaped eSiGe), which result in higher LPNP beta, as confirmed by TCAD simulation shown in Figure 9. However, at higher current, the differences in beta diminish and the failure currents no longer show significant difference for these two cases.

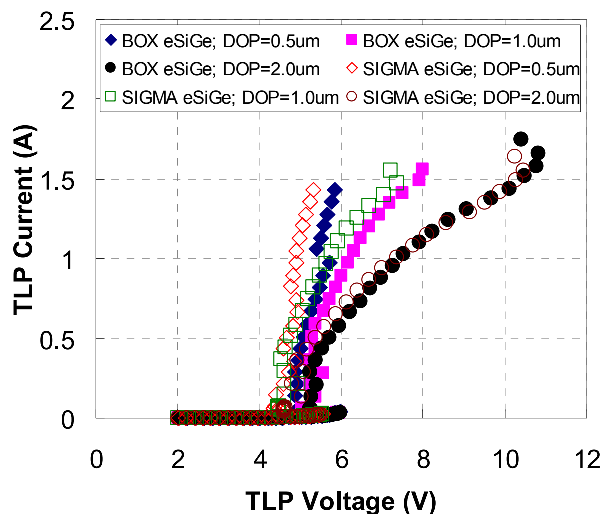

Figure 8. 100ns TLP I-V data of ESD PMOSFETs with BOX-shaped or SIGMA-shaped source/drain eSiGe. The drain silicide-block lengths are 0.5um, 1.0um, and 2.0um.

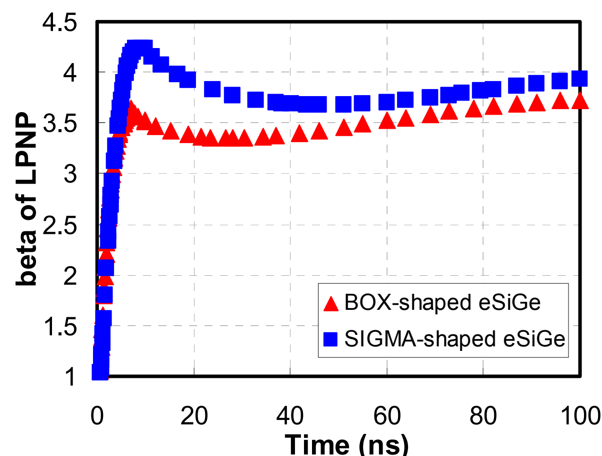

Figure 9. TCAD simulation results of LPNP beta shown for devices with BOX-shaped or SIGMA-shaped source/drain eSiGe (simulated at 3mA/um)

V. Conclusion

We present comprehensive technology scaling effects on the ESD performance of silicide-blocked ESD PMOSFET devices. Technology scaling continues to shrink the ESD design window and results in lower failure current per width for newer generations of devices. Stress liners do not have significant effect because of the shielding effects of the silicide-blocking layer, and further diminished stress effects at high current regions. For ESD PMOSFETs with source/drain eSiGe, higher beta of the SIGMA-eSiGe LPNP helps in both trigger voltage and holding voltage (~0.5V lower), compared to BOX-eSiGe LPNP. However, at the same time, the failure current of ESD PMOSFETs is lower (up to 14%) than the ones without eSiGe.

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