On the Transient Behavior of Various Drain Extended MOS Devices under the ESD stress condition

Mayank Shrivastava[1], Harald Gossner[2], Maryam Shojaei Baghini[1], V. Ramgopal Rao[1]
[1]Center for Excellence in Nanoelectronics, Department of Electrical Engineering, Indian Institute of Technology-Bombay
Mumbai-400076, India, shrivastva.mayank@gmail.com; rrao@ee.iitb.ac.in
[2]Infineon Technologies AG, P.O. Box 80 09 49, D-81609 Munich, Germany, Harald.Gossner@infineon.com

Abstract— This paper presents **ESD evaluation of various nanoscale drain extended MOS devices. Current and time evolution of current filaments formed under the ESD stress conditions are investigated. A complete picture of device's behavior at the onset of space charge modulation and the evolution of current filamentation is discussed based on Transient Interferometric mapping studies**.

Keywords- Drain extended MOS, ESD, It2, space charge modulation, TIM, base push out, current filament .

I. INTRODUCTION

The drain extended NMOS (DeNMOS) is a High Voltage (HV) device, which can be easily integrated with standard CMOS process in sub 100 nm node technologies. Attributed to shrinking ESD window it is very important to design self-protecting I/O devices, since the I/O devices may themselves be prone to fail because of an ESD event. Reliability of DeNMOS device under ESD stress is very critical for its use as an ESD protection device for some HV I/O circuit applications and its use as for I/O device applications. However these devices have been found to be extremely vulnerable to ESD events and till now, several mechanisms have been proposed for DeNMOS failure [1]-[9]. In most of the published works, the modeling of the ESD behavior of DeNMOS devices, were normally based on 2D TCAD simulations. Due to this it lacks a detailed physical insight required to predict the cause for filamentation and device failure. Along with 3D TCAD simulations, Transient Interferometric Mapping (TIM) is another useful tool for understanding the device behavior under the ESD stress condition [10]. TIM method monitors the temperature and free-carrier concentration induced changes through a change in the silicon refractive index. The motivation of this paper is to have a complete picture of the transient device behavior during various phases of current filamentation using TIM method.

II. DEMOS DEVICES AND TCAD SETUP

A. Various Drain Extended MOS Devices

Fig. 1a shows STI type DeNMOS device. It consists of (i) a deep N-Well region in order to achieve reduced surface fields and (ii) a STI in the drift region (i.e. underneath gate-to-drain overlap), which alleviates the high voltage handling capability of the device. We found that the parameter DL (Drain Diffusion Length, Fig. 1b) is the key for optimization of STI-DeMOS device [12,13]. Moreover such a device was processed in state-of-the-art sub 100nm node CMOS technology consisting thin gate oxide [14]. Fig. 1b shows another type of drain extended device i.e. RESURF DeNMOS [14]. Unlike STI-DeMOS, it uses a dedicated RESURF well in order to reduce the surface fields, which eventually improve junction breakdown voltage.

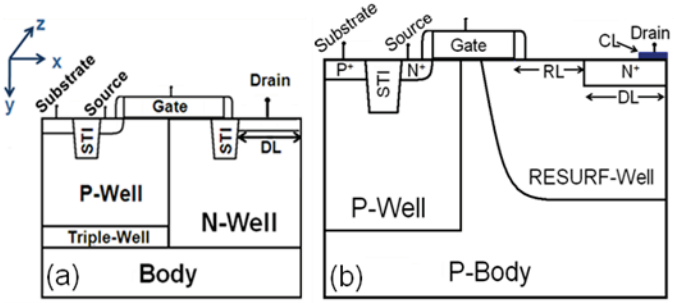

Figure 1: (a) STI DeNMOS and (b) RESURF DeNMOS devices

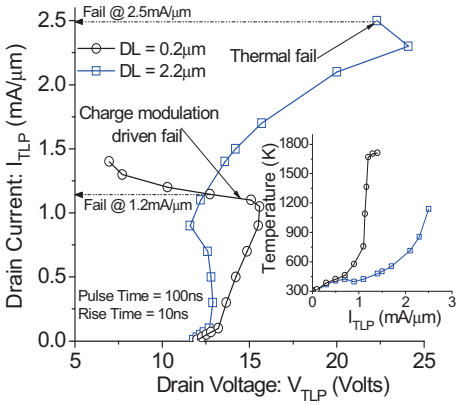

Figure 2: Simulated (3D) Transmission Line Pulsing (TLP) characteristics for Human Body Model (HBM) of DENMOS device having different drain diffusion length (DL). We find that the devices having higher DL survive higher currents.

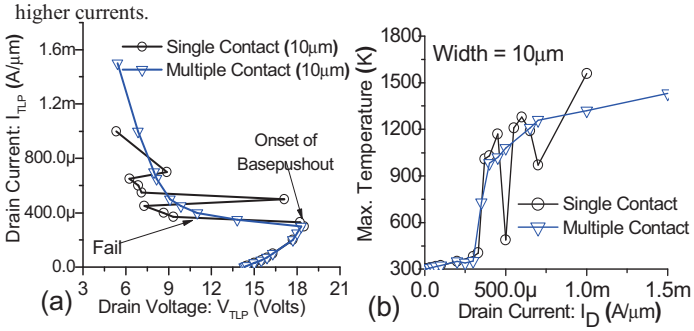

Figure 3: (a) Simulated TLP characteristics (HBM) of single contact strip and multiple contact strip devices. (b) Shows Temperature rise with increasing TLP current for device with width = 10μm.

B. *Device Behavior*

A well calibrated device and process simulation deck was used for the TCAD and TIM studies. The simulated TLP characteristics (Fig. 2 & 3) of both the devices (STI DeNMOS with DL=0.2µm and RESURF DeNMOS) show that the device undergoes failure at a very low current (~1.2 mA/µm and ~0.3mA/µm, respectively). Device behavior before failure can be explained as follows:

(i) Junction Breakdown: **I**nitial current, flowing through the device, is because of junction breakdown.

(ii) Bipolar Triggering: The parasitic bipolar triggers inefficiently ($\beta < 1$) at lower currents (0.1mA/µm). However, it triggers efficiently at moderate currents (0.2-0.3mA/µm). A bimodal behavior was also detected for RESURF DeNMOS, which indicates pulse-to-pulse instability during the onset of current filamentation.

(iii) Onset of space charge modulation (1mA/µm & 0.3mA/µm, respectively): device suffers from current filamentation and early thermal failure.

(iv) Device with higher DL: Increasing DL alleviates onset of space charge modulation, which eventually improves the ESD performance of the STI-DeMOS device (Fig. 2).

III. TRANSIENT INTERFEROMETRIC MAPPING SIMULATIONS

In this section we provided an insight into 3D filament behavior of both the devices using TIM simulations. For all devices X_{max} and X_{min} (length along the channel) is the drain and source end of the device, respectively. Similarly Z_{max} and Z_{min} (length along the device width) is the back and front end of the device, respectively. Both STI type devices have a half width of 4µm. The wavelength of the probing beam for TIM simulations was taken as 1.3µm (in air).

A. *STI DeNMOS (DL=0.2µm)*

An early base push-out or space charge modulation due to very high carrier density in the N-Well region was observed in this device [11]. Fig. 4 shows phase shift evolution for various TLP pulses (i.e. 0.3, 0.7 1 and 1.2 mA/µm) at pulse time=100ns. For a TLP pulse of 0.4mA/µm, almost uniform phase shift (i.e. 0.4 rad) along the device width and length was found. This show that at lower currents heating inside the device was almost uniform along the width, which is attributed to uniform current flow before the onset of base push-out. Slightly higher phase shift at the front end of the device is partially due to (i) current crowding at corners and (ii) non uniformity created in the device along the width. Since high electric field exists at the well junction before the onset of space charge modulation, it leads to maximum rise in phase near to the well junction (at X=0.8µm). Furthermore, at a moderate current, non uniform phase shift along the device width was observed. The peak phase-shift was observed at front side near to drain end. The shifted location of peak phase-shift (hot spot) under drain diffusion from well junction was attributed to the onset of base push-out near the drain diffusion. The variation in phase-shift along the device width was not significant (i.e. from 1.5 rad at front end to 1 rad at back end), which shows that there is an onset of filament but still not dominant. For higher TLP currents (i.e. 1 and 1.2mA/µm), there is no significant change in phase-shift in other parts of device except front side of drain end. This abrupt change at drain end is attributed to significant heating under drain diffusion because of strong space charge modulation and current filamentation. No rise in phase in other parts of the device shows less heat flux coming out from the hot spot (i.e. near drain diffusion). This is attributed to the STI in vicinity of hot spot.

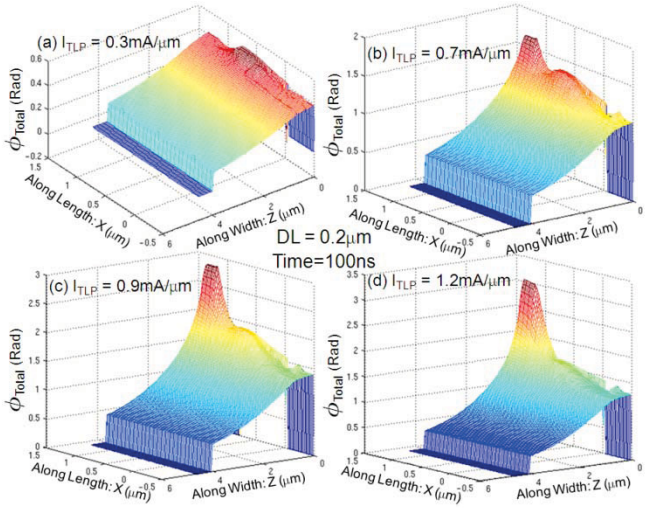

Figure 4: Phase shift for STI type DeNMOS device with DL=0.2µm for different forced TLP pulse (i.e. 0.3, 0.7 1.0 and 1.2 mA/µm) at 100ns.

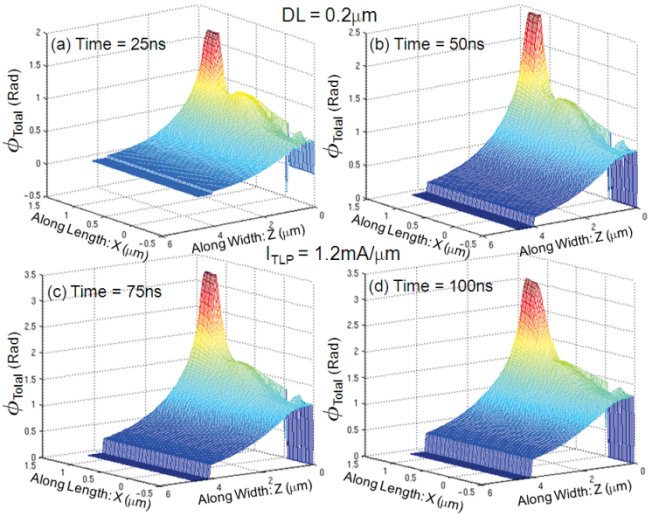

Figure 5: Phase shift for STI type DeNMOS device with DL=0.2µm for different forced TLP pulse (i.e. 0.3, 0.7 1.0 and 1.2 mA/µm) at 100ns.

In order to investigate the time evolution of current filament and self heating inside the device, phase-shift for a TLP current of 1.2mA/µm (which causes strong space charge modulation) at different times, i.e. 25, 50, 75 and 100ns, was studied as shown in Fig. 5. The figure shows that the location of hot spot was always near to the drain diffusion, which is due to strong space charge modulation and very high electric fields under the drain diffusion [13]. It depicts the maximum change

in signal-phase during 25-50ns (Δϕ=1 Rad in 25ns), however it changes by 1 rad during next 50ns (50-100ns). Maximum rise in phase (i.e. temperature rise) during early time scale shows instantaneous power dissipation during first 25-50ns.

B. Modified STI DeNMOS (DL=2.2μm)

This device was modified in a way to alleviate the onset of base push-out to higher current. Fig. 6 shows phase-shift for various pulsed currents (i.e. 1.1, 1.5 and 2.3 mA/μm) at pulse time=100ns. (*NOTE: The device width was 4μm, the data from Z= 4 to 10μm have no physical relevance in figure 5.13 and 5.14*). At lower current the phase-shift was almost uniform along the device width/length except front side of well junction, which is attributed to (i) a slightly higher current density near to the front end and (ii) peak electric field at the well junction. Furthermore, at I_{TLP}=1.1mA/μm, a lower value of phase-shift (i.e. ~1 rad) shows significantly less heating as compared to standard STI DeMOS device (i.e. DL=0.2μm). It is evident from Fig. 6 that self heating always takes place at well junction, which also validates an absence of space charge modulation and associated effects. Lower current density and higher volume available for heat diffusion (i.e. improved heat flux) at well junction is another major cause for relaxed heating and improved failure threshold. Moreover, at higher TLP currents (i.e. 1.5 and 2.3 mA/μm) the phase-shift (hot spot) increases at the front well junction. At failure current, device with DL=2.2μm has a higher ϕ (~ 3.5 Rad) and less abrupt (i.e. smooth) phase shift distribution across the device length/width as compared to the device with DL= 0.2μm (ϕ ~ 3.5 Rad). However, the peak temperatures observed through TCAD simulation were same (i.e. 1500 K) at failure. The smooth distribution of phase-shift shows improved heat flux in the modified device.

The observed higher phase-shift (even when the heat flux was improved and peak temperature near to the hot spot was similar) can be explained in following way- the device with DL=2.2μm (no base push-out) causes self heating at the well junction, where the current filament is more relaxed (i.e. higher filament radius) as compared to device with DL=0.2μm (caused heavy charge modulation). This eventually leads to a broader hot spot at well junction as compared to device suffering from charge modulation (where the hot spot sits under drain diffusion). Since the total phase-shift (φ) is the integral of the change in phase [Δφ(y)] over the full device depth (d), as shown in eq. 1 [10], the total phase-shift in a device with deeper hot spot will be higher as compared to device having narrow and localized hot spot. Other way around, higher phase shift at a equal temperature also validates (i) a broader radius of the current filament or tube and (ii) relaxed current density at well junction in the modified device.

$$\phi = \int_0^d \Delta\phi(y)\partial y \qquad (1)$$

Fig. 7 shows time evolution of current filament and self heating inside the device. Small rise in the phase of TIM signal during initial 50ns shows significantly relaxed heating due to almost uniform current flow. However, it rises up to 6 Rad within next 25ns, which shows an onset of current filament. Furthermore, device fails due to excess heating between 75-100ns of time scale. Figure does not show any sudden change in the phase shift during 100ns of TLP pulse, unlike to DL=0.2μm case. This validates that the modified device does not suffer from heavy charge modulation driven instantaneous current collapse or isothermal filamentation, which eventually contributes to higher failure threshold.

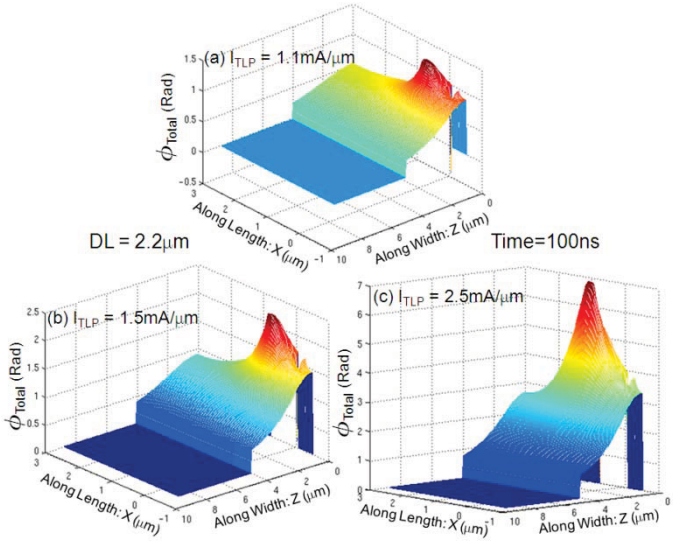

Figure 6: Phase shift for STI type DeNMOS device with DL=2.2μm for different forced TLP pulse (i.e. 1.1, 1.5 and 2.3 mA/μm) at 100ns.

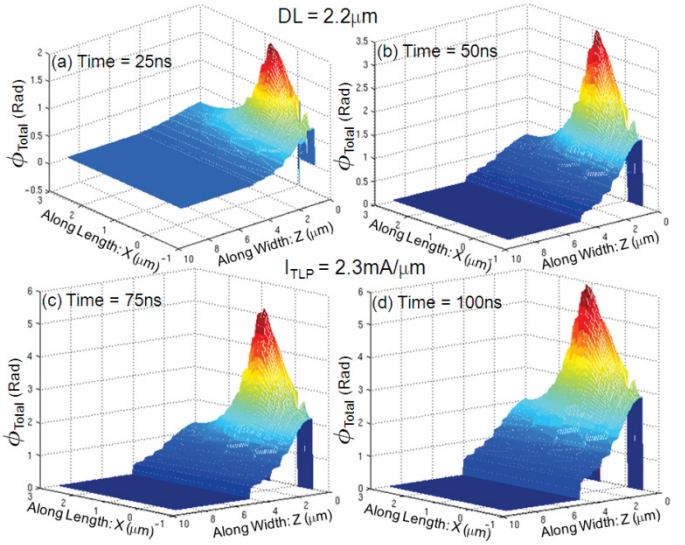

Figure 7: Phase shift for STI type DeNMOS device with DL=2.2μm at different times (i.e. 25, 50, 75 and 100ns) for a forced TLP pulse of 2.3 mA/μm .

C. RESURF DeNMOS

This is the device, which experiences space charge modulation at a very low current (i.e. ~0.3mA/μm). The actual half width of the simulated device was 10μm. Fig. 8 shows pulsed-current evolution (i.e. 0.2, 0.3, 0.4 and 0.5mA/μm) of

carrier and heat distribution across the device at pulse time= 100ns. At lower $I_{TLP,}$ (i.e. 0.2mA/µm) the current distribution was almost uniform along the width. Furthermore, at I_{TLP} = 0.3 mA/µm, the phase-shift at the front end increases up to 1 Rad, which is due to the onset of base push-out driven current filament. A uniform and smaller rise in signal phase (i.e. 0.15 Rad) for I_{TLP} = 0.4mA/µm shows uniform current flow along the width. This shows that the device was able to survive base push-out driven current filamentation. Moreover, it also shows a unique behavior leading to pulse-to-pulse instability in the TLP characteristics. Furthermore, at higher currents we observed a strong current filament formation, which leads to a very deep snapback in the TLP characteristics. This behavior is evident from a very phase-shift (i.e. 2 Rad) near to the front corner. The localized charge modulation along the device width causes a local heating near drain diffusion, which eventually causes irreversible damage to the device.

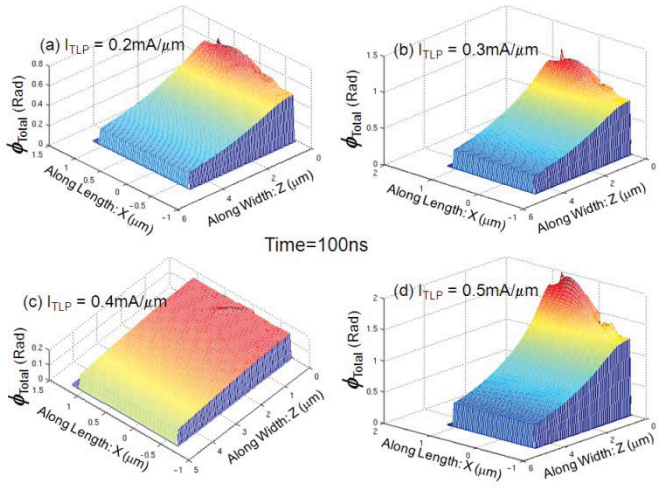

Figure 8: Phase shift for RESURF DeNMOS device for different forced TLP pulse (i.e. 0.2, 0.3, 0.4 and 0.5 mA/µm) at 100ns.

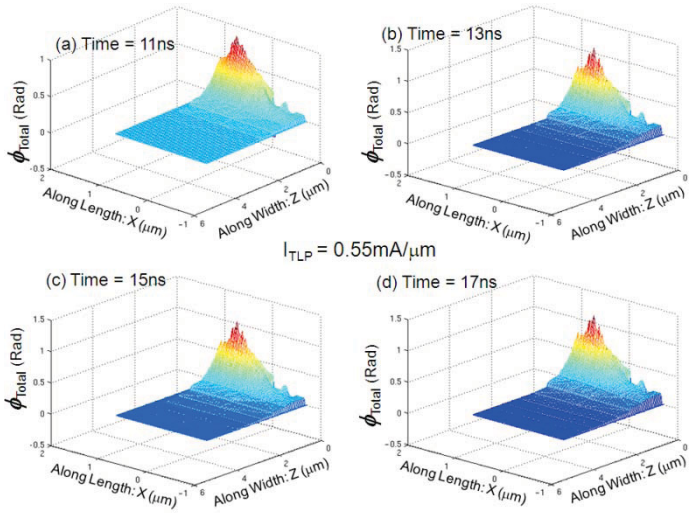

Figure 9: Phase shift for RESURF DeNMOS device at different times (i.e. 11, 13, 15 and 17ns) for a forced TLP pulse of 0.55mA/µm

Figure 9 shows time evolution of current filament and self heating i.e. phase-shift after the strong charge modulation, i.e. 0.55mA/µm Unlike to STI type devices, RESURF devices have significantly fast formation of current filament (i.e. with ~10 to 15ns). However, both the devices suffers from similar mechanisms, which lead to early device fail.

IV. Conclusion

Transient Interferometric mapping simulation studies of drain extended ULSI devices under ESD stress conditions have been presented for the first time and compared for different drain extended MOS device options. A significantly improved failure current of the modified drain extended NMOS was shown by alleviating the onset of base push-out. Using a combination of TCAD device simulation and TIM t, detailed device physics behind the critical ESD phenomena under high current transients could be explored. This understanding paves way for further device optimization and TCAD-based ESD robustness prediction.

References

[1] P. Hower, et. al., *Proc. of* ISPSD '99, pp. 55-58.

[2] P. L. Hower, et. al., *Proc. of IEDM*, pp. 193-196, 99.

[3] P. L. Hower, *Proc. of* ISPSD, pp 1-8, 2002.

[4] P. Moens, et. al., *Proc. of* ISPSD, pp. 221-224, 2004

[5] P. Moens, et. al., *Proc. of* IRPS, pp. 393-398, 2004.

[6] Gianluca Boselli, Vesselin Vassilev and Charvaka Duvvury, " Drain Extended NMOS High Current behavior and ESD protection strategy for HV application in sub 100nm CMOS technologies", IRPS, pp. 342-347, 2007.

[7] A. Chatterjee, et. al., Proceedings of International Electron Device Meeting 2005, pp 195-198.

[8] A. Chatterjee, et. al., IEEE International Electron Devices Meeting (IEDM), 2007, pp 181-184.

[9] A. Chatterjee, et. al., IEEE International Reliability Physics Symposium , 2007, pp 608-609..

[10] M. Litzenberger, et. al., "Scanning heterodyne interferometer setup for the time resolved thermal and free carrier mapping in semiconductor devices", IEEE Trans Instrumentation Measurement Vol. 54, 2005, pp. 2438–2445.

[11] Mayank Shrivastava, et. al., *Electron Devices, IEEE Transactions on* , vol.57, no.9, pp.2235-2242, Sept. 2010

[12] Mayank Shrivastava, et. al., *Electron Devices, IEEE Transactions on* , vol.57, no.9, pp.2243-2250, Sept. 2010

[13] Mayank Shrivastava, et. al., IEEE International Reliability Physics Symposium, 2009, pp. 669-675.

[14] Mayank Shrivastava, et. al., "On the differences between 3D filamentation and failure of n & p type drain extended MOS devices under ESD condition", IRPS-2010.