3D TCAD Based Approach for the Evaluation of Nanoscale Devices During ESD Failure

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***Abstract*— This paper demonstrates a 3D TCAD based approach towards the evaluation and pre-silicon development of nanoscale devices for advanced ESD protection concepts. Impact of various physical models and parameters on the accuracy of predicted ESD figures of merit are discussed. Moreover, various devices options, have been evaluated from 3D TCAD simulations.**

Keywords- ESD, It2, space charge modulation, on-state spreading, thermal failure, moving filaments.

I. INTRODUCTION

An electronic system often has multiple semiconductor chips fabricated in different technologies. Therefore, for interfacing between semiconductor chips or sub-systems in a chip having different levels of supply voltage, while satisfying speed and noise requirements, input-output (I/O) devices and circuits are important. One of the bottlenecks for introducing CMOS I/O circuits is their susceptibility to Electro Static Discharge (ESD) [1]. This problem is further increased by tight design window for high performance I/O circuits, not allowing large ESD devices to be used as protection elements [2]. This ends up reducing the number of options available to an I/O designer [3]. 2D TCAD simulations were used by different groups [4]-[8] in the past in order to model the ESD behavior of various I/O or ESD protection devices. Some of the devices like grounded gate NMOS and SCR fail purely due to excess temperature rise (at drain/anode) and thermal runaway at very high TLP currents can easily be modeled using 2D device simulation. However, we found that devices like drain extended MOS [9] or in general devices which suffer from heavy charge modulation at early currents, cannot be modeled using 2D device simulations. As discussed in [10], since the modeling for the ESD behavior of various devices [11]-[13] is normally based on 2D simulations, it lacks the physical insight required to predict the 3D filamentation and failure. Moreover we also found that 2D simulations for ggNMOS or SCR like structures underestimate the It2 value [14]. Keeping these points in mind, we demonstrate a 3D TCAD based approach towards the evaluation and pre-silicon development of nanoscale devices for advanced ESD protection concepts.

II. 3D TCAD APPROCH AND SETUP REQUIREMENTS

A. Electrical and Thermal Boundary Conditions

In order to achieve close predictions from ESD TCAD, primarily it is most important to have accurate definition of the thermal and electrical boundary conditions. This is only possible by a proper definition of device under test in the TCAD environment. Following points have to be considered while defining a device for ESD evaluation:

(i) *Parasitic paths should be captured properly*. This is possible only by proper definition of doping profiles and substrate/well contacts (Fig. 1a & 1b).

(ii) *Proper definition of electrical contacts*. It is worth mentioning that load line of TLP setup or resistance of the pulse line has big impact on the TLP characteristics. In order to capture the same, proper definition of electrical contacts is important (Fig. 1a).

(iii) *Proper definition of thermal boundary conditions*. Thermal contacts should be placed far apart from the active region in order to properly capture the heat transport across all 3 dimensions of active device. For ex. keeping depth ≥ 5µm gives near realistic thermal boundary conditions for 100ns of TLP pulse (Fig. 1b).

(iii) Physical non-uniformity must be incorporated in order to capture current filaments, which can easily be accomplished by defining multiple contacts across the device width with unequal spacing between them.

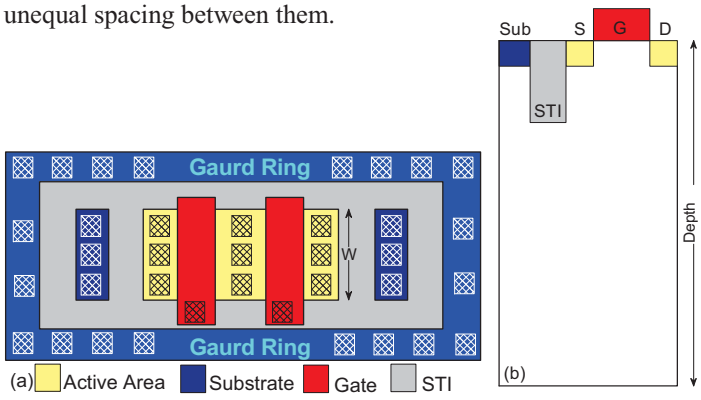

Figure 1: (a) Layout/top and (b) cross-sectional view of required device description in 3D TCAD for ESD evaluation.

B. Minimum Device Width (W) and Meshing Requirements

It2 of devices like ggNMOS or SCR can be approximated (with 20% underestimated value) from 2D simulations, however a 3D simulation with *min width ~ 5µm* can give even better approximation (error less than 5%). It is worth mentioning that even better predictions are possible by using higher device width in 3D TCAD environment at the cost of simulation time and complexity. In order to reduce simulation time while keeping accuracy in ESD predictions, it is worth having knowledge of appropriate width of various types of

devices. Devices which fail due to electrical or isothermal filamentation require a *min width > 15μm* in order to capture current filamentation and it failure. On the other hand, devices consisting ON state spreading of current filaments [14] should have a *min width > width required for uniform spreading in 100ns* (HBM).

III. IMPORTANT MODELS AND SENSITIVE PARAMETERS

It is always good to use minimum number of physical models for TCAD simulation. This helps in reducing the simulation time; on the other hand it can also lead to a wrong prediction. In order to reduce the simulation time with an accurate prediction, it is required to have a knowledge of the sensitive device parameters and their dependence on various physical models.

A. Impact Ionization

Since the device operates under high voltage and current conditions during an ESD stress, it is very important to use well calibrated physics based model for impact ionization. Almost every parameter i.e. transient voltage overshoot, It1, It2, Vt1, Vt2 and holding voltage depend on the impact ionization. Moreover, an impact ionization model should also be well calibrated for very high temperatures (~1200K). Impact ionization at very high temperatures also affects the ON state spreading of current filamentation in the device [14].

B. Carrier life time

Carrier life time is a very important parameter for device's turn-on time. However, since it does not affect the self heating behavior, it has no impact on the ESD failure and It2/Vt2 of the device as shown in Fig. 2. Fig. 2 shows that switching-off of the (i) carrier-carrier scattering driven mobility dependence, (ii) auger recombination, (iii) doping dependent carrier scattering and mobility degradation and (iv) SRH recombination models, has no impact on the TLP characteristics of a parasitic NPN device.

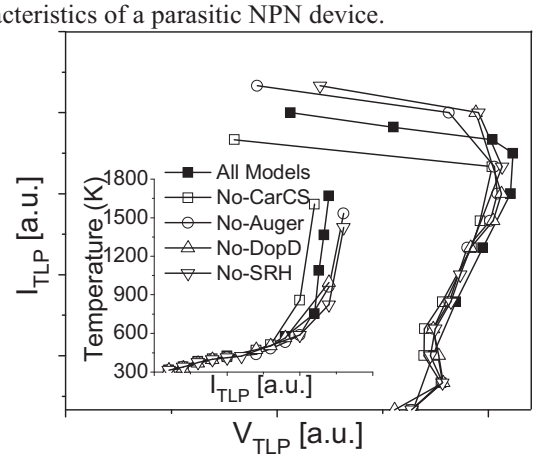

Figure 2: Impact of switching off - (i) carrier-carrier scattering dependent mobility dependence, (ii) auger recombination, (iii) doping dependent carrier scattering and mobility degradation and (iv) SRH recombination models, on the TLP characteristics of device under investigation (parasitic NPN).

C. High Field and Temperature Mobility

Since device operates under very high electric field and very high temperature conditions, transport models must be calibrated for such extreme situations. Fig. 3 shows that high electric field saturation and mobility degradation of majority carriers (i.e. electrons for parasitic NPN) have a significant impact on the TLP characteristics and failure current/voltage (It2/Vt2) of the parasitic NPN device under investigation. Moreover, figure 3 shows that mobility degradation of minority carriers (i.e. hole for parasitic NPN) under very high electric fields has a significant impact on the bipolar triggering of device under ESD stress.

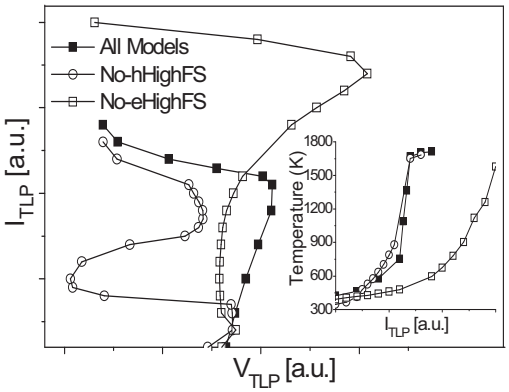

Figure 3: Impact of switching off – high electric field saturation and mobility degradation models for majority (No-eHighFS) and minority (No-hHighFS) on the TLP characteristics of parasitic NPN device.

IV. TCAD INVESTIGATIONS: WHAT CAN BE DONE

Until now we studied the approach for 3D TCAD and sensitive parameters for investigation under the ESD stress conditions. In this section we will discuss about various device options, which can be investigated accurately with advanced 3D TCAD. Moreover, we will also talk about the associated physics of ESD failure - investigated from 3D TCAD - while stressing different device types.

A. Electrical or Iso-Thermal Filamentation

Drain extended MOS (DeMOS) devices are known for their early failure due to space charge modulation or base push out at very low TLP currents. This leads to isothermal filamentation [10] and permanent damage. Fig. 4 shows uniform distribution of pulsed (ESD) current and uniform temperature rise (due to self heating) across the device width till 40ns and filament formation (Fig. 4a) thereafter. This leads to significant temperature rise (Fig. 4b) and permanent damage of the device.

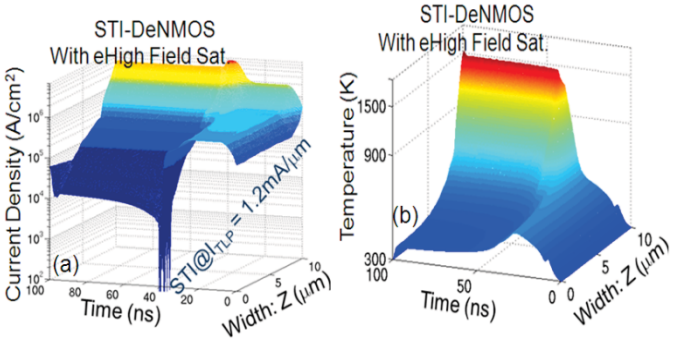

Figure 4: (a) Current Density and (b) Lattice temperature along the width of the device and extracted underneath the drain diffusion.

Fig. 5a compares transient evolutaion of drain voltage and lattice temperature extracted from 2D and 3D TCAD simualtions. It clearly depicts a huge difference between 2D and 3D TCAD and the associated predictions. It shows that drain voltage collapses significantly just after the onset of current filamentation, however this behavior was absent in 2D TCAD environment. The collapse of drain voltage fits well with the experimental data as shown in Fig. 5b and validates the importance of 3D TCAD approch.

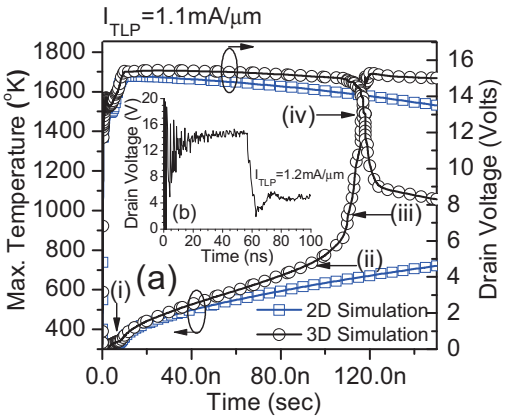

Figure 5: (a) Comparison of 2D and 3D transient characteristics of DeNMOS device extracted from 100ns (HBM) of ESD stress. (b) Measured transient characteristics (drain voltage w.r.t. time), which matches well with the simulated (3D) characteristics and validates the 3D modeling approach.

B. *Thermal Filamentation*

Fig. 6 shows the simulated TLP charecteristics of ggNMOS device, which depicts the junction breakdown, It1, Vt1 and It2 points. Moreover, Fig. 7 shows current density and lattice temperature profile of ggNMOS device (under 100ns ESD stress) extracted from 3D TCAD simulations at I_{TLP}~It2 (Fig. 6). It shows a higher current density in a local region near to drain end and a localized hot spot close to the drain-body junction. Overall, it clearly depicts that 3D TCAD can easily capture the onset of thermal runaway (Fig. 7a) and associated temperature rise (Fig. 7b) or failure. It is worth menting that the device width was kept more than 5μm and device's inactive region was extended by ~3μm, in order to properly capture heat diffusion across the Si region.

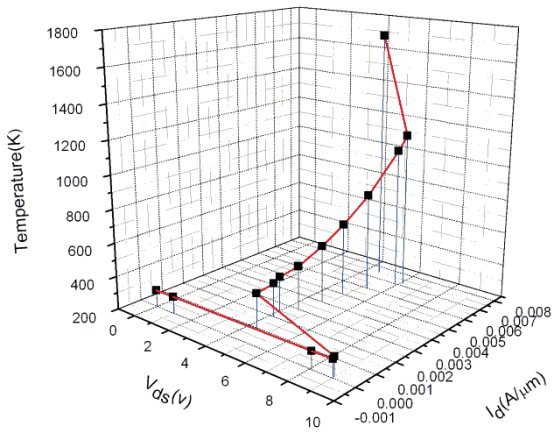

Figure 6: Simulated TLP charecteristics of ggNMOS device

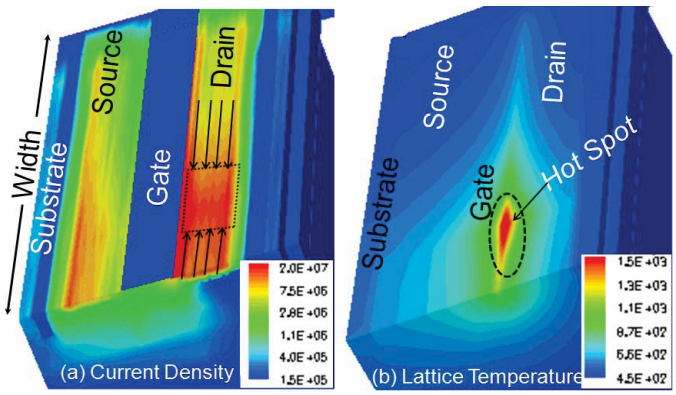

Figure 7: (a) Current density and (b) lattice temperature profile of ggNMOS device (under 100ns ESD stress) extracted from 3D TCAD simulations at I_{TLP}~It2

C. *Ultra Thin Body devices*

FinFET and ETSOI devices [15] are believed to be suitable candidates, which can replace planar bulk CMOS. In the existing industry trends, it is very important to have pre-silicon development of such novel devices. Since ESD is everywhere, it should also be considered during pre-silicon phase of any technology development. However, due to SOI substrate and ultra thin body, these devices require an extra effort in order to achieve close predictions. Fig. 8a shows experimental and simulated TLP characteristics of FinFET device with different channel lengths. It shows a very close fit between experiment and 3D TCAD simulation. A close fit eventually helps towards an accurate prediction of the cause for ESD failure (Fig. 8b). Fig. 8b shows hot spot at the drain-body junction which leads to FinFET device failure at higher ESD stress conditions. Since heat transport takes place primarily from the metal gate and interconnects in SOI structures, it is worth using thermal contacts in order to tune the thermal boundary conditions.

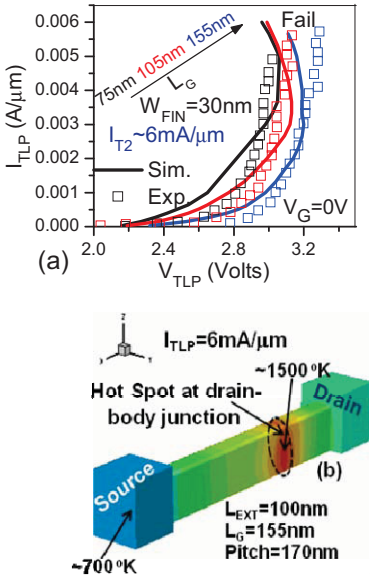

Figure 8: (a) Experimental and simulated TLP charecteristics of FinFET device, depicting a close fit between experiments and 3D TCAD. (b) Lattice temperature profile for FinFET device stressed under 100ns ESD conditions at I_{TLP}~It2.

D. *Moving Filaments*

Recently several investigations have been done on moving filaments in Drain extended MOS devices [16] [17]. It was found that ESD performance of drain extended MOS devices can be improved by achieving filament motion across the width of the device. However, such options are only possible by detailed 3D TCAD based studies- in order to predict (i) the physics of such events and (ii) available window for the optimization. Current density profile in Fig. 9 extracted from 3D TCAD simulations clearly shows moving filaments, which were recently observed in HRB-DeNMOS [17]. This work demonstrated TCAD based optimization of standard DeNMOS device in order to achieve moving filaments.

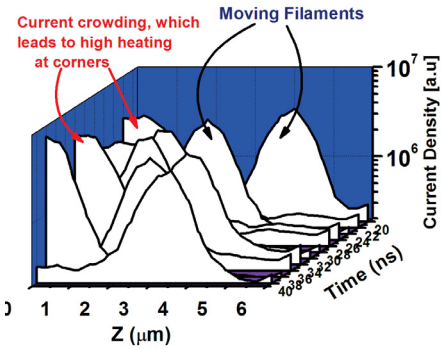

Figure 9: Current density profile extracted from 3D TCAD simulations, which clearly shows moving filaments in HRB-DeNMOS.

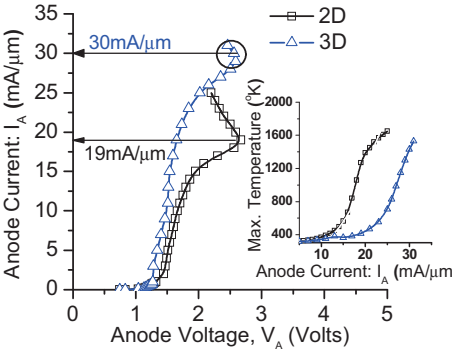

Figure 10: TLP characteristics of a SCR device extracted from 2D and 3D simulations.

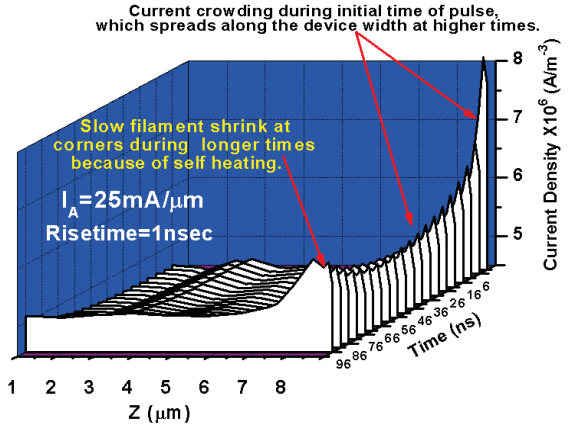

Figure 11: Current density profile extracted from 3D TCAD simulations, which clearly shows on-state spreading of current filament during the ESD stress condition.

E. *On State Spreading or Spreading Filaments*

Devices like SCRs show on-state spreading of current filaments. This is due to weak turn-on of parasitic PNP in the SCR path. Fig. 10 shows TLP characteristics of an IGBT plugged SCR device [14] extracted from 2D and 3D TCAD simulations. Fig. 11 shows current density profile, which shows spreading filaments in IGBT-SCR device. Fig. 10 shows that 2D simulation underestimates the It2 value, which is attributed to lack of on-state filament spreading and tight thermal boundary conditions (i.e. higher heating) in 2D simulations.

V. CONCLUSION

In this paper, we demonstrated a 3D TCAD based approach for the evaluation and failure analysis of nanoscale devices in advanced CMOS technologies. This approach will greatly help towards the robust development of novel ESD protection concepts in the pre-silicon phase of any technology node. We demonstrated the impact of various physical models and parameters on the accuracy of predicted ESD figures of merit. Moreover, we also discussed a range of device options and associated physics, which can be evaluated from 3D TCAD.

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