On the Failure Mechanism and Current Instabilities in RESURF Type DeNMOS Device Under ESD Conditions

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***Abstract*- We present 3D device modeling of RESURF or non-STI type DeNMOS device under ESD conditions. The impact of base push-out, pulse-to-pulse instability and electrical imbalance on the various phases of filamentation is discussed. A new phenomenon called "week NPN action" and the cause of early and fast failure is identified. A modification of the device is proposed which achieved an improvement of ~5X in failure threshold (I_{T2}) and ~2X in ESD window without degrading its I/O performance.**

***Index Terms*- DEMOS, ESD Failure, space charge build-up, Filamentation, pulse-to-pulse instability.**

I. Introduction

Shallow Trench Isolation (STI) and non-STI type *Drain extended MOS* (DeMOS) devices, used for high voltage I/O applications, have been found to be extremely vulnerable to ESD events. In order to improve the behavior of these devices under ESD conditions, there have been several attempts from various groups which provide an insight into their failure mechanism [1]-[4]. Recently it has been proposed that carrier heating in the high-field region influences the saturation velocity and the impact ionization, triggering a regenerative NPN action which causes the second breakdown [5]. Space charge limited current leads to filamentation and device failure [6-7]. Regenerative turn on of parasitic NPN causes a short circuit power dissipation leading to a failure [8]. Further, a complete understanding of various phases of filamentation and the final thermal runaway has been discussed for STI type DeNMOS devices [9]. However, a complete picture of the transient device behavior during base push-out with an understanding of the various phases of filamentation based on 3D simulation studies is still missing for RESURF (or non-STI) type DeNMOS, which is needed for improving its ESD behavior in order to design robust I/O devices.

II. Device Description And Simulation Results

Before we discuss the simulation results, it is worth mentioning that in order to capture the current filamentation, we created physical non-uniformity along the device width in the following way: (i) Non-Uniform contact strip i.e. Multiple contacts with unequal spacing between different contact holes or Single contact strip having width less than the total device width and (ii) Single sided termination (along the width) of device with a dummy STI. A triangular meshing scheme was used with a grid size resolution less than 200nm along the Z-axis. This simulation study was performed for silicide blocked RESURF type DeNMOS devices with thin gate oxide, as shown in Fig. 1, in a typical state-of-art 65 nm node CMOS technology. A well-calibrated process/device simulation deck was used as discussed in our previous work [9].The advantage of RESURF device over STI-DeMOS is its better R_{ON} v/s V_{BD} performance and smaller gate length, which provides a higher current driving capability and less gate-oxide capacitance. In order to model filamentation and device failure mechanism, this work extensively utilizes systematic 3D device simulations. This device can be used in two ways (i) I/O driver or (ii) high-voltage ESD clamp.

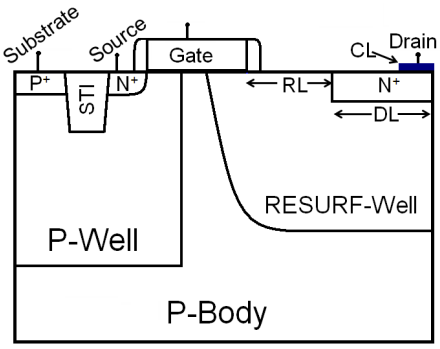

Fig. 1: RESURF DeNMOS device structure (*Type 1*).

The RESURF device has a good electrical performance in order to meet the I/O driving capability, however the device has shown only a low ESD robustness (Fig. 2 and 3). These reliability issues make the RESURF device less attractive as an output driver or power clamp. Fig. 3 shows that the devices with a larger width are prone to early failures, i.e. just at the onset of base push-out driven snapback.

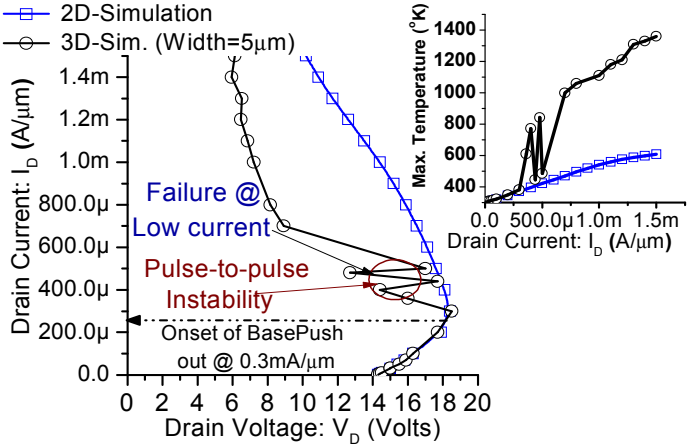

Fig. 2: Simulated (2D and 3D) TLP characteristics of RESURF DeNMOS under HBM like ESD condition. Width in 3D simulation is chosen to 5 µm. 3D simulations are done with single contact strip.

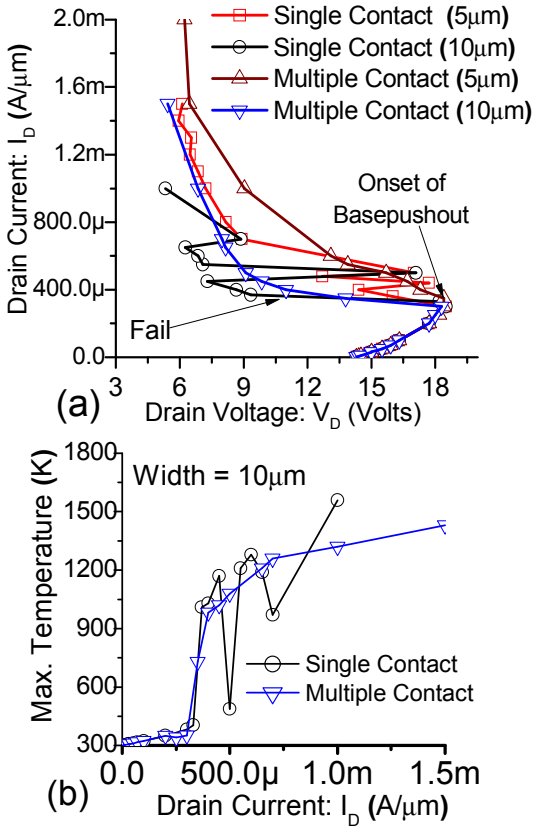

Fig 3: (a) Simulated TLP characteristics (HBM) of single contact strip and multiple contact strip devices with different widths. Devices with higher width fail at the onset of base push out driven snapback. (b) Shows Temperature rise with increasing TLP current for device with width = 10μm.

Two different states (i.e. pulse-to-pulse instability) were observed in TLP characteristics (Fig. 2 and 3), which is attributed to different locations of current filament along the device width. After the formation of current filamentation, i.e. after base push-out, we found that only very few bipolar keeps turned on along the device width. For most of the pulses (Fig. 4b & 4d), device leads to a filament formation at any one of the corners and causes deep snapback (low resistance state).

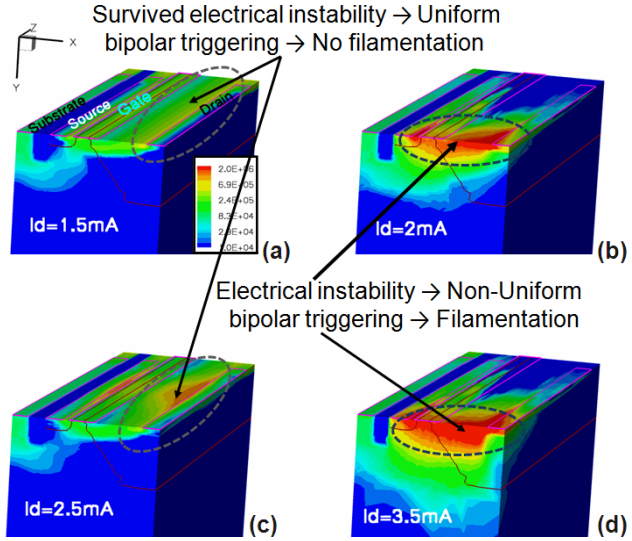

Fig. 4: Current density plot (A/cm^2). Figure describes two different conditions- (i) uniform bipolar triggering along the width and (ii) non uniform triggering or current filamentation (Width=5μm).

However, for a few pulses, NPN triggers uniformly across the device width (Fig 4a & 4c) and causes no significant filamentation or snapback (high resistance state). Fig. 5 shows that pulse-to-pulse instability was observed for slow HBM pulses, whereas it was absent for fast pulses. It is worth mentioning that we have observed these pulse-to-pulse instabilities for various cases, i.e. device with different widths, device with different contact scheme (Fig. 2 & 3) and for different rise time of the TLP pulse. This validates that the observed pulse-to-pulse instabilities have some physical significance and are not due to some numerical inaccuracies. Figures 3,6 & 7 summarize the device behavior: (i) The junction breakdown occurs at a very low current followed by a parasitic bipolar triggering at 0.1mA/μm. The device fails at even higher currents, which proves that the parasitic bipolar turn-on is not the dominant cause of device failure unlike to the proposed model in [2][4][8] (ii) The onset of base push-out at 0.3mA/μm which leads to a deep snap back (iii) Fig. 6 (b & d) shows that the current leading to filamentation after the base push out, which causes a localized (along the width) hot spot under the drain diffusion. This is leading to significant temperature rise, which can eventually cause the device failure for higher width devices. Whereas in smaller width device it is visible in the form of lower resistance state. In contrast, when the device survives filamentation (a & c) or when the filament forms in the center of the device, the temperature is quite relaxed along the width and leads to high resistance state. **(iv)** Fig. 7 shows that when the filamentation occurs (b & d), the device shows an even higher carrier modulation in the localized region along the device width, which is named as "localized base push-out" in the later sections.

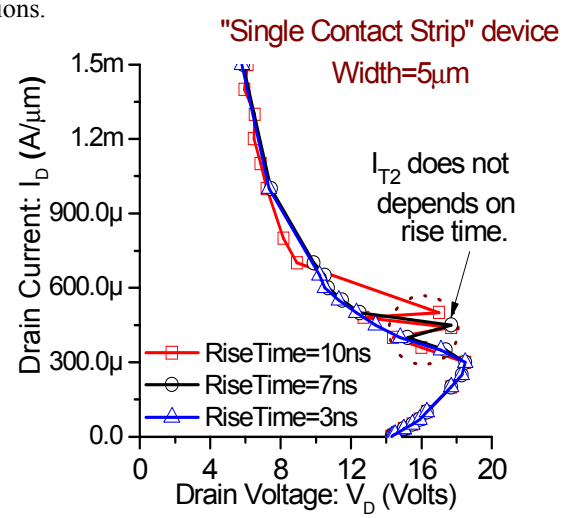

Figure 5: Dependence of simulated TLP characteristics on rise time (or pulse shape). Pulse-to-pulse instability depends on rise time of pulse, eventually on pulse shape.

III. Physics Of ESD Failure

Before we discuss the ESD failure mechanism, it is worth pointing out the failure criterion used in this work. Fig. 2 and 3 shows a significant rise in the temperature just after the base push out driven snap-back. This is due to the current filamentation and hot spot formation. Furthermore, it also shows that temperature rise for device with larger width (Fig.

3, 10µm device) is significantly higher compared to device with smaller widths (Fig. 2, 5µm). For ex: @ I_{TLP} = 0.4mA/µm, when width was increased from 5µm to 10 µm, maximum temperature inside the hot spot increases from 800K to 1200K respectively. Another simulation (data not shown here) for device with 15µm width @ I_{TLP}~0.35mA/µm shows temperature greater than 1600K at 100ns. These observations are due to the following fact- We found that the cross-sectional diameter of current filament does not changes with the device width. Due to this, device with higher widths leads to increased current density inside the filament, which eventually attributes to larger temperature rise inside the hot spot. Due to the very huge TLP simulation time required for device with width ≥ 15µm, we have restricted our studies to device with width = 10µm. In this way, the onset of current filamentation, i.e. the onset of base push-out is defined here as the failure point.

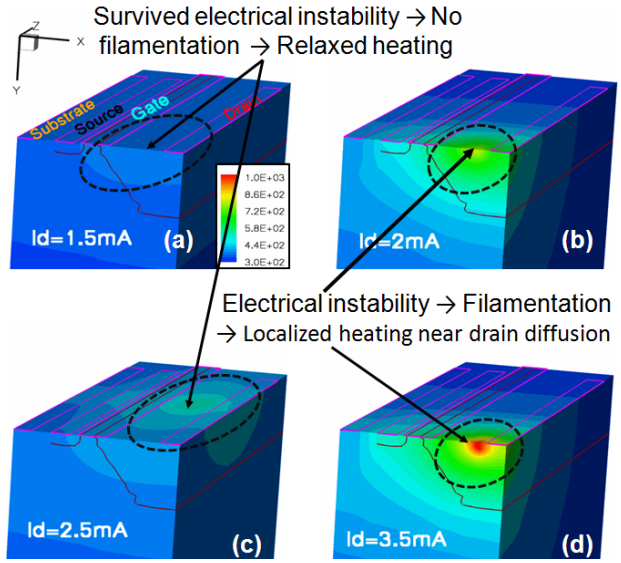

Fig. 6: Lattice temperature plot (K). Self heating in the device under two different conditions. (i) Relaxed temperature when bipolar triggers uniformly and device survived electrical instability, (ii) localized heating after current filamentation. (Width=5µm).

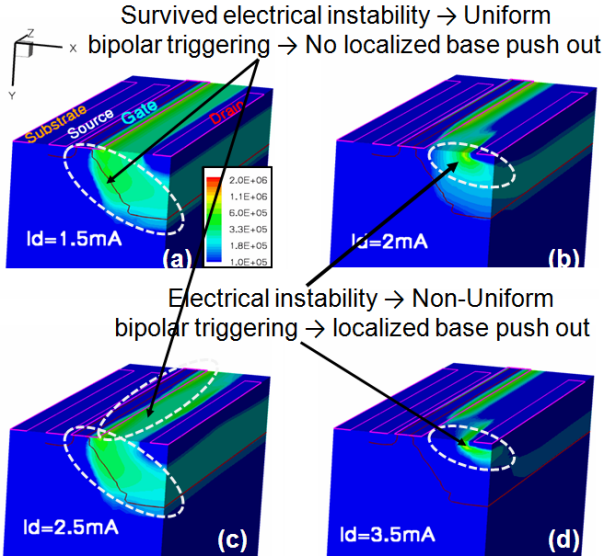

Figure 7: Electric field (V/cm) plot (Width=5µm) at different TLP level. Figure shows uniform bipolar triggering after base push out in 2D plane for few pulses (Fig. 7a and 7c), whereas filament, shrink at the corner, (Fig. 7b and 7d) leads to higher carrier modulation (causes deep snapback) for other pulses.

Figures 4c-4d, 6c-6d and 7c-7d differentiate the device behavior under two different conditions- (i) almost uniform bipolar triggering along the width and filament formation in the center of the device and (ii) non-uniform triggering or current filamentation at any one of the corners of the device. Furthermore, Fig. 8 illustrates the failure model of the device.

(i) *Onset of base push out*, which causes snapback. This happens at ~ 0.3mA/mm, at which the carrier concentration in the drain extension region exceeds the background doping.

(ii) Base push-out in the 2D plane causes snapback, which may lead to an *electrical instability*. If the device survives this instability, current flows almost uniformly along the width without any significant temperature rise.

(iii) Deep snapback because of the base push out-driven electrical instability which leads to a lower Impact Ionization (II) generated carriers, making it less efficient in triggering the distributed parasitic bipolar along the width. Such a *non-uniform bipolar triggering* causes the current to shrink (filamentation) at any one of the corner along the width and leads to significant temperature rise inside the localized hot spot. We refer to this phenomenon as "*Week NPN action*".

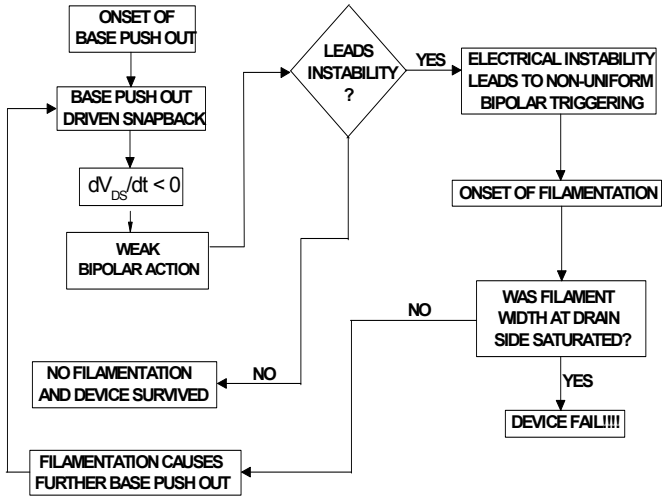

Fig. 8: Flowchart representation of current filamentation and device failure model.

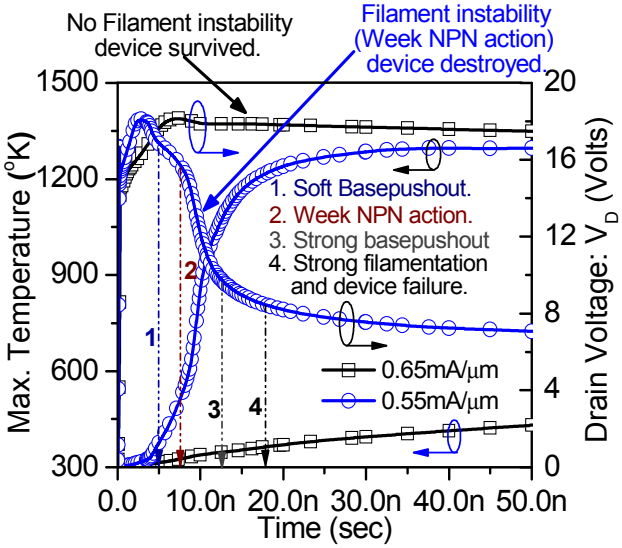

Fig. 9: Figure shows voltage drop because of base push out and early heating. Also describes various phases of filamentation.

(iv) Increased carrier/current density in a localized region along the device width due to the onset of current filamentation leads to further carrier modulation in that localized region (i.e. *localized base push out*) and causes further shrink of the current filament in a way similar to (iii).

(v) Week NPN action, localized base push out and current filamentation act as positive feedbacks to each other, eventually leading to a very fast and dense filament formation (within 2-3ns) causing early device failures (Fig. 9).

IV. Validation Of Failure Model

It was claimed in the past that these devices gets fail due to the regenerative triggering of parasitic bipolar [5][8]. As discussed in [9], drain hole current is the direct measure of excess carrier generation, which leads to regenerative NPN triggering. Fig. 10 shows the absence of regenerative NPN (i.e. significantly small amount of drain hole current) action after the base push out, different from previously reported works [5][8]. Fig. 9 also shows that when the device survives an electrical instability, there is no significant voltage drop and temperature rise, whereas in the presence of electrical instability temperature rises significantly with a simultaneous drop in the potential within a very short time.

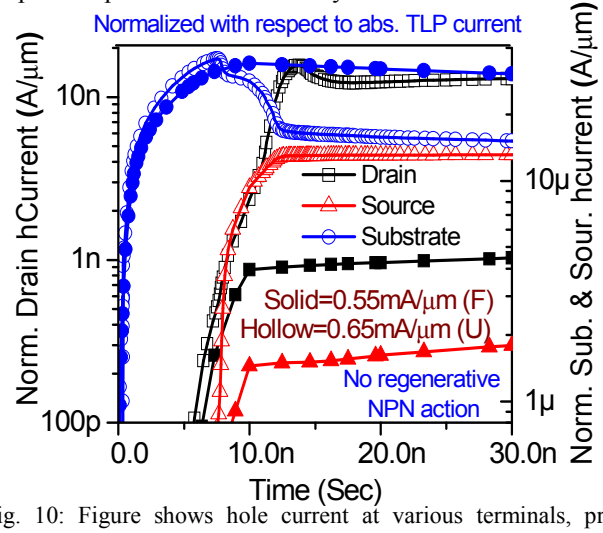

Fig. 10: Figure shows hole current at various terminals, proves absence of regenerative NPN action. (Markers: F→Filamentation and U→Uniform)

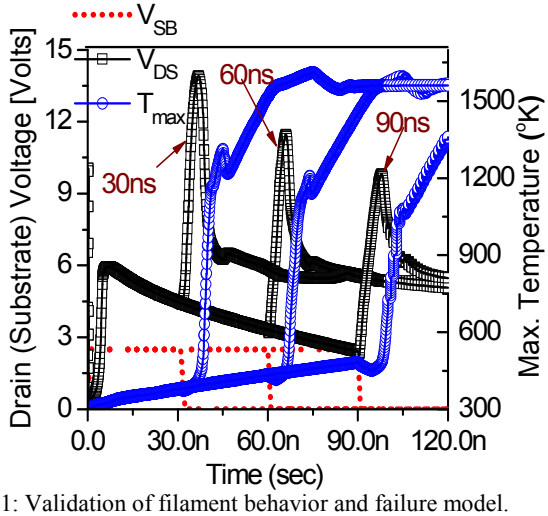

Figure 11: Validation of filament behavior and failure model.

Fig. 11 validates the failure model and the time evolution. It shows that when parasitic bipolar is triggered using an external substrate bias, there is no electrical instability and temperature rise. On the other hand, when the substrate bias is removed, the device goes into a filamentation and elevated temperature because of the electrical instability. Fig. 12 shows that the device failure occurs because of filamentation even under CDM like conditions.

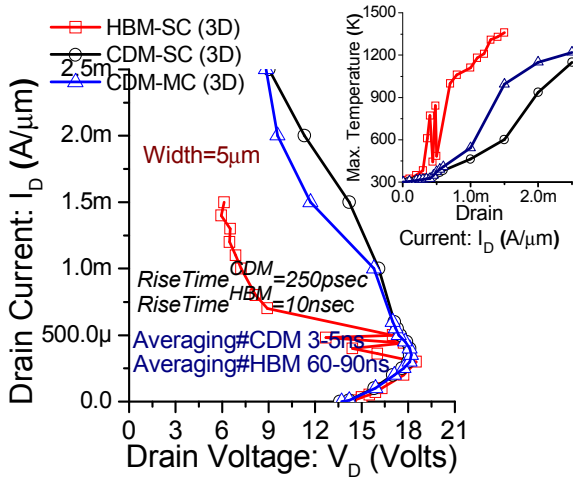

Fig. 12: Simulated HBM and CDM characteristics (TLP). Figure shows early failure even under CDM conditions. Inset shows significant heating under CDM time domain. (Markers:- SC→Single contact strip and MC→Multiple contact strip).

V. Device Modification And Performance Improvement

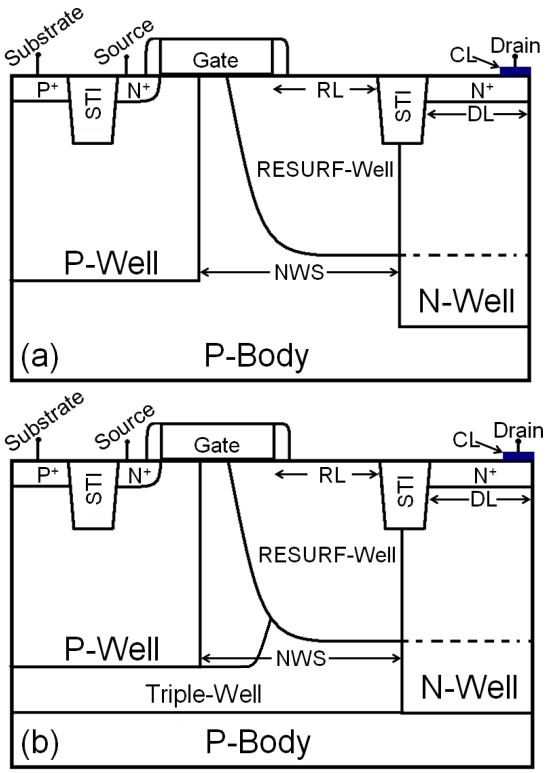

Fig. 13: Various modified RESURF DeMOS devices. (a) Device with extra STI and N-Well -"*Type 2*" (b) Further modified device with added triple well- "*Type 3*".

In order to improve the device ESD robustness, modifications are required which should ideally push the onset of base push out to higher current levels. Furthermore, the mixed signal performance of the device should not be sacrificed while incorporating any changes. Fig. 13 shows the modified RESURF device where an extra n-well implant far from the p-well to RESURF-well junction is added, which increases the onset of base push out by increasing the background doping. A STI region is also added which pushes the current deep into the n-well and RESURF-well in order to overcome the electrical instability. Since the STI and n-well implant exist in the standard sub 100nm node CMOS technologies, the modified device has no extra processing cost.

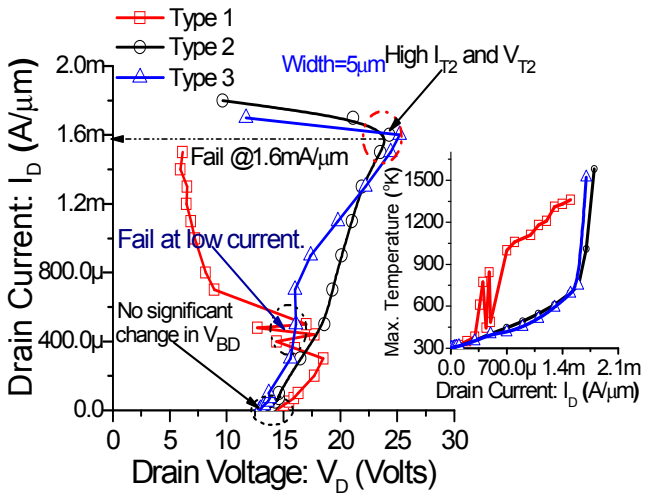

Fig. 14: Comparison of simulated TLP characteristics of standard and modified RESURF devices. Modified RESURF device show higher I_{T2} and ESD window.

Figure 14 shows that the modified device has a significantly improved ESD performance and from TABLE-I one can see that the R_{ON} v/s V_{BD} performance is degraded only by about 10%, which is still in the optimum range [10]. This performance improvement is attributed to the absence of base push out.

TABLE I

DIMENSIONS AND SIMULATED ELECTRICAL PERFORMANCE PARAMETERS OF VARIOUS INVESTIGATED DEVICE TYPES.

Device types & Dimensional Parameters							Electrical Performance			
Device Number	Device Type	RL (nm)	DL (nm)	CL (nm)	NWS (nm)	X (nm)	R_{ON} (KΩ/µm)	V_{BD} (V)	V_{T2} (V)	I_{T2} (mA/µm)
1	1	500	375	200	NA	NA	3.8	14.3	6.1	0.4
2	1	500	775	200	NA	NA	3.9	14.4	6.3	0.4
3	1	900	375	200	NA	NA	4.9	14.4	7.6	0.4
4	2	500	500	200	900	200	5.2	14	19.3	1.8
5	2	800	500	200	900	200	4.8	14	27	1.7
6	2	500	500	200	800	200	4.8	13.8	21	1.7
7	2	500	500	200	700	200	4.5	13.5	24.3	1.6
8	3	500	500	200	900	200	4.7	13	24.4	1.5
9	3	500	500	200	800	200	4.5	13	25.2	1.6

V. CONCLUSION

We found that the filamentation is caused by the electrical instability at the onset of base push out. The degree of confinement and the rate of filament formation strongly depends on the existence of week NPN action. The regenerative NPN triggering is shown to be absent even at higher currents (and temperature) and the bipolar turn-on is therefore not the dominant cause of device failure. Further a modified-RESURF DeNMOS device is proposed with an extra N-Well and STI region near the drain diffusion in order to avoid the base push out, which improved the ESD window by a factor of ~2X and the failure threshold by a factor ~5X. The proposed modification has been shown to not degrade the R_{ON} v/s V_{BD} performance and has no extra processing cost.

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