IGBT PLUGGED IN SCR DEVICE FOR ESD PROTECTION IN ADVANCED CMOS TECHNOLOGY

Mayank Shrivastava[1], Jens Schneider[2], Ruchil Jain[1], Maryam Shojaei Baghini[1], Harald Gossner[2], V. Ramgopal Rao[1]

[1]Center for Nanoelectronics, Department of Electrical Engineering, Indian Institute of Technology-Bombay Mumbai-400076, India, mailto:mayank@ee.iitb.ac.in; mailto:rrao@ee.iitb.ac.in
[2]Infineon Technology AG, P.O. Box 80 09 49, D-81609 Munich, Germany, mailto:Harald.Gossner@infineon.com

Abstract: *We have proposed modifications in the standard SCR structure to inherently improve quasi static triggering voltage, transient overshoot and trigger time without changing its failure threshold and holding voltage. The device is an useful option for the protection of low voltage interfaces and power domains in advanced CMOS reaching from 1 V to 3.6 V.*

I. INTRODUCTION

Silicon controlled rectifiers (SCRs) are used as highly efficient ESD protection elements because of their *high failure thresholds* (30-40mA/μm), *low holding voltage* (1-2 volts) and *very low on resistance*. Along with these figures of merit, when SCR device protects the gate oxide, the ESD performance is also determined by the time dependent dielectric breakdown (TDDB). This makes the *transient voltage overshoot* and *trigger time* as crucial parameters. To protect the gate oxide in sub 100nm node technologies, having thickness below 2nm, modifications in existing SCR structures and their triggering mechanism are required.

Transient behavior of diode triggered SCRs during ESD event is discussed in [1]. The trigger time was found in the range of 4 ns for current pulse having rise time equal to 1ns. Though this work gives an idea on the optimization parameters and transient behavior of current filament, a detailed study to improve the device performance is required. Also the solution for unwanted transient overshoot, which may give rise to a TDDB failure, was not addressed. Other works [2] [3] discuss the design factors which can improve the turn-on-time of SCRs during CDM events. For forced TLP pulses having rise time of 250ps the best achieved trigger time was 500ps. The impact of optimization parameters on HBM event, where the device fails because of self heating at higher time scales, has not been explored. Also the unwanted transient overshoot has not yet been solved. Low Voltage Triggered SCRs (LVTSCR) were previously reported by different groups [3], but this device was also not able to solve transient overshoot related problems. The work discussed in [4] explored the voltage overshoot behavior of SCR devices and proposed specific trigger circuit level solutions for controlling transient overshoot.

In this work, we have proposed modifications to the standard SCR structure ***to inherently improve the quasi static triggering voltage, transient overshoot and trigger time by maintaining the high failure thresholds and low holding voltages***. The device is an useful option for the protection of *low voltage interfaces* and *power domains* in advanced CMOS reaching from 1 V to 3.6 V. The device is fully compliant with an advanced CMOS process.

II. PROPOSED STRUCTURE AND ITS ADVANTAGES

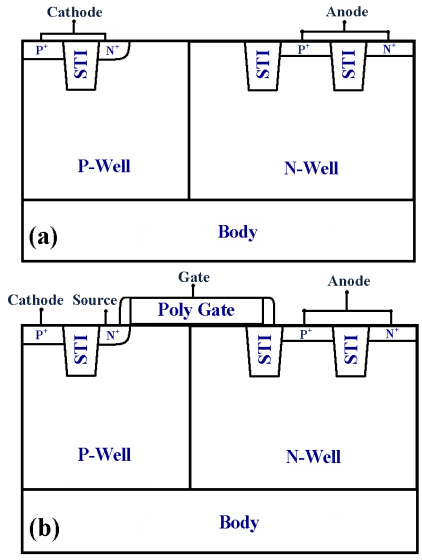

Figure 1: Standard SCR devices.(a) LSCR and (b) MLSCR

To understand the operation of the improved SCR it is compared with the basic SCR structures of *Lateral Silicon Controlled Rectifier* (LSCR) and the Modified LSCR (MLSCR) devices (Figure 1 (a) and (b)), respectively. Figure 2 (a) and (b) respectively show the proposed Insulating Gate Bipolar Transistor plugged SCR (IGBT-SCR) device and its modified version (HRB-IGBT-SCR) with a highly resistive body and a single "halo implant" near the source region. Equivalent circuit of proposed device is also shown in figure 2(b).

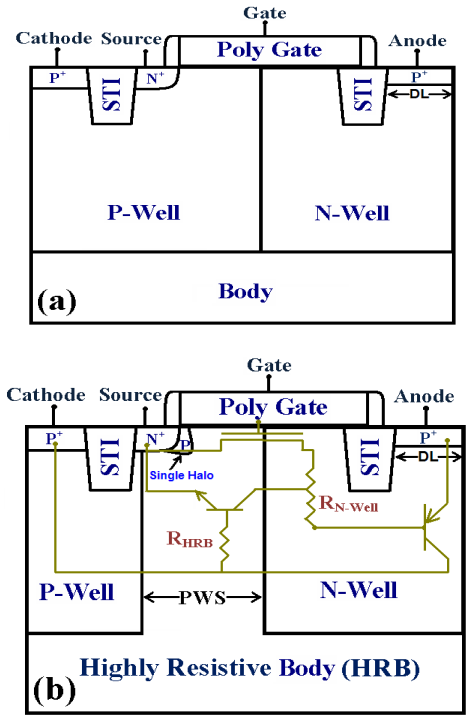

Figure 2:(a) Proposed IGBT plugged SCR device (IGBT-SCR) and (b) IGBT plugged SCR device with high resistive body and Single Halo (HRB-IGBT-SCR).

The proposed device has two modifications (i) floating N-well region and (ii) highly resistive P-body along with single halo. Following are the various advantages of proposed modifications by which the triggering speed of both PNP and NPN devices embedded in the proposed structure can be improved.

1. Floating N-well region: In the first step the N-Well contact is removed [5], which enhances the turn-on of the PNP. After the formation of channel in the presence of gate bias, excess carriers appear in N-Well. In MLSCR device the channel current, which causes excess carriers in N-Well during initial transient, drift out from N-well contact, which may be connected to some external triggering circuit or to the anode (P^+ contact) of the SCR device. Because of the fast drift of excess carriers from N-Well, it does not help in improving the trigger behavior of PNP. Making a floating N-Well helps in accumulating the excess charge carriers in the N-Well region (base of PNP), which actually improves the triggering property of embedded PNP in the proposed IGBT device. Further we have also shown that accumulation of excess carriers in floating N-Well leads to a highly capacitive nature of device for higher voltages at anode which eventually helps in skewing the transient overshoots.

2. Highly resistive P-Body and Single halo: Triggering speed of NPN device is proportional to β (beta) of transistor, which depends on the emitter-to-base electric field (defines the drift nature of excess carriers from emitter to collector) and base doping (defines the recombination in base). Incorporating a single halo implant forms graded base in NPN device, which causes a high electric field at the emitter-base junction. This improves the drift of carriers from emitter to base, which in turns improves the bipolar gain. Similarly a highly resistive body or very low body (base) doping helps in reducing the excess carrier recombination in base improving the bipolar gain. Also, since the NPN triggering occurs by impact ionization (II) generated holes, highly resistive body helps in raising the body potential even in the presence of very less number of II generated holes, eventually leading to a fast bipolar triggering. It is worth mentioning here that there is no V_T adjust implant used for the proposed device and the subthreshold leakage is also controlled by halo implant, hence blocking the halo implant is not acceptable and the combination of HRB-SH should always be used in order to improve the triggering speed of NPN.

III. SIMULATION SETUP AND RESULTS

The devices were realized and simulated using well calibrated process and device simulation decks [6][7]. Transmission Line Pulsing (TLP) characteristics are extracted by transient device simulations for Human Body Model (HBM) as well as Charge device Model (CDM). In order to extract pulsed (TLP) I-V characteristics, various current pulses with current values ranging from few µA/µm up to several mA/µm were applied at anode terminal. The applied current pulses have rise time of 10ns and pulse duration of 150ns (250ps and 5ns respectively for CDM). Further the voltage value extracted from transient simulation was averaged between 60ns-90ns and 2ns-5ns for HBM and CDM respectively. The gate triggering was

achieved by applying a trigger voltage pulse with a rise time of 0.5ns, pulse time of 10ns (0.1ns and 1ns respectively for CDM) and peak voltage up to 1.5volts at gate terminal, whereas the source and cathode terminals were grounded. Applied trigger pulse was selected based on the RC trigger circuit discussed in [8], with time constant of 0.1ns and 0.5ns. In order to mitigate the unwanted turn on because of dV/dt effect, a dual base triggering circuit similar to the one proposed in [9], can be used. In this case the third inverter can be removed and the output of second inverter is connected to the gate of proposed HRB-IGBT-SCR device. Capacitance values were derived by small signal AC simulations using Sentaurus device TCAD tool. The subthreshold current was the dominant leakage component in the device under grounded gate condition. The total leakage current through the device was ~1E-11A/µm under normal operating condition, which is significantly less than diode triggered SCR but slightly higher than dual base triggered SCR [9].

1. Device performance: Figure 3 shows the simulated Transmission Line Pulsing (TLP) characteristics of proposed devices and its comparison with respect to the existing SCR devices in grounded gate configuration.

In the absence of gate bias, the proposed device as well as the standard SCR's triggering takes place because of junction breakdown. As shown in figure 4(a), at very low currents, the conduction takes place because of junction breakdown. On the other hand, figure 4(b) shows a very high electric field at low currents which results in a device triggering because of junction breakdown.

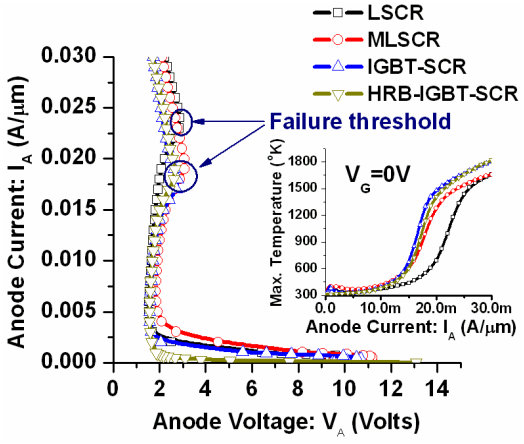

Figure3: TLP Behavior of various device in gate grounded configuration (V_G=0V).

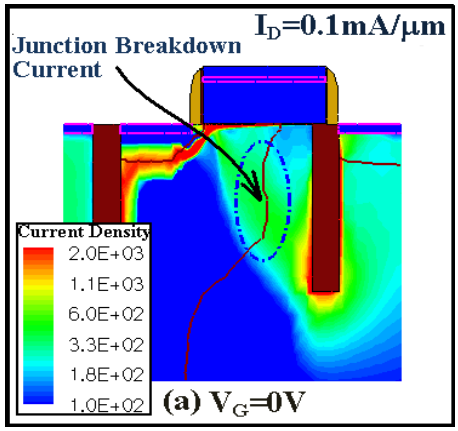

Figure 4 (a): Figure shows current flow in HRB-IGBT-SCR is dominated by Junction breakdown.

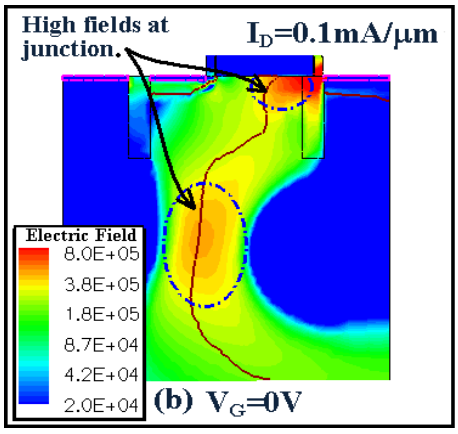

Figure 4 (b): Figure shows high electric field (V/cm) at Well Junction in HRB-IGBT-SCR .

Figure 5 shows the TLP characteristics of various devices in the presence of gate trigger pulse. Triggering voltage of all the devices is quite different. It shows that standard SCRs have a higher triggering voltage compared to the proposed IGBT device.

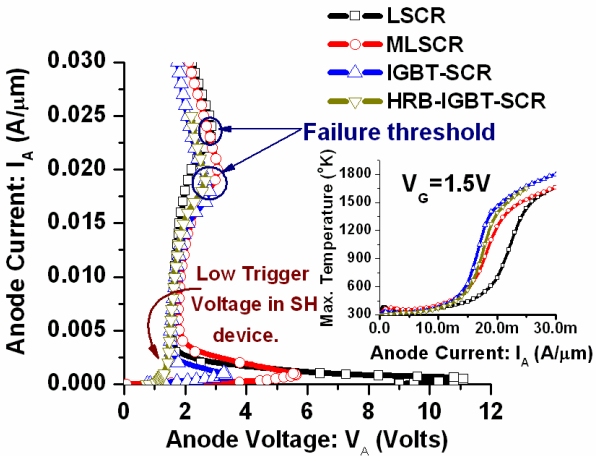

Figure 5: TLP Behavior of various device in presence of gate triggering (V_G=1.5V).

Figure 6(a) shows the dominance of current flow because of channel conduction irrespective of junction current as shown in figure 4(a). Because of channel current, triggering of SCR happens at low anode voltage. Low junction fields as shown in figure 6(b) also proves the absence of junction breakdown in the presence of gate triggering. The very low triggering voltage observed for the proposed IGBT-SCR device as compared to MLSCR is because of the floating N-Well region. The excess carriers because of channel conduction accumulate in the N-Well region, which eventually lowers the potential across the base of PNP causing a faster PNP triggering at low anode voltage. MLSCR device does not take full advantage of gate triggering because part of excess carriers drift out of the N-Well contact (N+ connected with anode). The modified HRB-IGBT-SCR shows triggering voltage lower than IGBT-SCR device. This is attributed to the effect due to the highly resistive body and single halo at source side as discussed in the previous section.

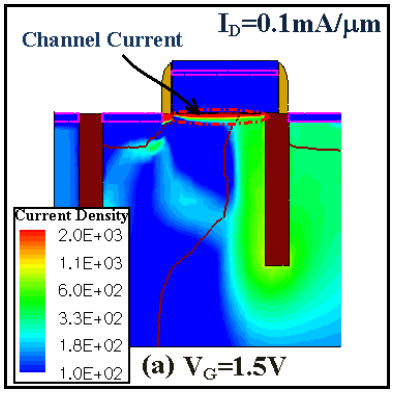

Figure 6 (a): Figure shows current flow in HRB-IGBT-SCR is because of channel conduction.

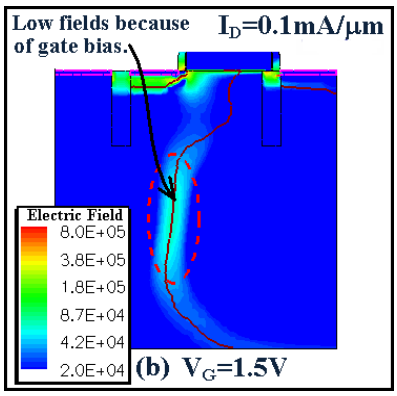

Figure 6 (b): Figure shows low electric field (V/cm) at well Junction in HRB-IGBT-SCR because of gate bias.

2. Transient behavior and self protection from transient overshoot: Figure 7 shows the transient performance of various devices. The MLSCR device has a slow triggering (~8nsec) as compared to standard SCR (~6nsec), whereas the proposed IGBT-SCR exhibits a faster triggering (~2nsec) as compared to MLSCR and standard SCR because of floating N-Well region. The HRB-IGBT-SCR device shows a very fast triggering behavior (~0.2nsec) as compared to other devices because of floating N-Well, highly resistive body and single halo. Since all the device parasitics are incorporated in the TLP simulations, we expect accurate modeling of overshoot behavior. It is also clear from transient characteristics that overshoot voltage in case of HRB-IGBT-SCR device is quite low as compared to other devices. This behavior is attributed to a very high anode capacitance inside ESD design window as shown in figure 8. The anode capacitance of HRB-IGBT-SCR increases exponentially with respect to the anode voltage inside ESD window where as the anode capacitance during normal operation is quite less and is comparable to other devices. The high capacitive nature in ESD window helps in skewing transient overshoot, which blocks the transient voltage to go beyond the ESD window. The highly capacitive nature of IGBT devices is because of excess carrier accumulation inside the N-Well in the presence of the gate triggering. IGBT-SCR device shows an exponential rise in anode capacitance beyond ESD design window, i.e. at even a higher anode voltage as compared to HRB-IGBT-SCR. This is the reason why a highly capacitive nature is not visible for IGBT-SCR device in figure 8. Reduced triggering voltage and self protection from transient overshoot will help in designing robust protection concepts with low ESD resistance (R_{ESD}), which can eventually improve the RF performance of I/O (input-output) circuits.

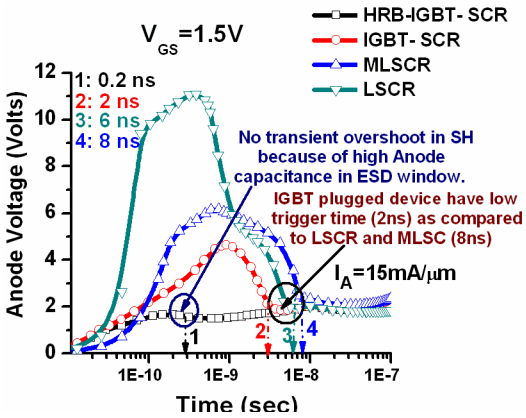

Figure7: Transient Behavior of various devices in presence of gate triggering (V_G=1.5V).

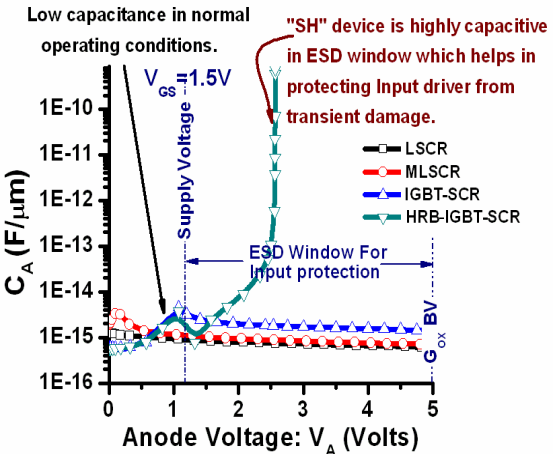

Figure 8: Capacitive Behavior of various device in presence of gate bias (V_G=1.5V).

3. Failure threshold: Based on the peak temperature of 3D (1500°K) device simulation, the failure threshold of standard SCR was extracted as 22mA/μm while it amounts to ~18mA/μm for the HRB-IGBT-SCR. The reduced failure threshold as compared to standard SCR is attributed to a gate bias induced excess heating [10]. Figure 9 shows the hot spot location. The heating takes place at anode (P^+) to N-Well junction because of high current density and junction field. The failure threshold can be increased to ~30mA/μm by increasing the dimensional parameter DL (figure 2), which relaxes the current density at the anode (P^+) to N-Well junction.

4. Gate bias: Figure 10 shows that the gate bias equaling the threshold voltage is sufficient for efficient triggering of the proposed device. The property of efficient triggering at low gate bias may help in designing robust RC triggering circuits for transient biasing the gate terminal.

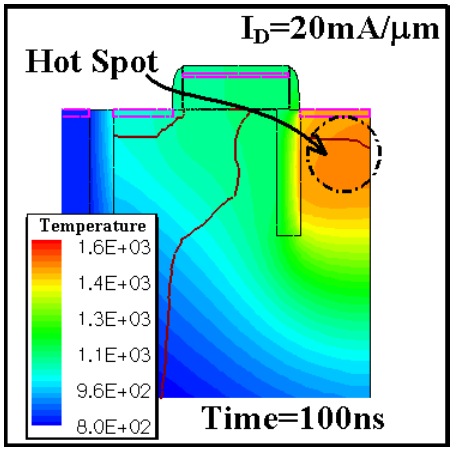

Figure 9: Figure shows (Lattice Temperature in °K) high heating at Anode and N-Well Junction (HRB-IGBT-SCR), which eventually leads to device failure.

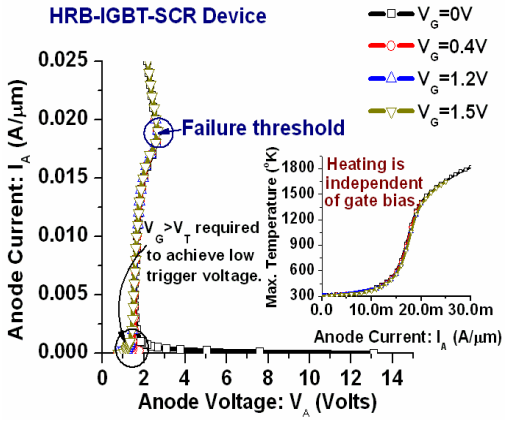

Figure 10: Impact of gate bias for HRB-IGBT-SCR device.

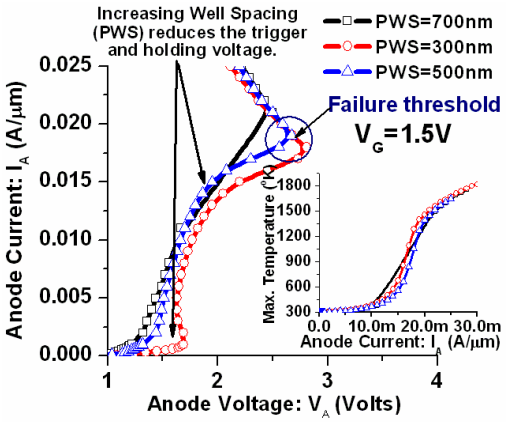

Figure 11: Impact of N-Well to P-Well spacing on trigger and holding voltage in HRB-IGBT-SCR device.

IV. IMPACT OF DIMENTIONAL PARAMETERS

1. P-well to N-Well Spacing (PWS): Figure 11 shows the impact of P-Well to N-Well spacing on triggering and holding voltage. Reducing the well spacing decreases the body resistance near source, which eventually leads to weak triggering of parasitic NPN. Also, parasitic NPN loses its graded base nature by reducing well spacing, which causes a lower β (bipolar current gain), eventually leading to a high holding and trigger voltages.

2. Anode diffusion length (DL): Figure 12 shows that increasing the diffusion length improves the failure threshold. This behavior is attributed to relaxed current density at anode by increasing the diffusion length. Relaxed current density leads to a lower self heating and eventually to a high failure threshold. Figure 13 provides the anode capacitance for different DL values, which shows that the device loses its

skewing property (which was because of exponential rise in anode capacitance inside ESD window) for higher DL values. Figure shows that DL=600nm seems an optimal value for preserving the skewing property of the device along with achieving a high failure threshold (~25mA/µm). Later we have shown better prediction of achieved failure threshold (~30mA/µm) using 3D simulations.

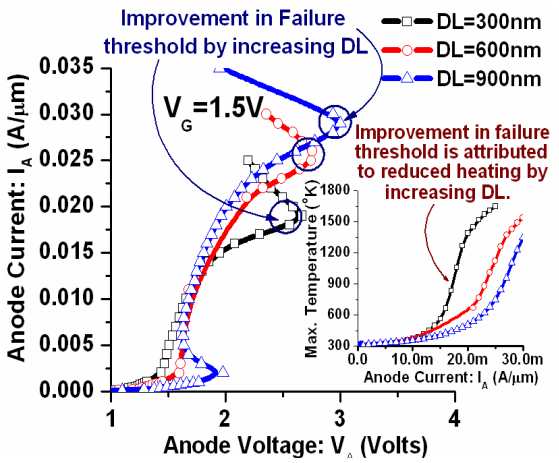

Figure 12: Impact of Drain Diffusion Length (DL) on failure threshold in HRB-IGBT-SCR device.

V. PERFORMANCE DURING ULTRA FAST ESD EVENTS

For effective protection of thin gate oxides during Charged Device Model (CDM) based ESD events, it is important to consider transient performance of devices during ESD events with fast rise times. Figures 14 and 15 show transient behavior of various devices with a rise time of 1ns and 250ps respectively. The results demonstrate a triggering time of 0.8ns and 400ps respectively for the proposed HRB-IGBT-SCR device.

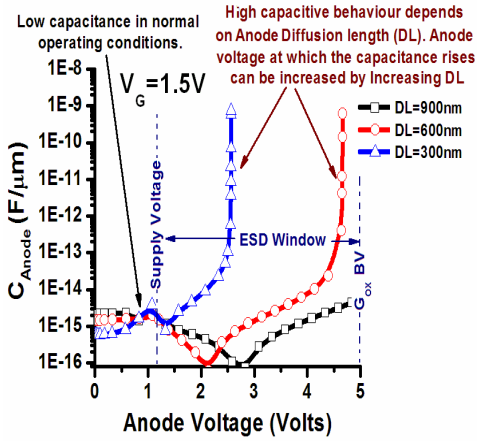

Figure 13: Impact of Drain Diffusion Length (DL) on highly capacitive nature in HRB-IGBT-SCR device.

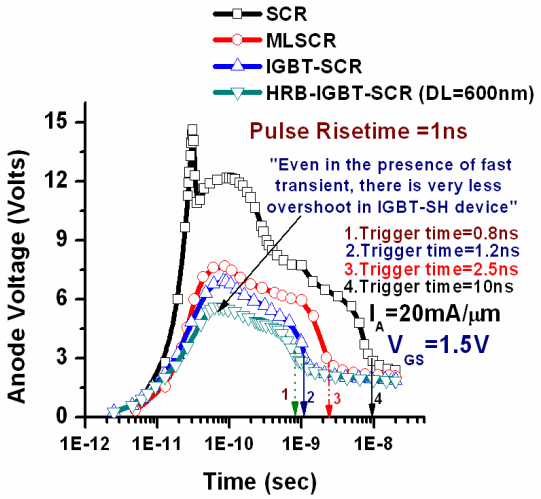

Figure 14: Transient performance of various devices during fast ESD event with rise time of 1ns.

Here, the ultra fast triggering of the proposed device, during CDM like ESD events, was achieved by simple gate triggering (RC trigger circuit), unlike the earlier reports [2][3][11]. This eventually saves extra design effort, chip area and I/O pad parasitics. Also the transient overshoots in the proposed device are less as compared to overshoot behavior of diode triggered SCRs presented in [2][3]. The TLP behavior for proposed structure during CDM like ESD event is shown in figure 16 which gives a foot print of robust ESD protection during the presence of fast ESD events.

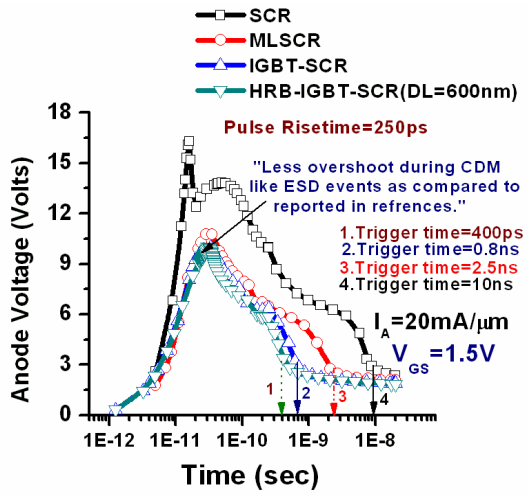

Figure 15: Transient performance of various devices during fast ESD event (CDM) with rise time of 250ps.

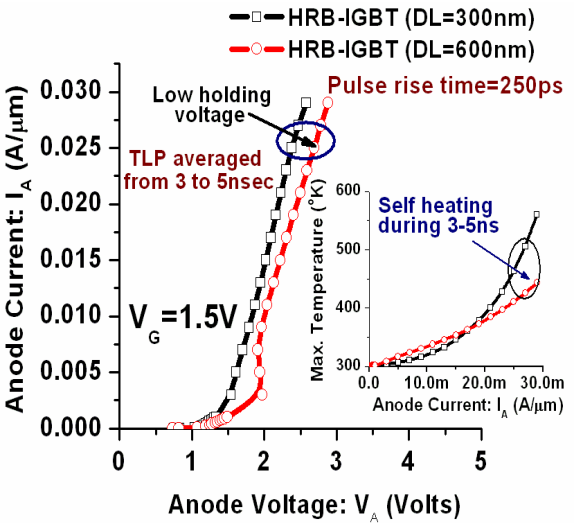

Figure 16: TLP performance of proposed device during fast ESD event (CDM) with rise time of 250ps.

VI. 3D BEHAVIOR

Figure 17 shows the simulated 2D and 3D TLP characteristics of proposed device for different DL values. The 2D simulation gives a lower prediction of failure threshold because of high self heating which was relaxed in the 3D device. The proposed device with DL=600nm, gives a failure threshold of 30mA/μm, which is in the acceptable range for sub 100nm node CMOS technology. We have shown that the proposed device with DL=600nm is robust in terms of triggering voltage, transient overshoot, trigger time and protection from ultra fast transients.

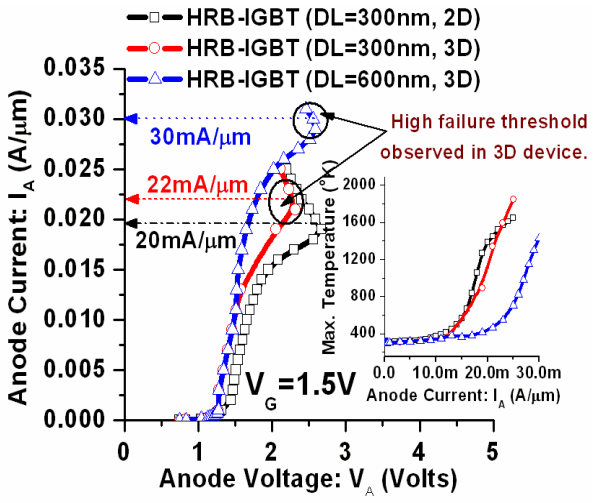

Figure 17: Comparison of 2D and 3D TLP characteristics of proposed device.

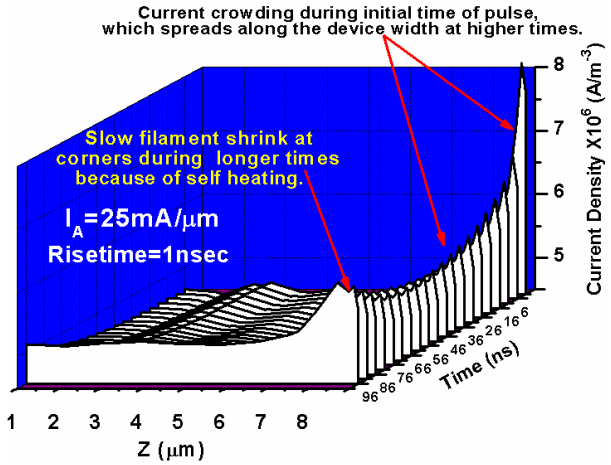

Figure 18: Current filament behavior along width in proposed device during 100nsec of HBM ESD event.

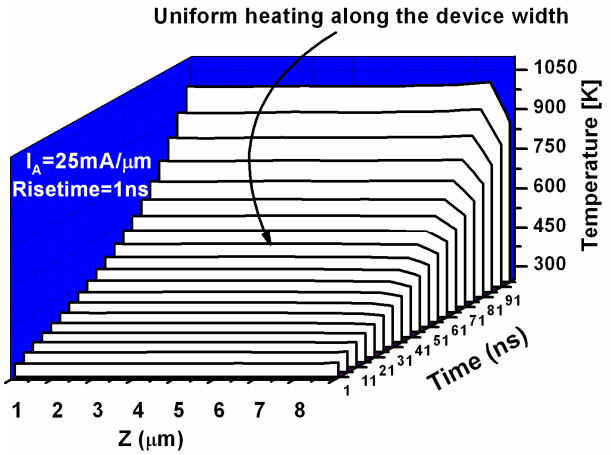

Figure 19: Self heating along device width in proposed device during 100nsec of HBM ESD event.

Figure 18 shows the filament nature in the proposed SCR device which is quite similar to the results presented in [1], up to 60nsec. Initially current shrinks at the corners, which further spreads along the device width. This behavior is attributed to non uniform SCR triggering along the device width during the initial time, which causes current confinement into a narrow region along the width. At moderate times (40-70 nsec) when there are sufficient number of excess carriers to trigger all the distributed SCRs along the width, the current starts to spread. The filament behavior for moderate times is in nice agreement with TIM's measurement presented in [1]. Figure 19 shows that the self heating in the device is uniform along the width for higher current densities. The uniform temperature distribution along the device width at all times (0-100ns) is attributed to the following behavior. For shorter time scales, when the current

density was non uniform along the device width, there was no significant self heating. However, for moderate time scales, because of uniform distribution of current along the width, the device can achieve a uniform self heating along its width. At higher times (80-100ns) there is an onset of current filamentation (fig. 18), which is attributed to significant temperature rise across the device.

VII. TRADE OFF: HOLDING VOLTAGE, OVERSHOOT AND TRIGGER TIME

ESD protection device with a low leakage, lower parasitics, smaller transient overshoot, higher failure threshold and an adjustable holding voltage is always a dream device for ESD engineers. Except for the adjustable holding voltage, the proposed device has shown significant improvement over other devices proposed in the literature. In order to find adjustability of holding voltage, we have done a few more investigations over the proposed device. Figure 20 shows that increasing the STI length underneath the gate-anode edge can help in tuning the holding voltage. This behavior is attributed to increased sheet resistance of N-Well region. It also increases the trigger voltage slightly which may solve the problem of unwanted latch-up in the device, whereas the inset of figure 20 shows that the increased holding voltage can be achieved at the cost of high trigger times. This behavior shows that there is always a trade-off among performance parameters of protection device. Nevertheless, the device with STI=300nm can be considered as an optimum device since the transient overshoot is not significant and it also provided a slightly higher holding and trigger voltages in order to overcome the latch-up related problems.

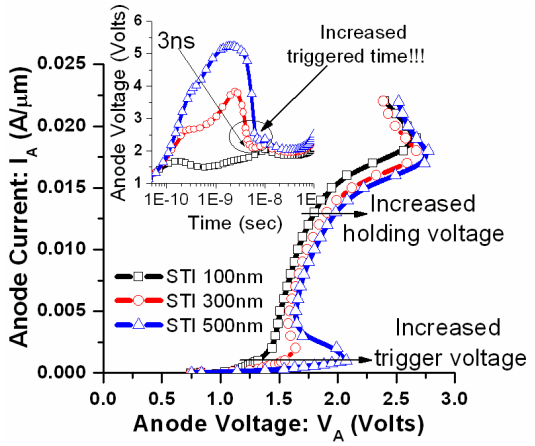

Figure 20: Impact of STI length or N-Well resistance over holding voltage, trigger voltage and trigger time. TLP curves are extracted from 2D simulations.

Further figure 21 shows the pulsed IV characteristics for three different cases. It should be noted that (i) removing the isolation between n+ source and p+ P-well contact (cathode) has no impact on holding voltage (ii) adding a diode chain (of 2 diodes) between cathode and ground does not show any increase in the holding voltage and (iii) incorporating a diode chain between source and ground leads to a shift in holding voltage without any increase in trigger time, but this approach causes a significantly higher trigger and holding voltages. This again shows a trade-off among the various performance parameters.

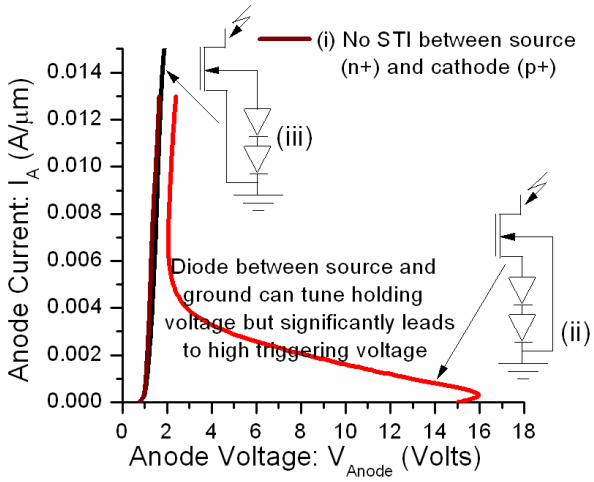

Figure 21: Figure shows three different investigated options in order to adjust holding voltage. (i) butted p-Well and source contact, (ii) diode chain between cathode and ground (iii) diode chain between source and ground.

VIII. AN ALTERNATIVE WAY TO TUNING THE HOLDING VOLTAGE AND ITS IMPACT

Figure 22 shows an alternative way for tuning the holding voltage by adding a resistance between source terminal and ground. Most of the current flows through source (emitter of NPN) of the device, once the SCR operation is triggered. Incorporating a resistance between the source and ground will lead to a rise in voltage at the source terminal. This eventually pulls-up the voltage at anode to higher values. Inset of figure shows that the proposed approach of tuning holding voltage does not degrade the trigger time and transient voltage overshoot. The gate is triggered by using a gate pulse similar to the one discussed in section III. At this stage it is worth mentioning that, in order to mitigate the unwanted turn on because of dV/dt effect, the trigger voltage can be increased by using a dual base trigger circuit

[9] in a way similar to the one discussed above in section III. The drawback of this approach is a slightly reduced failure threshold which is attributed to elevated self heating across the device.

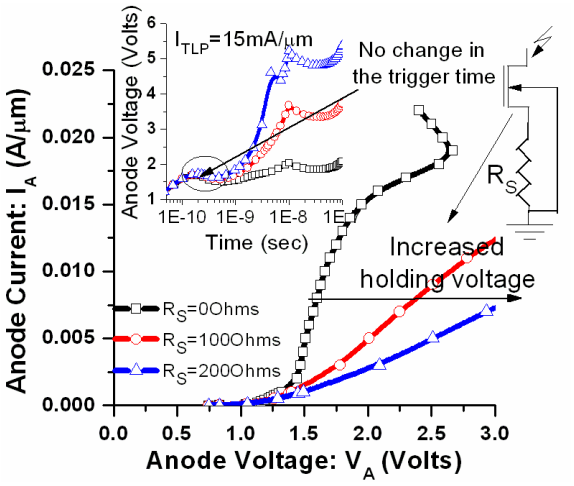

Figure 22: Figure shows the proposed way of tuning holding voltage and its impact over trigger time, trigger voltage and transient voltage overshoot.

IX. CONCLUSION

A novel highly resistive body IGBT SCR device combining excellent clamping behavior with low capacity per width represents a very attractive protection device choice for I/Os with a narrow ESD design window and sensitivity to parasitic capacitance. The trigger time is faster than 400ps and the transient overshoot is below 3V. The device exhibits a failure threshold of 30mA/μm and a holding voltage of 1-2Volts. The method for improving the bipolar property of both NPN and PNP building blocks of the SCR was discussed. The floating N-Well configuration improves the triggering property of embedded PNP whereas the highly resistive body and single halo nature of the device enhances the triggering property of NPN device. This results in a greatly improved triggering behavior of proposed SCR device when compared to the conventional configurations. It was found that exponential rise of anode capacitance in HRB-IGBT-SCR device helps to reduce the overshoot significantly. Also the anode width was found to be an important parameter to increase the failure threshold by preserving other advantages of the proposed device. The proposed device was also found to provide a good protection for the case of fast ESD events (i.e. CDM). 3-D device simulation results give a detailed insight of filament behavior and self heating in SCR device.

REFRENCES

[1] Kai Esmark, et. al., "Transient behavior of SCRs during ESD pulses", IEEE International Reliability Physics Symposium, 2008, pp. 247-253.

[2] James Di Sarro, et. al., "Study of design factors affecting turn on time of silicon controlled rectifiers (SCRs) in 90 and 65nm bulk CMOS technologies", IEEE International Reliability Physics Symposium, 2006, pp. 163-168.

[3] James Di Sarro, et. al. Evaluation of SCR-based ESD protection devices in 90nm and 65nm CMOS technologies", IEEE International Reliability Physics Symposium,2007, pp. 348-357.

[4] V. A. Vashchenko, et. al. "Voltage overshoot study in 20V DeMOS-SCR devices", Proceedings of EOS-ESD Symposium, 2007, pp. 53-57.

[5] T. Nikolaidis et. al. Electronics Letters, Vol 39, Issue 7.

[6] Mayank Shrivastava, et. al. "A new physical insight and 3D device modeling of STI type DeNMOS device failure under ESD conditions", IEEE International Reliability Physics Symposium, 2009, pp. 669-675.

[7] Mayank Shrivastava, et. al. "Highly resistive body STI NDeMOS: An optimized DeMOS device to achieve moving current filaments for robust ESD protection" IEEE International Reliability Physics Symposium, 2009, pp. 754-759.

[8] Sheng-Lyang Jang, et. al. "Novel diode chain triggered SCR circuit for ESD protection", Solid State Electronics, Vol 44, 2000, pp. 1297-1303.

[9] James Di Sarro, et. al., "A Dual-Base triggered SCR with very low leakage current and adjustable trigger voltage", Proceedings of EOS-ESD Symposium, 2008, pp. 242-248.

[10] Kwang-Hoon Oh, et. al. "Analysis of Gate-Bias-Induced Heating Effects in Deep-Submicron ESD Protection Designs", IEEE TDMR VOL. 2, NO. 2, JUNE 2002, pp. 36-42.

[11] C.J. Brennan et al., "Implementation of Diode and Bipolar Triggered SCRs for CDM Robust ESD protection in 90nm CMOS ASICs", Proceedings of the EOS/ESD Symposium, 2005, pp. 380-386.