Design Guidelines for Recessed Schottky Barrier AlN/GaN Diode for THz Applications

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***Abstract*— In this work, we have explored the design space for multifinger planar Schottky barrier diodes (SBDs) using AlN/GaN heterostructure for terahertz (THz) applications. Using a well-calibrated computational modeling framework, we have identified the critical design parameters and associated parasitic elements affecting diode's THz performance. The 3-D modeling of parasitics components has been deployed as the 2-D design approach overestimates the performance or underestimates the parasitic components in a multifinger design. Device design guidelines and the tradeoff between various parameters are discussed in detail. The optimum design space and related tradeoffs were found to be nonintuitive due to the presence of 3-D parasitics capacitances and resistances.**

***Index Terms*— AlN/GaN diode, GaN, high-electron-mobility transistor (HEMT) simulation, RF diode, Schottky diode, TCAD, terahertz (THz).**

I. Introduction

THz devices have found a range of applications in ultrahigh-speed communications, sensing, security screening, and various medical diagnostics. High-frequency Schottky barrier diodes (SBDs) are imperative to terahertz (THz) frequency detection, frequency multiplication, and mixing. The nonlinear characteristics of SBD are employed for various high-frequency applications mentioned above. The lack of minority carrier charge storage and relative simplicity in device fabrication makes SBD a preferred choice in THz systems. The low cut-in voltages of these devices enable them to operate as ideal rectifies, resulting in the detection of weak signals.

For long, GaAs-based SBDs have dominated the market mostly due to high mobility and its moderate bandgap. The demand for compact, fast, and reliable THz devices has increased significantly over the years. GaN-based heterostructures can be an excellent alternative due to high (∼20 times of GaAs devices) 2-D electron gas (2DEG) and electron mobility at the interface. In addition, a larger bandgap in GaN devices reduces the reverse leakage and improves the device's robustness even at high-temperature operating conditions.

The planer geometry-based SBDs have numerous advantages over the earlier whisker-based contact structures proposed for high-frequency applications [1]–[3]. Although the whisker-type contact has a low junction area, their integration and reliability are a major issue [4]. In order to mitigate this, several planar Schottky diodes have been reported in the literature [4]–[11]. The lateral Schottky diodes, first demonstrated by Peatman *et al.* [5], involve making a 1-D Schottky metal-2DEG contact. It significantly reduces the junction area, resulting in much lower contact capacitance (C) than the vertical counterpart. The higher concentration of 2DEG and excellent mobility minimize the series resistance (R) of the device. Both of these factors are extremely important for the design of any device operating at THz frequencies as the low RC product results in a significant gain in device performance. However, despite the distinct benefits of lateral SBD, their performance is far from the theoretical limits.

Most of the earlier studies on high-frequency SBD are based on AlGaAs/InGaAs/GaAs systems [4]–[7], [12] and there are only limited reports on lateral AlN or AlGaN/GaN-based THz diodes [8]–[10]. The first lateral diode based on GaN material was proposed in 2006 by Veksler *et al.* [8] for THz detection. Since then, few efforts have been made to improve the device performance. Cywiński *et al.* [9] optimized the epilayers to enhance the AlGaN/GaN Schottky diode performance in the sub-THz region. Shinohara *et al.* [11] demonstrated highly scaled multifinger planer SBD and reported a high cutoff frequency of 2.02 THz. However, the report does not probe into the entire design space of the THz diode device. The feasibility of GaN heterostructure-based SBD for sub-THz detector application is studied in [10]. The previous works are limited to exploring the viability of GaN-based SBD for THz or sub-THz applications, and none of the reports provides deep insights into the design of these devices or design guidelines to maximize the performance.

The planer, multifinger SBD topology looks most promising due to the ease of integration and high cutoff frequencies demonstrated. It is essential to explore the associated design parameters affecting the SBD performance at THz frequencies. TCAD simulations can provide significant insights into the impact of parasitic elements on device performance at high frequencies. The TCAD-based design approach substantially

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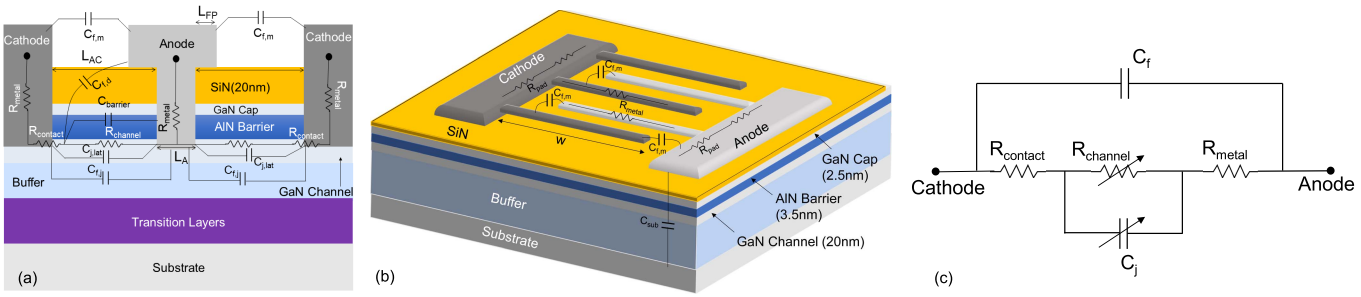

Fig. 1. (a) Cross-sectional schematic and parasitic components of AlN/GaN SBD simulated in this study. The area of T-shaped anode is 0.06 μm^2 and the metal resistivity is 2.4 $\times$ 10^{-8} Ω·m. (b) 3-D multifinger topology of planer diode. (c) Equivalent model of SBD.

reduces the design time as well as the cost. In addition, the performance of an individual device cannot be extrapolated to a multifinger topology. In reality, the potential drop across the metal lines as well as the fringing capacitance severely degrades the high-frequency performance. This is the first report on the design and engineering of multifinger THz SBD using TCAD computations. The study investigates the design metrics of AlN/GaN-based multifinger, lateral SBD, and proposes guidelines to maximize the performance for THz operation. We have presented a detailed analysis by studying the contribution of parasitic elements and the dependence on the multifinger design topology. This article is arranged as follows. Section II discusses the simulation framework adopted in this work. Section III presents the performance metrics of the THz SBD. Section IV discusses the impact of physical scaling on device RF performance. Sections V and VI present the impact of ohmic contact resistance and anode field plate on device cutoff frequency, respectively. Finally, Section VII concludes the work.

II. Simulation Framework

A. Computational Modeling

The computational TCAD framework used in this work has been derived from our previous works on high-electron-mobility transistors (HEMTs) [13]–[16] and AlGaN/GaN SBDs [17], [18]. We have studied the AlN/GaN-based SBD, adapted from experimental work reported by Shinohara *et al.* [11]. The device cross-sectional schematic is presented in Fig. 1(a). Polarization charge is computed using polarization models presented in [19], and the same has been accounted for all the heterointerfaces. Surface traps are considered at the SiN passivation and GaN cap interface as the origin for the channel 2DEG.

Cathode metal contact is formed with an ohmic contact resistance of 0.02 Ω·mm to match the experimental conditions. In order to capture the accurate transport across the Schottky interface, anode is modeled as a nonideal contact. Various donor-/acceptor-like trap states are present at the metal–semiconductor interface, incorporated during the device processing. These dangling bonds alter the localized energy band level and impact the carrier transport. We have modeled the anode contact interface by accounting for: 1) thin ($\sim$5 Å) interfacial oxide layer; 2) discrete energy levels in energy band gap due to nitrogen vacancies; and 3) continuum of trap states due to surface dangling bonds. The detailed aspects of interface modeling in SBD are discussed in our earlier work [18]. The breakdown simulations are done using the impact ionization model following Chynoweth's law [20]. The corresponding device calibration is shown in Fig. 2 and discussed in following section.

B. Device Calibration and Simulation Methodology

The lateral diode cross section and topology studied in this work are shown in Fig. 1(a) and (b), respectively. The total diode width is represented by $W = n \times w$, where W is the total number of anode fingers and w refers to the width of each finger. It is imperative to account for metal resistance as a function of device width and a number of fingers to extract the true device performance. However, the TCAD simulation of a 3-D multifinger structure is computationally expensive. In order to accurately capture the physical effects of 3-D simulations, we carried out mixed-mode 2-D simulations by accounting for the metal line resistance. It is achieved by dividing the planer multifinger geometry in a discrete set of diodes devices and corresponding series resistance, as shown in Fig. 3(a). The multifingers can be seen as a number of parallel diodes connected via metal lines. The series resistance for each discrete device increases in proportion to metal finger length as we move away from the anode/cathode pad. This network can be equivalently converted to a single anode finger ($n = 1$) topology by calculating the effective resistance per unit length of the metal line, as shown in Fig. 3(b). This effective resistance (R_n) is a function of the number of metal lines and is calculated using the below expression [21]

$$R_n = \frac{\rho . W}{3n^2 A} \tag{1}$$

where ρ is the metal resistivity, W is the total width of the metal lines, n is the number of metal fingers, and A represents the cross-sectional area of contact. The anode metal resistance as a function of n calculated from the above equation is shown in Fig. 4(a). The width of each diode is chosen to be 10μm such that the voltage drop across this length of metal line is negligible under forward bias conditions. For example, if the device width is 200 μm, a total of 20 diodes are connected in parallel with resistors R_n in accordance to Fig. 3(b) and mixed-mode simulations are carried out.

The simulation results are calibrated against the experimental data presented in [11]. Fig. 2(a) shows the diode forward

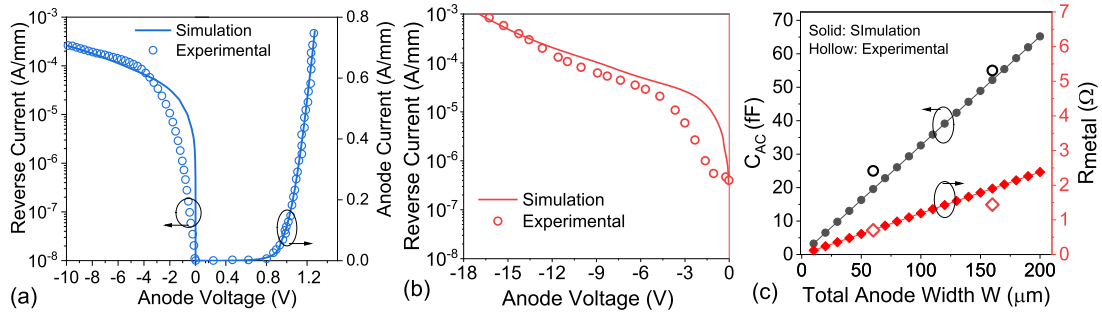

Fig. 2. (a) Diode's forward and reverse *I–V* characteristics depicting match between the experimental and simulation data. (b) Calibration of reverse breakdown characteristics of SBD. (c) Diode total capacitance and metal finger resistance as a function of device width for $n = 4$. The modeled data have been calibrated with the experiments [11].

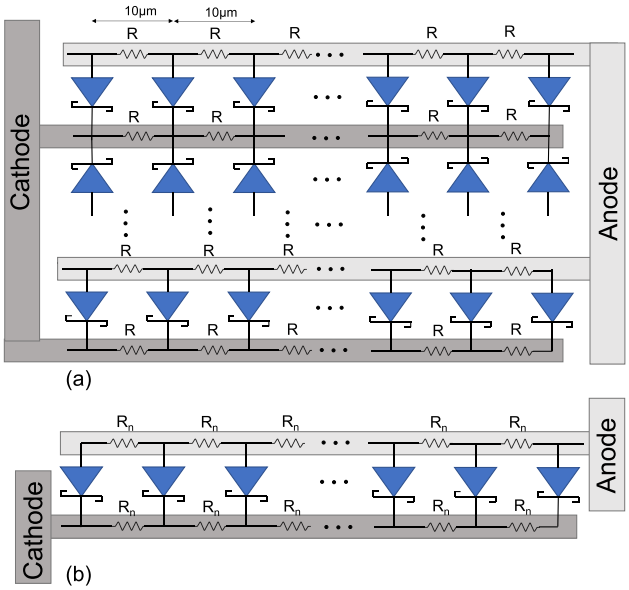

Fig. 3. (a) Distributed resistors model of the multifinger diode structure. (b) Equivalent single anode finger model simulated using TCAD.

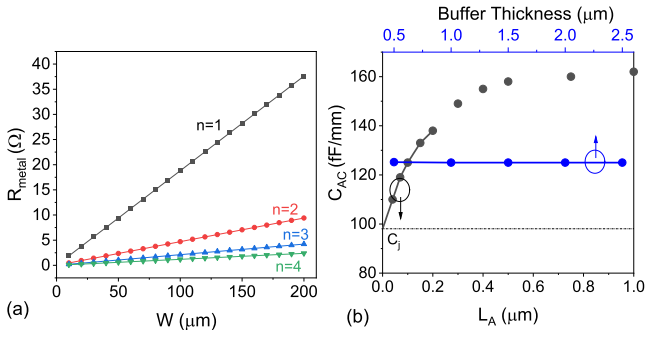

Fig. 4. (a) Anode metal resistance as a function of device width for different number of metal fingers (n). (b) Total capacitance (C_{AC}) as a function of buffer thickness and junction length (L_A). The lateral junction capacitance component is independent of L_A. However, the fringe capacitance component (C_{fj}) increases with anode area.

and reverse *I–V* characteristics. The reverse breakdown calibration is shown in Fig. 2(b). Similarly, Fig. 2(c) shows the calibration of total capacitance between anode and cathode terminals (C_{AC}) and the parasitic metal resistance (R_{metal}) as a function of device width for $n = 4$. Detailed discussion on these parasitic elements and their impact on device performance has been presented in the following section. The accurate physical device modeling and calibration provide a reliable simulation setup to make a fair prediction of device behavior. The same has been achieved in this study, as presented in the following. The anode recess is formed such that the metal extends 20 nm below the GaN/AlN interface for making a lateral contact with 2DEG. Anode-to-cathode length (L_{AC}) and anode metal length (L_A) are considered to be 70 nm unless specified otherwise.

III. THz SBD: Performance Metrics

The performance of various THz circuits, such as mixers, frequency multipliers, and detectors, greatly depends on the device characteristics. For instance, the conversion loss in the case of a mixer is a strong function of diode parasitics that leads to performance degradation at high frequencies. Hence, it is imperative to identify the parasitic elements and then define a performance figure of merit that can be employed to understand various design tradeoffs. The most widely adopted performance metric is the cutoff frequency (f_c) determined by the series resistance and diode capacitance as [22]

$$f_c = \frac{1}{2\pi R_{\text{series}} C_{\text{AC}}}. \tag{2}$$

The parasitic resistive and capacitive components in case of the planer SBD are shown in Fig. 1(a) and (b) and it is represented by an equivalent circuit model in Fig. 1(c). The total series resistance of the diode (R_{series}) can be described as follows:

$$R_{\text{series}} = R_{\text{channel}} + R_{\text{contact}} + R_{\text{metal}}. \tag{3}$$

A. Parasitic Resistance

The three components of device parasitic resistance are discussed in the following.

1) Channel Resistance ($R_{channel}$): The intrinsic diode resistance represented by R_{channel} is a function of applied voltage and 2DEG carrier density. Scaling down the channel length is an effective measure to lower the channel resistance, but the associated tradeoffs need to be studied. The AlN barrier results in a higher polarization charge at the interface compared to

the AlGaN barrier. Hence, the 2DEG carrier density in AlN barrier devices is much higher. It can be further enhanced by using epigrowth optimization such that the number of defects is minimized and higher 2DEG concentration is obtained. However, from the device design perspective, the channel resistance cannot be reduced below a minimum value limited by the net polarization charge at the interface.

2) Contact Resistance ($R_{contact}$): The ohmic contact resistance is given by R_{contact}. The contact resistance becomes a vital component as the device is scaled down, and the channel resistance falls proportionally. It is mostly determined by the choice of the metal stack and the processing conditions. Various techniques such as regrowth have been employed to reduce the contact resistance to very low values [11]. The ohmic contact regrowth techniques require complex and additional growth processes. Hence, while designing the devices, it is important to understand the magnitude of performance improvement rendered by minimizing the contact resistance. As we observed in our studies, the contribution of the contact resistance component is correlated with the device width and the number of metal fingers.

3) Metal Resistance (R_{metal}): In the case of planer diode, another crucial parameter is the resistance of the metal fingers depicted by R_{metal}. As the devices are scaled-down, the thickness of metal fingers is also reduced, resulting in a significant metal resistance contribution that surpasses the other parasitic resistance components. The metal resistance is strongly dependent on the number of fingers and the width of each metal line. This aspect has never been explored in the previous works. The anode/cathode metal pads connecting the anode/cathode fingers, respectively, have large areas. Hence, the resultant metal pad resistance component (R_{pad}) as shown in Fig. 1(b) does not contribute significantly to the total resistance and can be neglected.

B. Parasitic Capacitance

The total capacitance (C_{AC}) consists of the Schottky junction capacitance (C_j), the parasitic fringing components (C_f), and the substrate capacitance (C_{sub}). It can be written as

$$C_{\text{AC}} = C_j + C_f + C_{\text{sub}}. \tag{4}$$

The junction capacitance is independent of the anode area due to lateral contact to 2DEG. The fringe capacitance is contributed by the metal lines ($C_{f,m}$), passivation dielectric ($C_{f,d}$), barrier layer ($C_{f,\text{barrier}}$), and vertical anode junction ($C_{f,j}$), as shown in Fig. 1(a). It is desired to minimize the anode contact area to reduce the fringe capacitance, as shown in Fig. 4(b); however, it can adversely affect the series resistance, degrading the device frequency performance. Similarly, aggressive device scaling can substantially increase the fringe capacitance. Therefore, it is essential to study these tradeoffs to find an optimized design window. The substrate capacitance component does not have a significant contribution in submicrometer channel length devices. The same has been shown in Fig. 4(b) that the total capacitance (C_{AC}) does not vary as a function of buffer thickness.

IV. Impact of Device Scaling

The carrier transport in case of lateral SBD is parallel to the heterointerface; it enables a significant advantage of scaling down the device length (L_{AC}) to reduce the carrier transit time. However, a deeper investigation is required to understand the effective impact on the device cutoff frequency. The reduction in channel length does not necessarily cause linear improvement in the device's high-frequency performance. The contribution of various parasitic elements needs to be evaluated. In this section, we have discussed the impact of the anode-to-cathode length (L_{AC}) scaling and anode junction length (L_A) scaling.

A. Anode Junction Length

The cutoff frequency (f_c) is inversely proportional to the product of parasitic resistance and capacitance. Minimizing the anode length (L_A) results in a proportional decrease in the junction area, which in turn lowers the anode fringe capacitance ($C_{f,j}$), as shown in Fig. 4(b). However, it should be noted that the reduction in anode metal length (L_A) adversely impacts the diode series resistance. This tradeoff requires further investigation as a function of the number of metal fingers.

Fig. 5(a)–(d) shows the cutoff frequency as a function of anode metal length (L_A) and device width for $n = 1$–4, respectively. The following observations are made from the analyses.

1) The cutoff frequency for smaller device widths increases as the junction length is reduced. However, as the device width is increased, the improvement subsides due to dominating metal line resistance.
2) f_c degrades as a function of device width significantly faster for short junction devices than long junction devices. This is attributed to increased metal resistance, which is much higher for smaller junction devices as the device width is increased. It counteracts the improvement due to smaller vertical anode fringe capacitance ($C_{f,j}$) shown in Fig. 4(b).
3) The f_c roll-off as a function of device width is mitigated as the number of metal fingers is increased from $n = 1$ to $n = 4$. It also increases the design space for obtaining THz operating frequencies. A higher number of metal lines reduce the effective series resistance of the diode, as shown in Fig. 4(a).

The corresponding anode current for the same set of design parameters is shown in Fig. 5(e)–(h). Diode forward bias current is another design parameter that affects various performance figures of merits, such as conversion loss in a mixer circuit. We extracted the diode anode current at $V_{\text{AC}} = 1.4$ V, for all the cases mentioned above. We observe that the diode current increases linearly as a function of device width for long junction devices. However, for narrow junction, the device current saturates at lower device widths. This effect is more pronounced for $n = 1$ and gradually subsides as the number of fingers is increased to $n = 4$. The high metal resistance in narrow junction devices degrades the device current.

In order to find an optimized design window, we must evaluate both high-frequency and dc performance parameters.

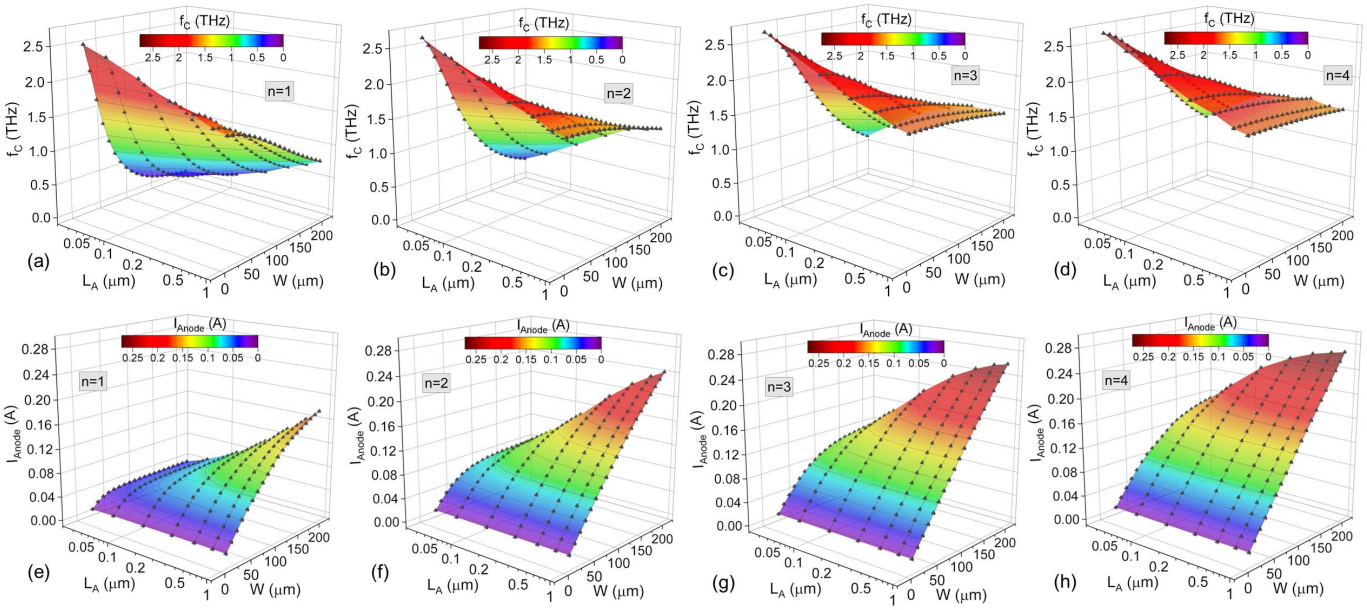

Fig. 5. Cutoff frequency (f_c) and anode current variation as a function of junction length (L_A) and device width (W) for (a) and (e) $n = 1$, (b) and (f) $n = 2$, (c) and (g) $n = 3$, and (d) and (h) $n = 4$. Channel length is fixed at $L_{AC} = 70$ nm.

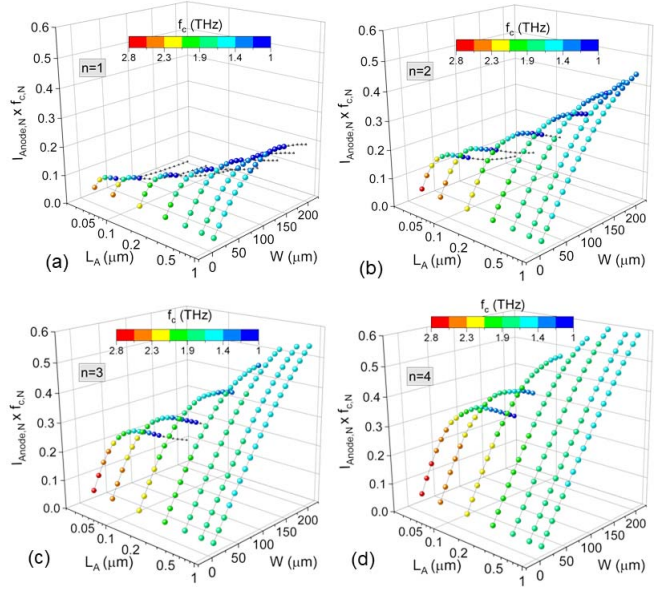

Fig. 6. Normalized cutoff frequency and anode current product ($f_{c,N} \times I_{\text{Anode},N}$) as a function of junction length (L_A) and device width (W) for (a) $n = 1$, (b) $n = 2$, (c) $n = 3$, and (d) $n = 4$. Channel length is fixed at $L_{AC} = 70$ nm.

Hence, we extracted the normalized product $f_{c,N} \times I_{\text{Anode},N}$, as plotted in Fig. 6(a)–(d). The data points with cutoff frequency ≥ 1 THz are also represented to select the device with high $f_{c,N} \times I_{\text{Anode},N}$ product and desired operating frequency. The observations are discussed as follows.

1) In case of narrow junction devices, we observe a peak in $f_{c,N} \times I_{\text{Anode},N}$ curve at certain device width. The product increases initially due to relatively higher cutoff frequencies and an increase in device current. However, as the device width is further increased, the cutoff frequency degradation becomes significant and the saturation in anode current tends to decrease the overall product.
2) The device width at which the product is maximum shifts to a larger value as the junction length increases. For longer junctions, the degradation is not observed as f_c becomes independent, but I_{Anode} continues to increase at higher widths. However, f_c values for this range are lower due to the higher total capacitance attributed to larger junctions area.
3) The product improves with the increase in the number of fingers as the reduction in metal series resistance aids in improving both cutoff frequency and anode current.

In summary, anode junction has a significant impact on diode series resistance and parasitic capacitance. For optimum design, it is imperative to account for both dc and high-frequency performance. The product of normalized cutoff frequency and anode current suggests that for highly scaled devices, we observe the highest cutoff frequencies. However, there is an optimum device width at which maximum product is obtained. Beyond this point, the overall device performance degrades. Increasing the number of metal fingers significantly improves both the RF and the dc performance. It also expands the design space for which THz frequencies can be achieved.

B. Channel Length (L_{AC})

Diode channel resistance is another critical design parameter that affects the device's high-frequency performance. Scaling down the channel length can significantly reduce the transit time and series resistance. However, any improvement in cutoff frequency is determined by the RC product, as discussed in the earlier section. Hence, in this section, we study the impact of device channel length scaling on the high-frequency performance of the SBD.

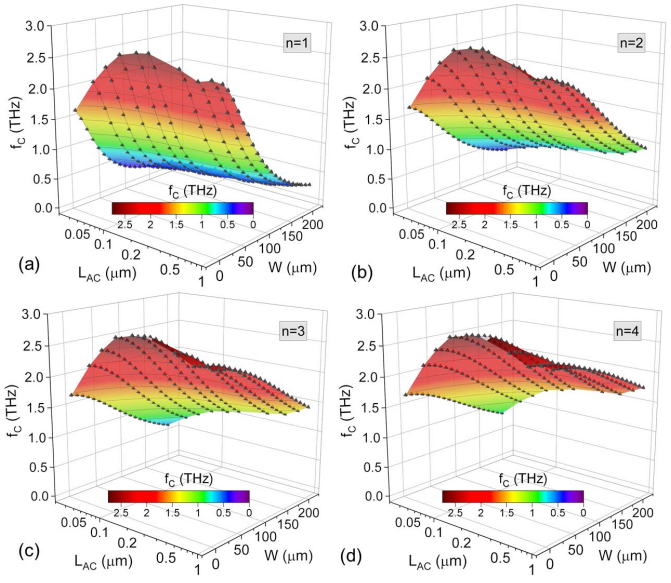

Fig. 7. Cutoff frequency (f_c) variation as a function of channel length (L_{AC}) and device width (W) for (a) $n = 1$, (b) $n = 2$, (c) $n = 3$, and (d) $n = 4$. The anode junction length is fixed at $L_A = 70$ nm.

Fig. 7(a)–(d) shows the variation of f_c as a function of channel length for various device widths. The following observations are made.

1) The cutoff frequency does not improve in proportion to device scaling. For short-channel devices, we observe degradation in f_c, and it is more pronounced for smaller device widths. It can be attributed to nonuniform variation in device capacitance and resistance. Scaling down the device from $L_{AC} = 1$ μm to $L_{AC} = 150$ nm results in a reduction in channel resistance, without a significant increase in parasitic capacitance. Hence, f_c improves for this range. However, scaling the channel length further to $L_{AC} = 30$ nm, we observer fall in cutoff frequency. As shown in Fig. 8(a), scaling from 1-μm channel length, the channel resistance is reduced by a factor of ~0.5; however, the parasitic capacitance increases by a factor of ~4. The fringing capacitance increases significantly for short-channel devices, leading to a reduction of f_c.
2) For higher device width (W), the dependence of f_c on channel length L_{AC} becomes weaker as the resistance of metal lines begins to dominate the channel resistance.
3) a higher number of metal fingers lead to better scaling of f_c as a function of L_{AC}, especially at larger device width. The overall design space is also improved with the number of metal fingers. The same is reflected by the increase in anode current shown in Fig. 8(b).

Scaling of channel length is a critical parameter that affects the diode current, breakdown voltage, and cutoff frequency. Hence, careful consideration is required to account for all the figures of merit while designing the device.

V. Impact of Contact Resistance

Contact resistance is another factor that adds to the diode series resistance and can affect the device cutoff frequency.

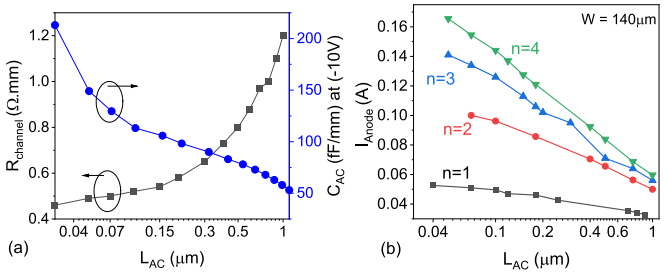

Fig. 8. (a) Channel resistance and device capacitance as a function of channel length scaling. (b) Variation of anode current with channel length. The current is extracted at $V_{AC} = 1.4$ V. The anode junction length is fixed at $L_A = 70$ nm.

As discussed before, it is desirable to achieve minimum ohmic contact resistance to reduce the parasitics. However, it is imperative to understand the impact of contact resistance in correlation to various physical device dimensions. We also investigate the discrete contribution of different parasitic resistances for the entire design space.

A. Correlation With Device Scaling

First, we will probe into the degradation in cutoff frequency with contact resistance as a function of various physical dimensions. We have extracted the relative percentage reduction in f_c when the contact resistance is increased from 0.02 Ω·mm to a certain value. The same has been shown in Fig. 9(a)–(c) and explained in the following.

1) In case of fixed junction length ($L_A = 70$ nm) and channel length ($L_{AC} = 70$ nm), the impact of contact resistance on f_c increases as the number of fingers are increased, as shown in Fig. 9(a). The effect of contact resistance decreases with an increase in the device width as the metal resistance starts to dominate. However, for a higher number of fingers, the contact resistance can have a significant impact even for larger device widths.
2) Fig. 9(b) shows the impact of contact resistance in correlation with anode junction length. The device width and L_{AC} are fixed at 140 μm and 70 nm, respectively. The results show that the effect of high contact resistance is more severe on long junctions compared to small junction lengths. However, as the number of fingers is increased, degradation in f_c becomes more uniform as a function of junction length.
3) The impact of contact resistance in correlation to channel length is shown in Fig. 9(c). For a fixed junction length ($L_A = 70$ nm) and device width ($W = 140$ μm), if the number of anode fingers is less than 3, the degradation in f_c with contact resistance is independent of channel length (L_{AC}). However, with an increase in the number of fingers, the degradation becomes more pronounced for short-channel devices.

The above observations suggest that contact resistance is a critical design parameter for short-channel devices and has a higher impact on device cutoff frequency as the number of

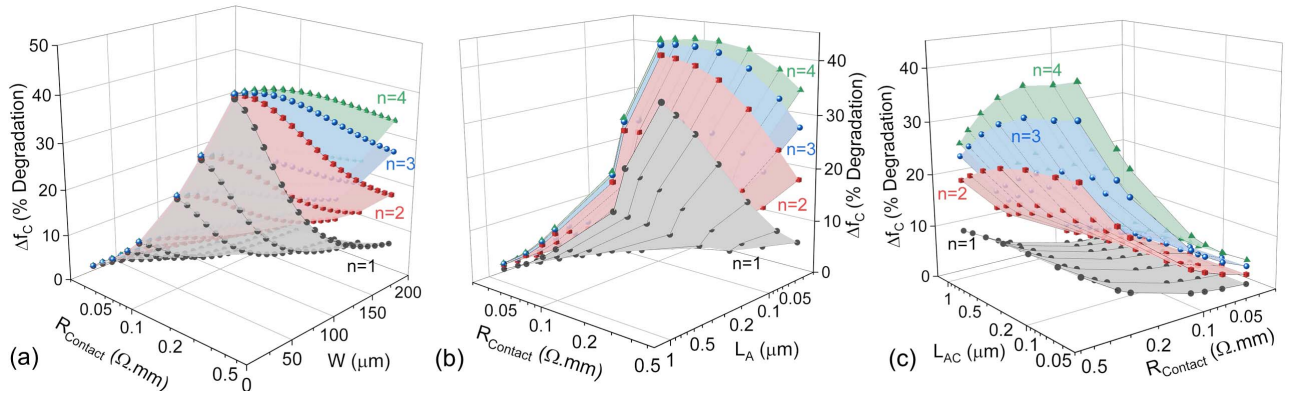

Fig. 9. Percentage degradation in cutoff frequency (f_c) by an increase in contact resistance from 0.02 Ω·mm to higher values as a function of (a) device width (W) (L_{AC} = 70 nm and L_A = 70 nm), (b) junction length (L_A) (W = 140 μm and L_{AC} = 70 nm), and (c) channel length (L_{AC}) (W = 140μm and L_A = 70 nm).

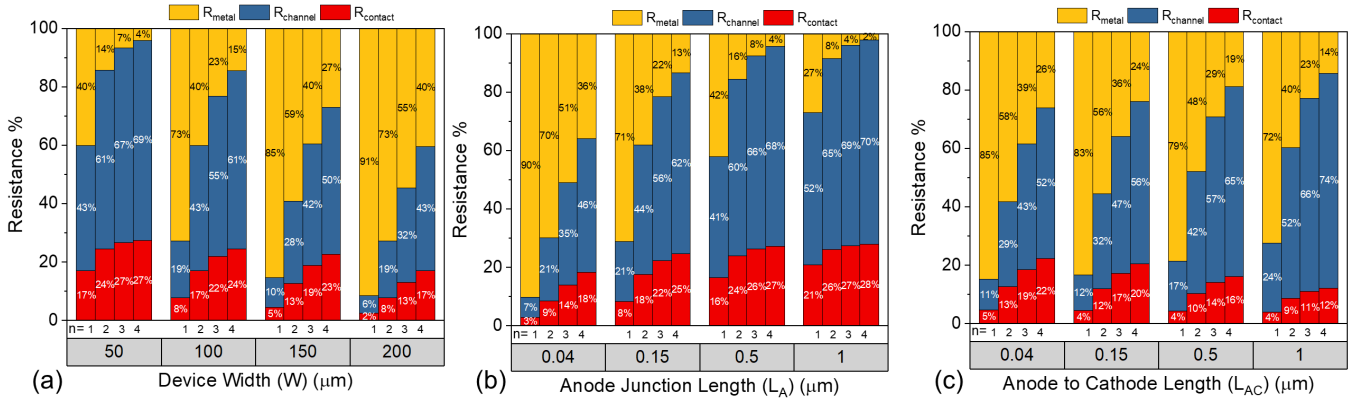

Fig. 10. Percentage distribution of each parasitic resistance as a function of (a) device width (W) (L_{AC} = 70 nm and L_A = 70 nm), (b) junction length (L_A) (W = 140 μm and L_{AC} = 70 nm), and (c) channel length (L_{AC}) (W = 140 μm and L_A = 70 nm).

fingers is increased. Further insight into the contribution of various parasitic resistances is discussed in the following.

B. Parasitic Resistance Contribution

Having studied the impact of individual parasitic resistance components on device cutoff frequency, we determine the contribution of each in various design scenarios. These observations provide a clear picture of the dominating resistance component, which can help identify the key design parameters and prevent the overdesign of secondary parameters. Contact resistance value is considered as 0.2 Ω·mm for these studies. The results are presented in Fig. 10(a)–(c) and discussed in the following.

In scaled devices (L_{AC} = 70 nm and L_A = 70 nm), the distribution is shown in Fig. 10(a). For all the device widths, the contribution of metal resistance falls with the number of fingers. It is highly desired to have multifinger topology as the device width approaches 200 μm. It should be noted that for multifinger devices with lower device widths, most parasitic resistance is contributed by the series and contact resistance. Hence, device scaling and contact resistance optimization is the way forward to achieve higher cutoff frequencies. On the other hand, as the device width is increased, the back-end metal process has to be optimized to reduce the series resistance. At large widths, the use of complex ohmic regrowth techniques can be avoided as the contribution of contact resistance is minimal.

Fig. 10(b) shows the resistance distribution as a function of junction length for fixed L_{AC} = 70 nm and device width W = 140 μm. For smaller junction lengths, the increasing number of fingers is imperative as the metal resistance is significant in this case. For the larger junction lengths, back-end metal optimization does not significantly impact the device performance. Hence, a larger device width can be used in this case. Both channel resistance and contact resistance are the major contributors to device parasitic resistance.

For a fixed junction length (L_A = 70 nm) and device width (W = 140 μm), varying the channel length L_{AC} produces the distribution shown in Fig. 10(c). The contribution of series resistance increases with channel length. In short-channel devices with a high number of fingers, performance is limited by the contact resistance and channel resistance. The channel resistance is fixed by the 2DEG concentration, as L_{AC} is already scaled; the ultralow contact resistance and further increasing the number of metal lines are essential to improve f_c. However, at higher channel lengths, metal resistance and contact resistance optimization do not

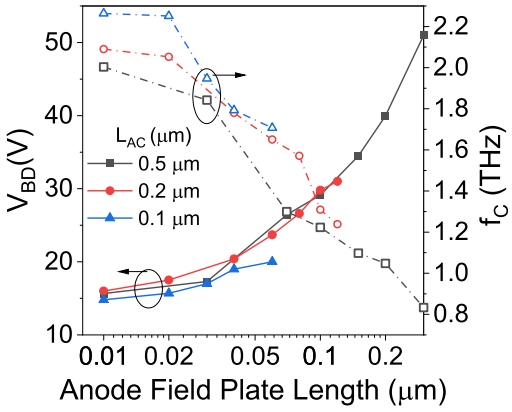

Fig. 11. Device breakdown voltage and cutoff frequency variation as a function of anode field plate length for various channel lengths. $L_A = 70$ nm and $W = 100$ μm has been considered for this study. The reverse anode current = 1 mA/mm is taken as breakdown limit.

yield any significant performance improvement. In this case, longer device widths can be used without compromising the high-frequency performance.

VI. Impact of Anode Field Plate

The long-distance transmission has resulted in an increase in the RF power for a low signal-to-noise ratio at the receiver end. Hence, it is desirable that the mixer or detector systems are qualified for higher input voltage and current swings. The breakdown voltage of high-frequency SBD is an imperative figure of merit and can no longer be overlooked. The aggressive device scaling to obtain high RF performance compromises the device breakdown voltage. Anode metal field plate is an effective technique to increase the device breakdown voltage as it redistributes the electric field in the channel and mitigate premature breakdown [18]. We investigated the impact of field plate on device breakdown and RF performance for different channel lengths (L_{AC}), as shown in Fig. 11. It is evident that there is a significant improvement in the reverse breakdown voltage of the diode. However, it adversely affects the diode cutoff frequency. It is attributed to the additional fringing capacitance of the field plate metal, which adds to the total device capacitance. Hence, this tradeoff must be accounted for while designing the THz SBD.

VII. Conclusion

We presented a comprehensive TCAD design methodology of multifinger planer SBDs for THz applications. A novel modeling approach is proposed to include the 3-D parasitic effects on multifinger SBD performance. The impact of lateral device scaling is studied in correlation to the physical width and a number of fingers. We found that minimizing the junction length improves the cutoff frequency, but it degrades drastically as a function of device width. On the other hand, the short junctions contribute to high series resistance leading to low anode current. In order to obtain a better insight into this tradeoff, we proposed a performance figure of merit parameter, which is the product of the normalized cutoff frequency and anode current. We observed that the performance peaks at a specific device width beyond which it degrades monotonously. In short junction devices, the peak is toward lower device widths, and it shifts to higher widths as the junction length is increased. Depending on the application, the device with a high current and desired f_c can be selected by analyzing this FOM. With increase in the number of fingers, the design space to obtain THz operating frequency expands. Similarly, the performance of short-channel devices was found to be substantially influenced by the device width and the number of metal fingers. An optimum channel length is found to have a maximum of f_c due to nonuniform scaling of parasitic capacitance and resistance. Contact resistance was observed to be an imperative design parameter for short-channel lengths, low device widths, and long junctions. The impact of contact resistance increased with the number of fingers. The contribution of all parasitic resistances is plotted in various design scenarios to select the critical performance optimization parameter and to avoid the overdesign. Finally, we investigated the tradeoff between breakdown voltage and f_c for a field-plate-terminated SBD.

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