Design Guidelines and Performance Tradeoffs in Recessed AlGaN/GaN Schottky Barrier Diodes

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***Abstract*— Critical design parameters for AlGaN/GaN Schottky barrier diodes (SBDs) are analyzed in this work using TCAD computations and detailed experiments. A comprehensive TCAD-based computational modeling approach is developed for GaN-based SBD. Breakdown mechanisms in SBD for unintentionally doped (UID) buffer, Fe-doped buffer and C-doped buffer are studied. For the first time, we have reported impact of anode recess, on breakdown and leakage behavior of SBD, in correlation with interface defects. Using these insights an optimum recess design strategy has been presented and is validated experimentally. Furthermore, for the first time, we have revealed critical repercussions of the field plate termination on SBD's breakdown, leakage as well as transient behavior. Forward and reverse recovery measurements were carried out to study the diode's transient performance as a function of field plate design. Various performance matrices such as diode current collapse, reverse current overshoot and reverse recovery time were studied experimentally as a function of field plate design. Moreover, the field plate-dependent electro-thermal behavior of SBD was studied using TCAD computations and experiments. Using the systematic device design approach we have experimentally demonstrated large periphery SBD with 15 A forward current at 5.5 V.**

***Index Terms*— AlGaN/GaN diode, diode, HEMT simulation, power diode, Schottky diode.**

I. Introduction

SCHOTTKY barrier diode (SBD) is one of the most essential components for power electronics systems. AlGaN/GaN-based SBD, owing to its ability to sustain high electric fields and high temperature, while offering very high current density, have attracted tremendous attention for high power switching applications. Various SBD designs have been discussed in the literature over the past few years comprising conventional (nonrecessed) diodes [1], partially recessed diodes [2], [3], recessed diodes [4]–[7], hybrid [8], [9], and 3-D anode structures [10]–[13]. The conventional Schottky diodes exhibit high cut-in voltage and low current, resulting in a lowered converter efficiency. The recessed diodes have been able to mitigate these issues but still face significant design challenges. For example, in our recent work, we disclosed increased reverse leakage by field localization at the anode edge, which was attributed to the presence of interface defects/traps at the Anode (metal)–GaN interface in the recessed region [14]. While we addressed it by surface passivation and florine plasma techniques, however, design methods to suppress or engineer electric field from critical regions is largely missing in previous works. Furthermore, while there are reports on anode field plate design approaches [15] to improve the breakdown voltage, its implications on other critical performance parameters such as diode-current recovery, reverse-recovery performance and heat dissipation are missing in earlier works. Moreover, the impact of buffer traps (i.e., buffer doping) on breakdown performance of the diode is also missing in previous works. For example, Chiu *et al.* [16] have studied the impact of Fe-doped buffer on AlGaN/GaN SBD, however, the physical insights into the electric field distribution and its relation with buffer traps in SBDs are largely not discussed. Similarly, while there have been extensive studies to understand field distribution at the breakdown in AlGaN/GaN HEMT devices consisting of C-doped buffers [17], [18], similar reports however, for SBDs are nonexistent. Due to high power operating conditions, SBD is expected to generate significant heat, which can potentially deteriorate the device performance. Therefore, understanding the self-heating behavior in SBDs is imperative to design a device for efficient heat dissipation, which is also missing in previous works.

In this article, we have addressed these gaps by using a comprehensive TCAD-based design approach and have validated all findings using detailed process experiments and rigorous device (dc and pulse) characterizations. The article is arranged as follows: Section II presents the experimentally calibrated TCAD computation framework developed in this work for the design studies of AlGaN/GaN SBDs, which is missing in previous works. Section III presents the details of the AlGaN/GaN recessed SBD fabrication process. The design aspects related to the recessed Anode region of the SBD is discussed in Section IV, whereas the impact of buffer on diode's breakdown performance is presented in Section V. Section VI presents the Anode side field plate design guidelines, its impact on the breakdown and reverse recovery and thermal management guidelines, Besides, physical insights into heat dissipation and the role of field plate is also discussed in Section VI. Finally, Section VII concludes the work.

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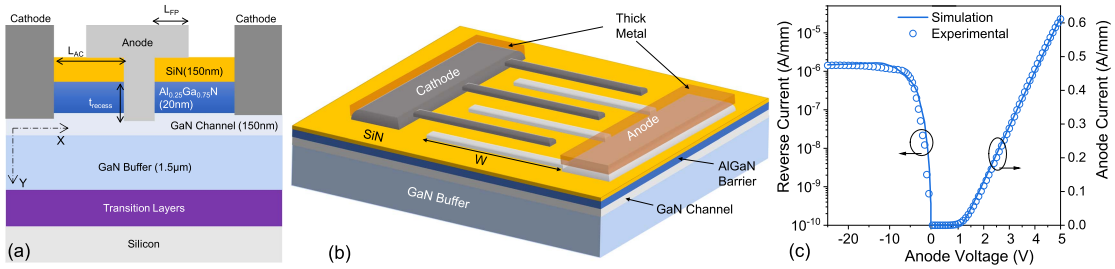

Fig. 1. (a) Schematic view of AlGaN/GaN SBD realized in this work for experimental validation. The same architecture was used for TCAD simulations. (b) Design layout of the fabricated SBD. (c) Diode's forward and reverse *I–V* characteristics depicting match between measured data and characteristics extracted from calibrated TCAD setup.

II. Device Fabrication

The SBDs are realized using a commercial-grade 600 V AlGaN/GaN stack grown over Silicon substrate, as shown in Fig. 1(a). The GaN buffer is carbon doped with 20 nm AlGaN barrier layer grown on top. AlGaN surface is passivated with *in situ* grown silicon nitride (50 nm). The fabricated device layout is shown in Fig. 1(b), with $n \times W$ being the total electrical width. Here, n is the number of anode fingers and W is the finger width. Three different devices layouts, 1×400 μm, 1×1 mm, and 25×1 mm were fabricated for various studies in this work. The anode to cathode separation (L_{ac}) of 5 μm and 10 μm was used for $W = 400$ μm and $W = 1$ mm, devices, respectively. The device fabrication process started with blanket deposition of 100-nm SiN using PECVD to thicken the passivation dielectric. To make ohmic contacts in the cathode region, while the SiN layer was fully recessed, partial recess of the AlGaN layer was done followed by Ti/Al/Ni/Au metal deposition. Ohmic metal stack was annealed in N_2 ambient postmetal lift-off. To form the Anode region having Schottky contact SiN layer was selectively removed from the anode region. Subsequently, AlGaN layers or GaN layers were etched up to a recess depth of t_{Recess}, as shown in Fig. 1(a). This was followed by surface treatments as discussed in our previous work [14], Ni/Au metal stack deposition and postmetalization thermal anneal. To reduce metal resistance and current drop across anode/cathode metal fingers, a thick metal stack of Ni/Al/Au (20 nm/1000 nm/50 nm) was deposited over the anode, cathode, and pad regions. Subsequently, a soft anneal was done to reduce device-to-device metal resistance and variability.

III. Computational Modeling and Design Framework

For developing design insights into AlGaN/GaN SBD, TCAD framework used in our previous works for AlGaN/GaN HEMTs [17]–[20] has been extended here for AlGaN/GaN SBDs while using device structure shown in Fig. 1(a). Experimentally measured SBD characteristics are shown in Fig. 1(c) and its match with characteristics extracted from the calibrated TCAD setup. The details of computational modeling, calibration, and design framework are elaborated below.

A. Polarization, Surface, and Buffer Traps

Polarization at all the heterointerfaces is considered to accurately estimate the band profile and two-dimensional electron gas (2DEG) in the device. The polarization charge has been calculated using the polarization models as discussed in [21]. As reported experimentally [22], surface traps are included at the AlGaN/SiN interface to model the origin of 2DEG in the channel. To study the impact of buffer traps three types of buffer dopants have been modeled and examined. First, in unintentionally doped (UID) buffer most of the traps (present at $E_C - 1.1$ eV) emerge from dislocations, which have higher density near the substrate when compared to channel [23]. Second, Iron (Fe) doped buffer with doping concentration of 3×10^{18} cm^{-3}, capture cross section and trap energy level of 10^{-13} cm^{-2} and E_c–0.7 eV, respectively, is considered [24]. Third, a carbon-doped buffer, with C as a compensating dopant has been accounted. The donor and acceptor concentrations are taken as 10^{18} cm^{-3} and 5×10^{17} cm^{-3}, respectively. More details on modeling of C-doped buffer can be found in our previous works [17], [18].

B. Carrier Transport and Contacts Modeling

In order to accurately model the transport through the Schottky interface, the anode region has been modeled as a nonideal Schottky contact consisting 1) distribution of interface states with a charge neutrality level (CNL) ϕ_0; 2) donor traps corresponding to nitrogen vacancies (V_N) at the plasma-etched surfaces; and 3) interfacial layer emulating the ultrathin oxide between the metal and etched III-N surfaces. Fig. 2 shows the energy band diagram along with the Schottky interface. Here, ϕ_m is the metal work function, ϕ_{Bn0} is the barrier height, ϕ_0 is the CNL above the valance band, χ is the electron affinity of semiconductor, ψ_{bi} is the built-in potential, δ represents the thickness of the interfacial layer and E_g is the semiconductor bandgap. ϵ_i and ϵ_s are permittivity of the interfacial layer and the semiconductor, respectively. Δ is the potential across the interfacial layer. Interface trap density is given by D_{it} and the effective interface charge is Q_{ss}. The shallow donor trap level introduced due to Nitrogen vacancies is shown as V_N at energy $E_C - 0.37$ eV [25]. E_C, E_V, and E_F represent conduction, valence, and Fermi energy levels, respectively.

Surface dangling bonds due to plasma etching leads to nitrogen vacancies at the surface, which creates a surface state continuum with a discrete energy peak. The charge transfer between metal and the interface states pins the Fermi level at the CNL. This Fermi level pinning modifies the Schottky barrier height and needs to be accounted for accurate device modeling, without which the Schottky barrier height will be left to be only a function of metal work function, as shown

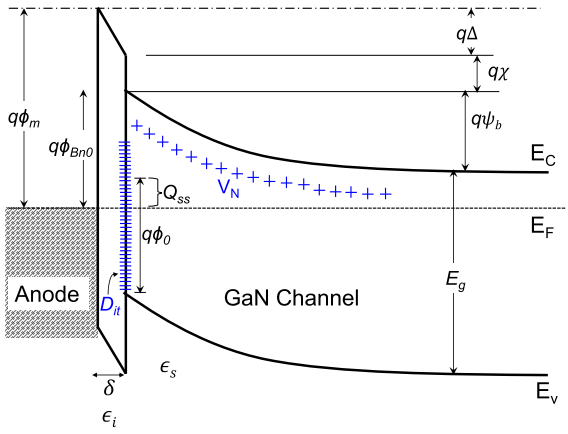

Fig. 2. Energy band diagram along the anode Schottky contact.

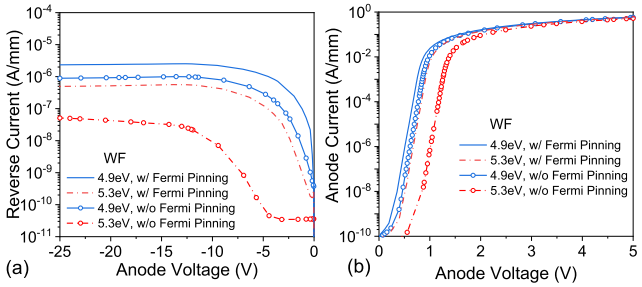

Fig. 3. Diode (a) reverse and (b) forward characteristics without (w/o) and with (w/) Fermi level pinning.

in Fig. 3. This has been accounted in TCAD simulations while using the following relation [26]:

$$\phi_{Bn0} = S(\phi_m - \chi) + (1 - S)\left(\frac{E_g}{q} - \phi_0\right) \tag{1}$$

where S is given by (in case the Fermi level pinning is not accounted, the value of S becomes 0)

$$S \equiv \frac{\varepsilon_i}{\varepsilon_i + q^2 \delta D_{it}}. \tag{2}$$

A unified model for electronic states at the Schottky/III-N material interface is used here in the simulations [27]. The U-shaped surface states continuum is defined using disorder induced gap states (DIGS) model

$$N_{ss}(E) = N_{ss0} \exp\left(\frac{|E - E_{CNL}|}{E_0}\right)^n \tag{3}$$

where N_{ss0} is the minimum surface state density, E_{CNL} ($E_g - \phi_0$) is the CNL from the conduction band level. The surface states continuum distributed above the E_{CNL} has acceptor type state characteristics. Whereas, the levels below E_{CNL} have donor-like trap nature. E_0 and n are parameters related to the shape of surface state continuum. The position of CNL is mole-fraction dependent (x) and is given by the following formula:

$$E_{CNL}(\text{eV}) = E_g - (E_C + 2.37 + 0.60x). \tag{4}$$

In the U-shaped continuum, shown in Fig. 4(a), the discrete energy level corresponding to nitrogen-related vacancies (V_N) are also presented at energy level of $E_C - 0.37$ eV.

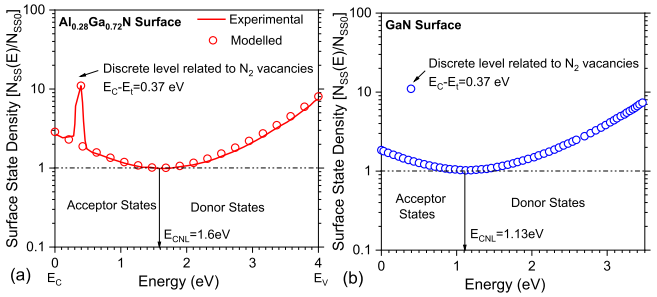

Fig. 4. (a) Experimental [25] and modeled distribution of interface state density for $Al_{0.28}Ga_{0.62}N$. (b) Modeled interface state distribution for GaN.

The concentration of these discrete states is a function of surface processing conditions, such as plasma etching, metal deposition, and thermal annealing. These donor traps are ionized at the interface due to Fermi level pinning, affecting the diode conduction. Furthermore, in order to accurately model these interface states, we fit the proposed D_{it} distribution for $Al_{0.28}Ga_{0.62}N$ [25] with (3) as shown in Fig. 4(a). The extracted values of parameters E_0 and n are 1.55 and 1.68, respectively. Furthermore, using (3) and (4), D_{it} distribution for GaN surface was calculated as shown in Fig. 4(b). The same has been included in the simulations to capture the accurate interface state distribution on an etched GaN surface. Finally, the carrier transport in Schottky diode is accounted for using nonlocal tunneling model, which uses Wentzel–Kramer–Brillouin (WKB) approximation [28]. Employing the proposed methodology for modeling the SBD, the simulation results are calibrated with the experimental data as shown in Fig. 1(c).

IV. Anode Design

A. Anode Schottky Interface

The density of surface defects is a function of plasma power during etching, etch chemistry, and postetch surface treatment. Impact of these interface traps on the electrical performance of the diode is studied using the model developed in the last section. In the first case, the minimum concentration in the surface state continuum (N_{ss0}) is varied and its' effects on diode I–V characteristics are observed. Fig. 5(a) and (b) show the reverse and forward diode I–V plots as function of N_{ss0}. The discrete trap level concentration (V_N) is kept fixed at 7×10^{13} cm^{-2}. Increasing the N_{ss0}, results in increased ionization of acceptor traps (Fig. 6), hence, the net positive donor charge reduces at the interface. Fall in net positive interface charge increases the Schottky barrier width [14], leading to a reduction in reverse-current and positive shift in cut-in voltage. However, the shift is not significant due to a large number of discrete donor state (V_N) introduced during device processing.

The V_N defects levels present at the interface are ionized due to Fermi level pinning. Increase in the V_N concentration causes thinning of the Schottky barrier, which leads to enhanced carrier tunneling at the contact. Consequently, high reverse leakage and a negative shift in threshold voltage are observed as depicted in Fig. 5(c) and (d), respectively. A detailed physical analysis of the impact of discrete nitrogen vacancies on diode breakdown characteristics is presented in our earlier work [14]. We can conclude that nitrogen-vacancy related

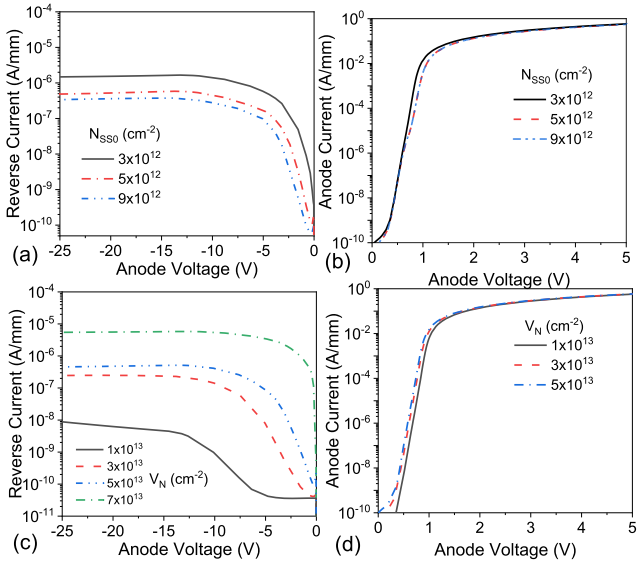

Fig. 5. Simulated (a) and (c) reverse and (b) and (d) forward characteristics as function of minimum surface trap density (N_{ss0}) and discrete nitrogen vacancies (V_N), respectively.

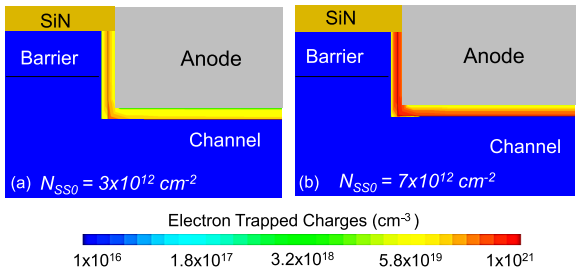

Fig. 6. TCAD contours representing charge state of acceptor traps at the Schottky interface for (N_{ss0}) = (a) 3×10^{12} cm^{-2} and (b) 7×10^{12} cm^{-2} at $V_{ac} = -25$ V.

trap concentration is the key parameter and minimizing it can significantly enhance the diode OFF-state performance.

B. Anode Recess

In this section, we understand the implications of anode recess on the breakdown and ON-state characteristics of the diode. The earlier literature demonstrating recessed diode architectures do not corelate the anode recess design with the interface trap distribution at the Schottky contact. The surface states are bound to appear due to various process steps involved during fabrication. In our past work [14], we established that even at the fixed anode recess depth, the diode performance may vary substantially attributed to the type of interface traps and its concentration. Here, we have studied the impact of these states on diode performance in correlation with anode recess depth.

The reverse leakage current as a function of recess depth is found to be a strong function of interface state density. If the surface defects are high, the space-charge is restricted to a narrower region near the contact [14]. It prevents the distribution of electric field peak and leads to degraded OFF-state performance. This dependence is illustrated in Fig. 7(a). The reverse current increases marginally and remains relatively less sensitive to surface state concentration for higher recess depths. For partially recessed barrier the increase in reverse

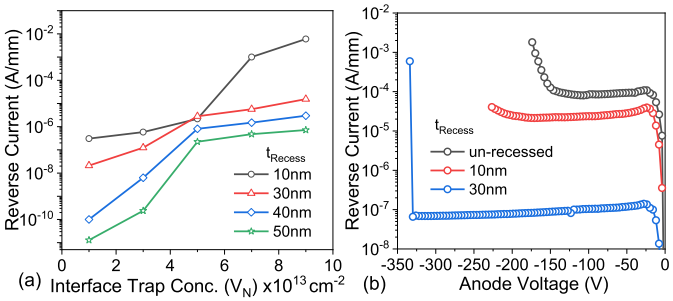

Fig. 7. (a) Simulated reverse leakage as function of interface trap concentration (V_N) and anode recess depth. (b) Experimentally measured breakdown voltage of 400 μm diode as function of anode recess depth.

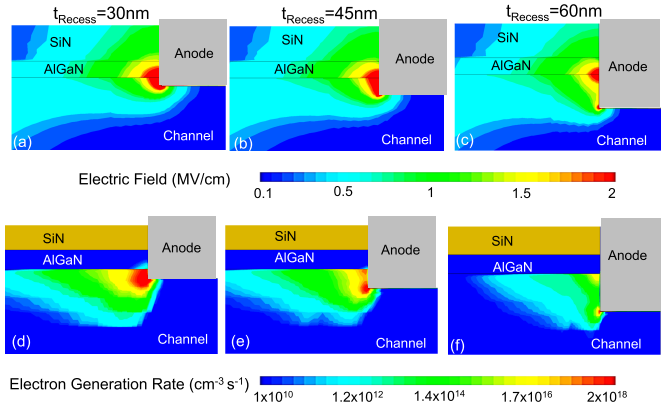

Fig. 8. Electric field and electron generation rate contours at $V_{ac} = -80$ V, for recess depth (t_{Recess}) of (a) and (d) 30 nm, (b) and (e) 45 nm, and (c) and (f) 60 nm, respectively.

leakage as a function of interface trap density is much higher compared to fully recessed design. The partially recessed design consists of 2DEG below the anode contact region, thereby, increase in the surface defects lead to enhanced carrier tunneling at the Schottky interface. Hence, even though the partial recess design provides minimum cut-in voltage, the diode performance is more sensitive to surface defects.

In the case of low trap density, space-charge is not limited by the donor states. Increasing the recessed depth depletes the 2DEG below and extends the depletion region away from the contact edge. Hence, the electric field peak is distributed and pushed away from the channel as shown in Fig. 8(a)–(c). The electric field proportionally affects the carrier generation rate at the anode contact. Higher electric field enhances the carrier tunneling rates at the anode junction, which eventually leads to impact ionization. It is also evident from the contour plots in Fig. 8(d)–(f), depicting lower field-induced carrier generation in devices with higher anode recess depth. For experimental verification, we measured the breakdown characteristics of diodes with varying recess depths as depicted in Fig. 7(b). The partially recessed device had poor breakdown performance, and it improved with the increase in recess depth. This corroborates with our simulation findings that the reverse current decreases significantly with recess depth due to space charge relaxation. The breakdown voltage is also improved as a result.

The statistical data of reverse leakage and device cut-in voltage as a function of recess depth is shown in Fig. 9(a) and (b), respectively. The cut-in voltage decreases as the AlGaN barrier

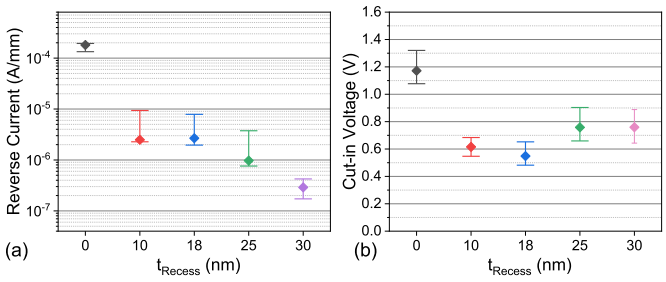

Fig. 9. Experimentally extracted (a) reverse current and (b) cut-in voltage as function of anode recess depth. Each data point is the median across the 30 devices with 400-μm anode width.

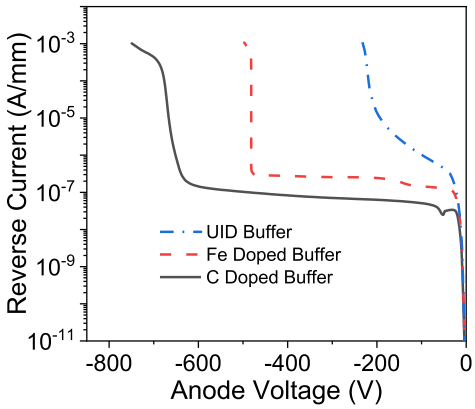

Fig. 10. Simulated breakdown characteristics for SBD consisting of UID, Fe-doped and C-doped GaN buffer.

is partially etched. It is attributed to enhanced carrier tunneling probability as the 2DEG is not completely depleted up to certain barrier thickness. Further etching of AlGaN and GaN channel depletes the 2DEG completely and increases the tunneling barrier width. Consequently, the cut-in voltage increases for higher recess depths. To avoid confusion from works presented earlier [29], [30], it is worth highlighting that the breakdown voltage is reduced in case of partially recess, as shown in this work, only when 2DEG is present below anode contact.

V. Impact of Buffer Doping

In this work, we have analyzed the impact of buffer doping on the breakdown of SBD using physical modeling. The three types of buffer stacks- UID, Fe-doped and C-doped are modeled here with trap parameters discussed in Section II earlier. Each buffer type consists of unique trap characteristics and used for specific applications. Hence, we have investigated the three buffer types in our studies. The breakdown characteristics for the three cases are shown in Fig. 10 with the detailed physical analysis as follows.

A. UID Buffer

In the case of UID buffer, the electric field at the anode contact edge and field plate edge increase with reverse bias voltage as depicted in Fig. 11(a). The depletion region extends laterally from anode edge toward the cathode side. The field plate also depletes the localized region in the channel, thus extending the voltage blocking capability of the device. At the breakdown condition, the impact ionization takes place near

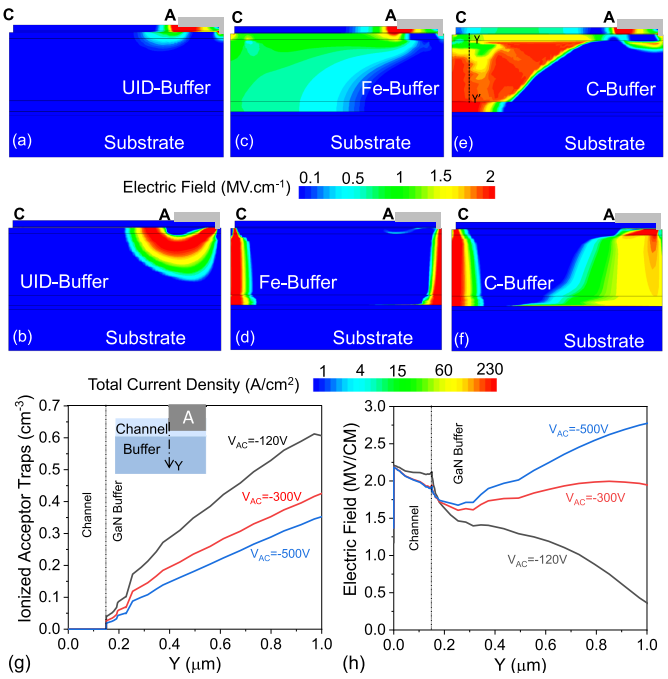

Fig. 11. Contour plots representing the electric field distribution and total current density at breakdown in case of (a) and (b) UID buffer. (c) and (d) Fe doped Buffer and (e) and (f) C-doped buffer. (g) Concentration of ionized trapped charges and (h) electric field near anode along the Y-direction, as function of reverse bias voltage.

anode contact and the field plate edge resulting in the generation of electron-hole pairs. The large of number holes spread into the buffer region and decrease the net negative charge in the buffer. It reduces the barrier for the injection of electrons into the GaN buffer. This results in high reverse current through the buffer region. Hence, the breakdown voltage is limited by punchthrough current due to avalanche process at the anode contact as shown in Fig. 11(b).

B. Fe-Doped Buffer

The buffer leakage current can be mitigated by using Fe-doped GaN buffer. Fe doping yields semiinsulating properties to GaN buffer by introducing acceptor traps. The spatial field distribution is similar to UID case, with electric field peak observed at the anode and field plate edge as depicted in Fig. 11(c). The acceptor traps in the buffer capture the injected electrons and prevent a sharp rise in reverse current. Due to suppression in reverse leakage, the breakdown voltage is substantially improved. In this case, the breakdown eventually occurs at the anode terminal due to avalanche action, and the current flows through the parasitic conduction path as shown in Fig. 11(d). This conduction path is formed due to the presence of polarization induced hole layer at the hetero-interface near the substrate.

C. C-Doped Buffer

C doping in GaN is compensating in nature, resulting in a peculiar electric field distribution at the breakdown as shown in Fig. 11(e). The impact ionization is not confined near the anode region and at the breakdown, due to avalanche, current conducts through the buffer as shown in Fig. 11(f).

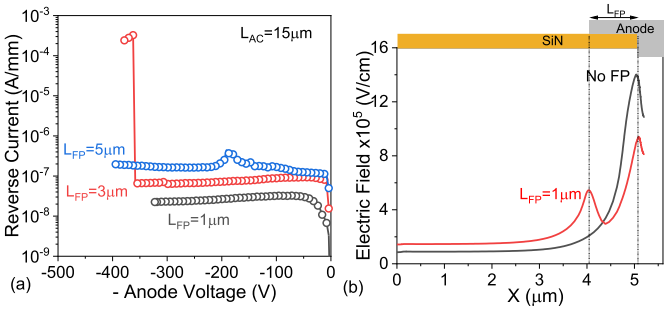

Fig. 12. (a) Experimentally measured breakdown voltage of 1 mm diodes as function of field plate length. The recess depth in this case is 30 nm. (b) Electric field distribution along the channel with and without field plate extracted at $V_{ac} = -80$ V.

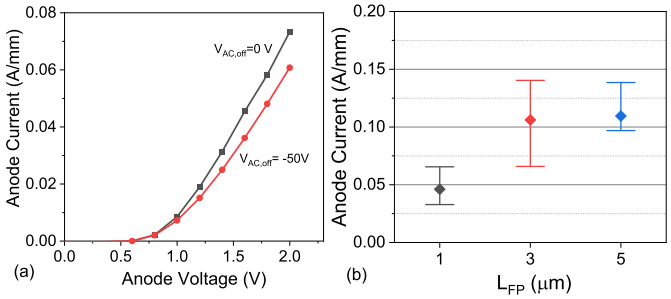

Fig. 13. (a) Diode current collapse due to switching from OFF-state ($V_{ac,OFF}$) to ON-state. (b) Measured diode current at $V_{ac} = 5$ V as function of field plate length after OFF- to ON-state switching. Each data point is the median across the 30 devices with 400-μm anode width.

The C-doped buffer consists of both acceptor and donor trap states. As the reverse bias is increased, the electric field drives the electron toward the cathode. This leads to deionization of acceptor traps in the buffer region as depicted in Fig. 11(g). As a result the net positive charge in the buffer increases, given as $N_T = N_D^+ - N_A^-$. Here, N_D^+ and N_A^- refer to ionized donor and acceptor charges in the buffer. Increase in net positive charge shifts the electric field into the bulk as shown in Fig. 11(h). Hence, in the case of C-doped buffer, the electric field is distributed at the surface by the field plate and into the bulk due to change in traps states. This enables high breakdown voltage in SBD with C-doped buffer stacks. Further physical insights into breakdown physics of C-doped buffer are presented in our earlier work [17], [18].

VI. Field Plate Design & Thermal Management

The field plate is a very effective edge termination for recessed diodes. There are several performance aspects to field plate design, however, only the breakdown oriented approach has been reported in the literature. We systematically analyze the field plate design in Schottky diodes as discussed below.

A. Breakdown Voltage

Breakdown characteristics measured for 1 mm diodes with different field plate lengths are depicted in Fig. 12(a). It is evident that the breakdown voltage improves with anode field plate length. The breakdown is destructive in nature and thermal failure is observed at the breakdown point. The electric field distribution along the channel is illustrated in Fig. 12(b). Two electric field peaks are observed in the presence of anode field plate, hence, the premature impact ionization at Schottky contact is mitigated. It should be noted that while the electric field profile has weak dependence on recess shape, it doesn't depend on the anode metal geometry.

B. Forward Recovery

Switching diode to OFF-state requires large negative bias at the anode terminal. It can lead to the injection of electrons from the anode to the traps on the AlGaN surface. This surface trapped charges deplete the 2DEG in the localized region. The inability of these trapped charges to recover during off to on switching transient can lead to ON-current collapse in diodes. This phenomenon is similar to "virtual gate" effect observed in HEMT devices that lead to current collapse. It is depicted in Fig. 13(a), as the diode current falls after switching it from -50 V ($V_{ac,OFF}$) to 2 V. We analyzed the impact of field plate on the current collapse due to this switching transient. The results are shown in Fig. 13(b). It is evident that the field plate is effective in fast recovery of depleted 2DEG, caused by the electron trapping in OFF-state. For the larger field plates, the forward recovery of current is more efficient. Hence, the anode field plate can be an effective measure to rectify the ON-state current degradation problem in SBD.

C. Reverse Recovery

Reverse recovery characteristics are imperative for SBD, especially for power switching applications. We carried out reverse recovery measurements on SBD for different field plate lengths using transmission line pulse (TLP) setup shown in Fig. 14(a). The characteristics are shown in Fig. 14(b). The diode is forward bias by injecting 50-mA current into the anode contact. A transient pulse with -50 V amplitude and 100 ps fall time is applied at the anode terminal to turn off the diode. The reverse recovery time (t_{rr}) decreased with the field plate length as shown in Fig. 14(c). It is attributed to the faster depletion of carriers in the channel by the capacitive effect of the field plate. However, the reverse current overshoot increased with field plate lengths, as depicted in Fig. 14(d). Field plate adds to the diode parasitic capacitance. The sudden change in the voltage bias conditions (dV/dt) leads to current transient overshoot. The parasitic capacitance increases with field plate length, resulting in larger reverse current during switching. It is a critical figure-of-merit parameter for power converters. High reverse overshoot current can significantly increase the power dissipation during the switching operation. It is imperative to minimize the switching losses, hence, the tradeoff between breakdown improvement and current overshoot must be accounted while designing SBD.

We have developed an electrostatic model to verify the regression of reverse recovery time with field plate length. The total reverse recovery charge (Q_{rr}) to be removed can be approximated as: $Q_{rr} = (I_{rr} \cdot t_{rr}/2)$, and, the reverse current (I_{rr}) is given by- $I_{rr} = t_{rr} \cdot (di/dt)$. Hence, t_{rr} can be written as: $t_{rr} = \sqrt{(2Q_{rr}/di/dt)}$. However, in presence of field plate the modified reverse recovery time is given by- $t_{rr} = \sqrt{(2(Q_{rr} - Q_{FP})/di/dt)}$. Where Q_{FP} represents the

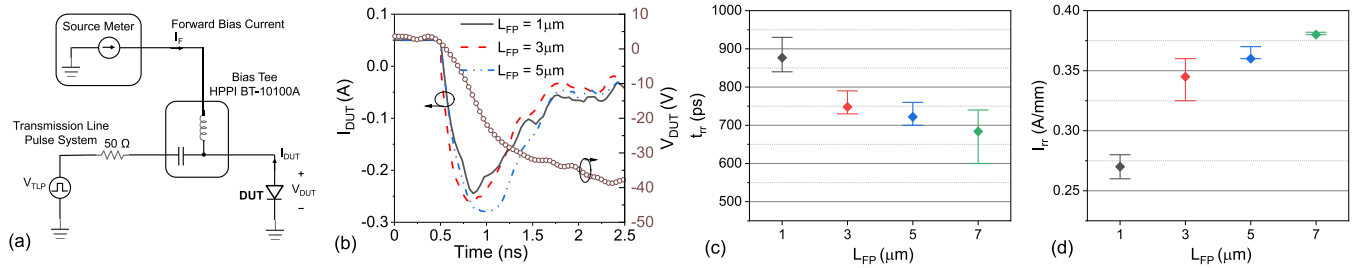

Fig. 14. (a) TLP measurement setup employed for measurement of diode reverse recovery. (b) Reverse recovery characteristics for SBD with varying field plate lengths. (c) Reverse recovery time (t_{rr}) and (d) reverse overshoot current (I_{rr}) as function of anode field plate length. The symbol representing the median of ten sets of measurement on 1 mm diodes.

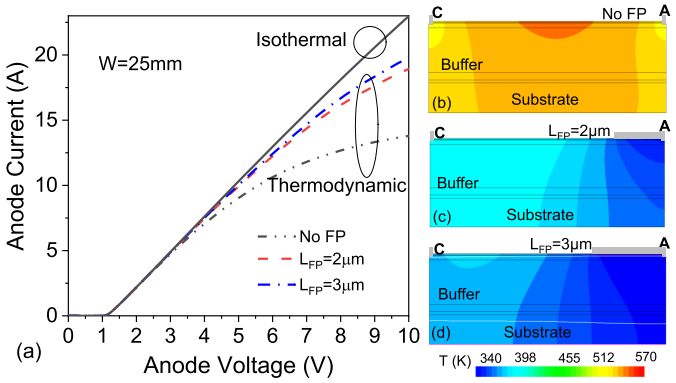

Fig. 15. (a) Simulated forward I–V characteristics as function of field plate length in isothermal and thermodynamic conditions. Lattice temperature distribution contours of device with (b) no field plate, (c) $L_{FP} = 1\ \mu$m, and (d) $L_{FP} = 3\ \mu$m.

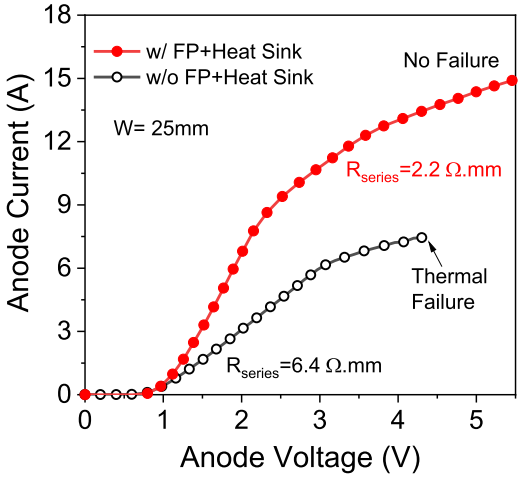

Fig. 16. Experimentally measured forward I–V characteristics of field plate terminated 25 mm diode, with and without heat sink.

contribution to the total charge carrier removed by the field plate. The field plate charge can be calculated using capacitive model: $Q_{FP} = C_{FP} \cdot V_{rev}$, which can be written as: $Q_{FP} = (\epsilon_0 \epsilon_r W \cdot L_{FP} \cdot V_{rev}/t_{pass})$. Here, ϵ_0 and ϵ_r represent the relative permittivity of vacuum and passivation layer. Device width, field plate length, and passivation thickness are represented by W, L_{FP} and t_{pass}, respectively. Reverse bias anode voltage is given by V_{rev}. Now, following expression can be obtained: $t_{rr} = \sqrt{(2(Q_{rr} - (\epsilon_0 \epsilon_r W \cdot L_{FP} \cdot V_{rev}/t_{pass}))/di/dt)}$. The above model suggests the reverse recovery time falls as function of field plate length for the Schottky diode.

D. Electro-Thermal Behavior

AlGaN/GaN-based SBDs are commonly used for high power applications, as a result, a significant amount of heat is generated in the device. The high lattice temperature degrades the carrier mobility and increases the series resistance of the diode. An external heat sink is imperative for these devices in order to sustain the high current. However, we need to enable a better propagation of heat at the intrinsic device level. Using simulations, we analyzed the electro-thermal behavior of SBD. A 25 mm device is simulated in isothermal and thermodynamic conditions as shown in Fig. 15(a). In isothermal simulations, the device temperature is kept constant at 300 K thought the operation. Whereas in thermodynamic simulations lattice heat equations are solved and electro-thermal transport is taken into consideration. We found that the degradation in anode current is mitigated with anode field plate length. For further analyses, the contours are shown in Fig. 15(b)–(d) representing the lattice temperature inside the device. The field plate provides a more efficient temperature distribution, recovering the carrier mobility.

For experimental verification of the impact of lattice heat on device current, we fabricated 25 mm (25 × 1 mm) diodes. In one set of devices, for efficient heat dissipation, the anode field plate of 2 μm was employed. The devices were measured with and without heat sink as shown in Fig. 16. We observed a significant boost in the diode current (15 A at 5.5 V) due to efficient heat propagation via field plate and heat sink. Hence, a thermally efficient diode design and field plate are indispensable for high power applications.

VII. Conclusion

The OFF-state diode performance was studied as a function of anode recess depth and in correlation to interface defects. We found that discrete energy levels introduced by Nitrogen vacancies have a more pronounced impact on diode performance compared to the continuum of surface states. It was observed that the reverse leakage is mitigated and the breakdown voltage was improved with the recess depth. Leakage in partially recessed design was found to be more sensitive to interface traps compared to the fully recessed diode. Increasing the recess depth further relaxes the e-field, which lowers the dependence of leakage and breakdown voltage on

interface traps. Breakdown mechanism in SBD as a function of buffer doping revealed uniform electric field distribution in case of C doped buffer, which allows C-doped buffer to offer the highest breakdown voltage. Trade-offs related to field plate design were examined in detail. Field plate termination improves the device breakdown voltage by redistributing the surface electric field and also enabled a faster recovery of trapped charges during switching transient from OFF- to ON-state. However, the field plate was found to generate higher reverse overshoot current during OFF- to ON-state transition, which is attributed to higher parasitic capacitance. This can lead to significant power loss, which lowers the converter efficiency. Thermodynamic investigations predicted improved heat distribution and mitigated self-heating behavior in the presence of the field plate. As predicted by TCAD-based design approach, experiments confirmed that field plate aids in mitigating the diode current degradation and early failure caused by self-heating. Fabricated diodes (with $W = 25$ mm) with an efficient thermal design provided 15 A diode current at a forward bias voltage of 5.5 V.

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