Device, Circuit, and Reliability Assessment of Drain-Extended FinFETs for Sub-14 nm System on Chip Applications

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***Abstract*— This article explores the scope of drain-extended FinFET (DeFinFET) as a high-voltage (HV) device contender for Fin-based SoC applications. For the first time, guidelines for efficient and reliable HV integration in sub-14 nm FinFET nodes are given. Up to what extent DeFinFET stands as a promising choice is carefully investigated through device-circuit interactions and reliability analysis of range of DeFinFET options. The same is then compared, in terms of radio frequency (RF)-power amplifier (PA) performance, dc–dc conversion efficiency, electrostatic discharge (ESD) robustness, and hot carrier immunity (HCI) reliability, with other HV alternatives in FinFET nodes and its planar counterpart, that is drain-extended MOS (DeMOS).**

***Index Terms*— DeMOS, Drain-extended FinFET (DeFinFET), drain-extended MOS, laterally double diffused MOS (LDMOS), PwrSoC, SoC.**

I. Introduction

FinFET technology at 14 nm node is equipped with full suite of analog/radio frequency (RF) features catering to functionalities up-to 3.3 V [1]. However, for advance SoC applications [2], high-voltage (HV) devices with >5 V rating are desired to enable a wider range of functionalities on chip like RF-PA, power management circuits, dc–dc converters, and so on. This gap can potentially be filled by stacking of the medium voltage transistors, which is one of the approach to scale up the voltage handling capability of a design. However, attributed to aggressive scaling in advance CMOS nodes, transistor stacking is not a preferred option due to intrinsic reliability concerns [3]–[5]. Other approach is to enable a HV device using drain extension [6]. Due to its CMOS process compatibility, HV drain-extended MOS devices in the preceding planar nodes have successfully enabled HV (5–20 V) functionalities, which has fueled the advanced SoC development [7]–[10]. Going forward to Fin-based technologies, drain-extended FinFET (DeFinFET) seem a much viable option. However, in a Fin-based technology, drain-extended solutions [11], [12] for HV options have not yet been adapted. Due to thin silicon volume in Fin technology [13], the performance and reliability assurance at higher voltage is questionable [11], [14], [15]. Furthermore, high ON-resistance (R_{ON}) caused by the Fins, and Fin technology-based design rules makes the drain extended device design much more challenging [16] than its planar counterpart.

In this work, the performance and reliability figure of merit (FOM) of various DeFinFET and Stacked FETs are investigated through device circuit codesign. dc–dc converters and RF-PA performance was used as a vehicle to establish the circuit performance tradeoff between DeFinFETs, stacked FinFET, and planar DeMOS concepts. This article is arranged as follows: Section II compares the performance of various HV options in FinFET node with its planar counterpart. Device-circuit interaction studies are performed in Section III. Section IV briefly compares the electrostatic discharge (ESD) and hot carrier immunity (HCI) of these HV device options. Finally, Section V concludes this work.

II. Device Design and Performance Tradeoff

A. HV Device Options in FinFET Nodes

Fig. 1 shows various HV FET options in ultrascaled CMOS nodes, which are employed in this study for the comparative study. Fig. 1(a) and (d) shows the cross-sectional view of planar DeMOS and shallow trench isolation (STI)-DeMOS devices, respectively. In this work planar, DeMOS has been used for bench-marking DeFinFET device's and circuit performance. Two variants of DeMOS have been used. One with 28 nm equivalent wells (i.e., deep well), to realize DeMOS using 28-nm CMOS process. For completeness, DeMOS using a shallower well, that is wells same as deployed in 14 nm process, has also been used. The same shallower well profile has been used for all DeFinFET options explored. Fig. 1(b), (c), (e), and (f) shows cross-sectional and 3-D

Manuscript received February 11, 2020; revised July 8, 2020; accepted August 25, 2020. Date of publication September 21, 2020; date of current version October 22, 2020. This work was supported by the IMPRINT Program through the Ministry of Human Resource and Development and Department of Science and Technology, Government of India. The review of this article was arranged by Editor H. Wong. *(Corresponding author: B. Sampath Kumar.)*

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Digital Object Identifier 10.1109/TED.2020.3020904

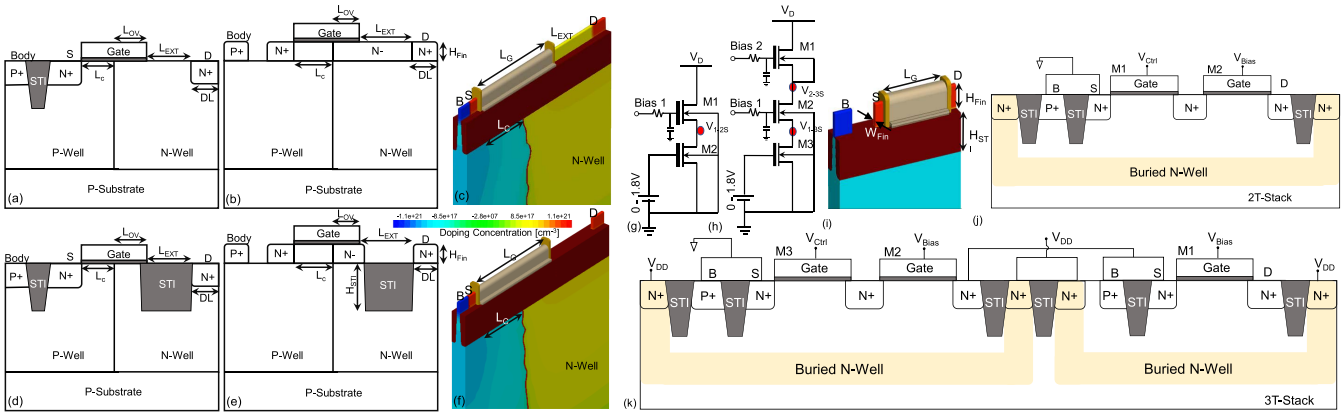

Fig. 1. Drain-extended devices employed for the comparative study: (a) cross-sectional view of drain-extended MOS (DeMOS) device, as used in planar nodes for HV implementation, (b) cross-sectional view of DeFinFET without STI in the drift region (nonSTI-DeFinFET), (c) 3-D view of nonSTI-DeFinFET, (d) cross-sectional view of drain-extended MOS with STI in drift region (STI-DeMOS) device, as used in planar nodes for HV implementation, (e) cross-sectional view of DeFinFET with STI in the drift region (STI-DeFinFET), (f) 3-D view of STI-DeFinFET, (g) and (h) circuit view of 2× and 3× stacked configuration with the respective biasing scheme, (i) 3-D view of FinFET used in stacking, (j) cross-sectional view of stacked FinFET (2×) with well isolation scheme (2 transistors stacked to realize 3.3 V capability), and (k) cross-sectional view of stacked FinFET (3×) with well isolation scheme (three transistors stacked to realize 5 V capability).

views, respectively, of DeFinFET and STI-DeFinFET. Furthermore, Fig. 1(j) and (k) show cross-sectional view of stacked FinFET concept to enable HV handling capability, having 2 and 3 nos. of transistors in the stack, respectively. It is worth noting the well isolation scheme is used with deep buried wells. Not more than two transistors are stacked inside a common P-well, while keeping individual P-Wells isolated by deeper N-Wells. Fig. 1(g) and (h) show the circuit view of 2× and 3× stacked configurations with the respective biasing scheme and local substrate connections. It should be noted that the deeper wells have 3× higher breakdown voltage than the maximum voltage handling capability of stack concepts; therefore, the breakdown voltage of the stack configuration is limited by local drain (N+) to P-well breakdown voltage.

For this work, a well-calibrated 3-D process and device simulation setup was used, as reported in our earlier work [17]. For both the types of DeFinFETs, N-well shallower than typically used in planar 28 nm process is used. Well profile and other device design parameters for respective devices were optimized with the help of a detailed design-of-experiment simulation for maximizing breakdown voltage—ON-resistance tradeoff. Devices having least ON-resistance for a given breakdown voltage were selected for this study while keeping their onset of quasi-saturation to be as high as possible [11]. The breakdown voltage is chosen to be close to 2× of supply voltage. With this design approach, stacked MOS configuration for 3.3 and 5 V operation, nonSTI-DeFinFET for 3.3 and 5 V operation, STI-DeFinFET for 7 V operation, planar DeMOS for 5 and 7 V operations are used for the comparative assessment in this work. On the one hand, stacked concepts require a certain biasing and well connection schemes, while ensuring gate oxide immunity and no internal latch up. On the other hand, DeFinFET only requires a dedicated HV N-well. The lateral design parameters in conjunction with N-well profile are required to be optimized to maximize breakdown voltage—ON-resistance tradeoff while mitigating quasi-saturation effect [18], [19]. Fig. 2 depicts

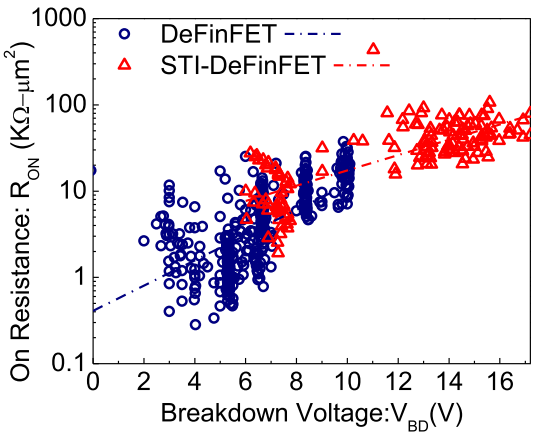

Fig. 2. ON-resistance and breakdown voltage extracted using a detailed DOE simulations of nonSTI-DeFinFET and STI-DeFinFET. DOE simulation was performed to select optimized DeFinFET designs for three different voltage classes with least ON-resistance and mitigated quasi-saturation effect.

R_{ON} versus V_{BD} tradeoff for DeFinFET devices, extracted using a detailed design of experiments (DOE) simulation. DeFinFET devices with least R_{ON} for a given V_{BD} have been selected for following three class of voltage 3.3, 5, and 7 V while maximizing the onset of quasi-saturation [11]. The same has been compared with stack FinFET and DeMOS configurations. The optimum values of design parameters of various drain-extended concepts studied are listed in Table I.

B. Performance Tradeoff

Fig. 3(a) and (b) shows R_{ON} and R_{ON-sp} comparison of stacked FinFET and DeFinFETs for various voltage classes. (Specific ON-resistance R_{ON-sp} is resistance per unit area of the design, Note: for stacked FinFET entire design configuration area is considered to measure R_{ON-sp}) DeFinFET show higher R_{ON} when compared to stack concepts, which

TABLE I

SUMMARY OF DEVICE DESIGN PARAMETERS. FOLLOWING ARE THE PARAMETER VALUES COMMON TO ALL THE DESIGNS: N-WELL DOPING = $3 \times^{17}$ cm^{-3}, P-WELL DOPING = $2 \times^{18}$ cm^{-3}, GATE OXIDE THICKNESS (T_{OX}) = 2 nm (EOT), FIN HEIGHT (H_{FIN}) = 40 nm, FIN WIDTH (W_{FIN}) = 8 nm, BURIED WELL DOPING = $5 \times^{16}$ cm^{-3}

Parameter	DeMOS (Shallow Well)	DeMOS (Deep Well)	DeFinFET (3.3V)	DeFinFET (5V)	STI-DeFinFET (7V)
Gate Length(L_G)	350nm	350nm	190nm	250nm	350nm
Gate Overlap on NWell (L_{OV})	140nm	140nm	100nm	120nm	160nm
Length (L_C)	210nm	210nm	90nm	130nm	190nm
Drain extension Length (L_{EXT})	200nm	200nm	100nm	200nm	220nm
STI Height (H_{STI})	100nm	200nm	NA	NA	100nm
Well Depth	800nm	1400nm	600nm	600nm	600nm
Drain Contact Length (DL)	250nm	250nm	70nm	70nm	250nm

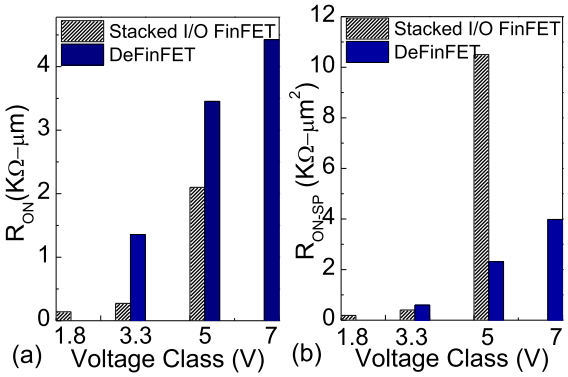

Fig. 3. Comparison of (a) R_{ON} per unit device width and (b) specific ON-resistance (R_{ON-SP}) of stacked FinFET and DeFinFET for different voltage class.

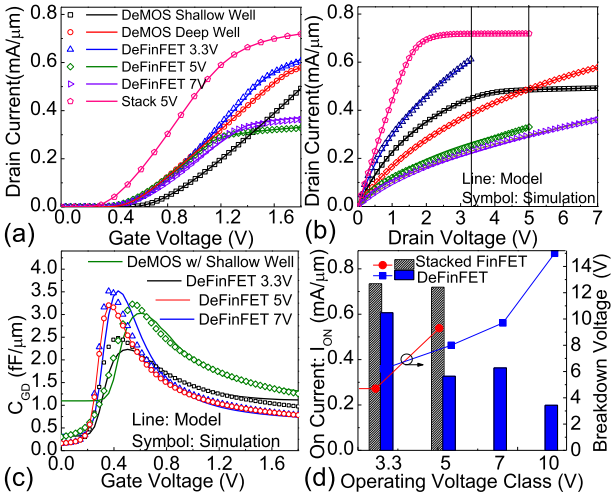

Fig. 4. (a) Transfer characteristics, i.e., I_{DS} versus V_{GS}. (b) Output characteristics, i.e., I_{DS} versus V_{DS}. (c) Miller capacitance, i.e., C_{GD} versus V_{GS}. (d) On current as well as breakdown voltage (V_{BD}) comparison of various HV configurations used for comparative assessment in this work. While symbols show data extracted from TCAD simulations, line depicts perfect matching of model with TCAD data.

is attributed to fin enabled drift region in DeFinFETs. Unlike planar, Fin-based drift region increases the drift region resistance by a factor of $(W_{\text{Fin}} + F_{\text{Pitch}})/W_{\text{Fin}}$, where W_{Fin} is Fin width and F_{Pitch} is Fin pitch. On the other hand, the added area due to well isolation required in stacked design, stacked FET design has higher specific ON-resistance (R_{ON}), as depicted in Fig. 3(b), when compared to DeFinFETs, for voltage class above 3.3 V. Inclusion of well isolation significantly adds to the total layout area.

Fig. 4(a) and (b) shows the transfer and output characteristic comparison of stack configuration (3.3 and 5 V), DeFinFETs (3.3, 5, and 7 V) and planar DeMOS. For one to one comparison and also study the implications of technology scaling deep and shallow well DeMOS devices are considered. Here deep wells are standard wells used in 28 nm planar CMOS (DeMOS) process. Whereas shallow wells are same as used in 14-nm FinFET process (DeFinFET). For one to one comparison, planar DeMOS having shallow wells are also used for comparison. Fig. 4(a) and (b) shows that the stacked FinFET concept provides higher drive current than DeFinFET. This is attributed to higher transconductance of stacked FinFET design due to lower gate lengths and reduced drain resistance. DeFinFET, on the other hand, suffers from early quasi-saturation. Quasi-saturation in DeFinFETs is discussed in the following section. Fig. 4(c) shows the C_{GD} comparison of drain extended devices. Quasi-saturation imposes nonlinear C_{GD} in all HV drain extended devices. Fig. 4(d) shows the breakdown voltage and ON current performance among stacks and HV devices. Extending V_{BD} above 3.3 V is convenient in DeFinFET when compared to stacked FinFET. For increasing operating voltage above 5 V STI-based design was opted for DeMOS and DeFinFET. Higher OFF-state breakdown (V_{BD}) is achievable using DeFinFET by facilitating reduced surface electric field, whereas stacked FET concept is prone to lower OFF-state breakdown voltage, as depicted in Fig. 4(d). This is attributed to lower drift doping in DeFinFETs whereas, standard FinFET cells with high doped Source/Drain terminated over the P-well are prone to early junction breakdown. Fig. 4(a)–(c) also show perfect matching of the model with TCAD data. The extracted model card is used for circuit design, simulation, and assessments.

C. Quasi Saturation in HV Devices

Fig. 5(a) shows saturation in drain current as a function of gate voltage (V_{GS}) in stacked FinFET and DeFinFET design. Saturation in drain current results into added nonlinearity in miller capacitance and fall in transconductance at higher gate voltages [19], [20]. This limits the gate overdrive in HV

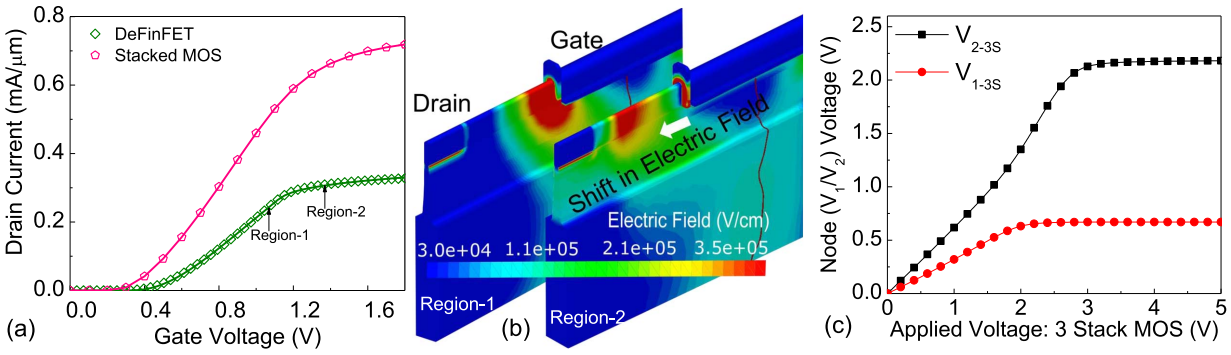

Fig. 5. (a) Saturation in drain current as a function of gate voltage (V_{GS}) in stacked FinFET and DeFinFET design. (b) Electric field contour depicting shift in electric field in DeFinFET from the gate edge to drain contact at the onset of quasi-saturation. (c) Potential across intermediate (floating) nodes of stacked FinFET design, shown in Fig. 1(h), as a function of drain voltage (V_{DS}).

designs. In DeFinFET, the root cause of the saturation behavior observed is onset of space charge modulation, which results in shift in peak electric field, as depicted in Fig. 5(b), from gate edge to drain edge. This shift leads to electric-field localization and peaking at drain contact, which results in mobility degradation and loss of gate control over channel current. Collectively these aspects result into the quasi-saturation behavior [14], [18]. On the other hand, in stacked design, the observed drain current saturation is attributed to the imbalance in the drain-to-source voltage drop across individual transistors in the stacked configuration. Fig. 5(c) shows an imbalance in drain-to-source voltage drop across individual transistors of stacked FinFET design. This pushes the driving transistor (the bottom most in the stacked configuration) into the linear region and make the drain-to-source voltage drop independent of applied supply voltage, which causes the drain current to become insensitive to gate voltage. Furthermore, the imbalance also leads to significantly higher drop across upper most transistors in the stack, which makes them more vulnerable to hot carrier stress.

III. Device–Circuit Interaction

As discussed in the previous section, different designs offer distinct characteristics both in terms of transistor behavior and the nature of parasitics involved. Therefore, it is not trivial to assess the relative performance of circuits designed out of these devices as far as HV functionality in SoC is concerned. Circuit blocks which consume most of the area and always stood as challenging designs for SoC integration are RF-PA and on-chip power management (dc–dc converter) modules. Therefore, it is worth assessing the circuit capability of various HV options, as discussed in earlier sections, while keeping the needs of these two circuit in mind.

For circuit analysis, I–V and C–V family of curves extracted using 3-D TCAD are used to develop model card for various devices using Keysight's ICCAP Device modeling suit and industrial standard Berkeley short channel IGFET model (BSIM) CMG 110.0.0 and HiSiM HV 2.3.1 models. Besides, the S-parameters extracted using model card were also matched with TCAD extracted S-parameters, as depicted in Fig. 6. Post dc, C–V and S-parameter matching, load-pull simulations were carried out using Keysight's ADS for PAs

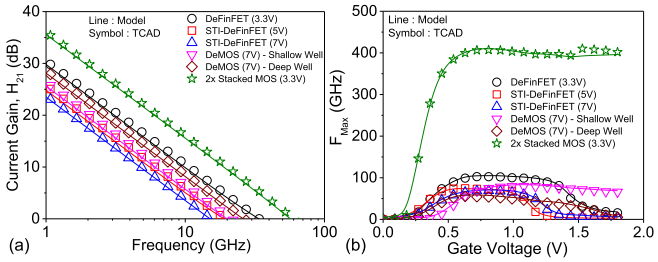

Fig. 6. (a) Current gain as a function of frequency. (b) Max oscillation frequency as a function of gate voltage. Symbols depicts H_{21} and F_{Max} extracted using TCAD, where line depict the same extracted using model matched to TCAD I–V and C–V data.

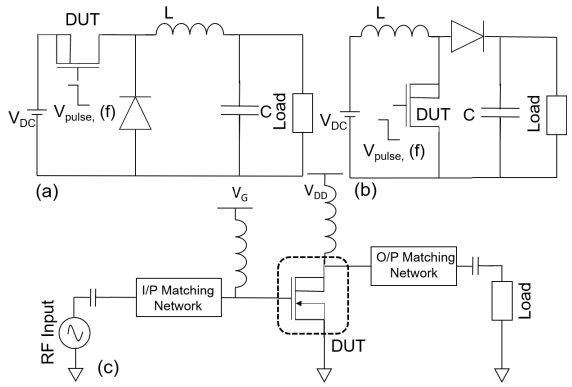

Fig. 7. Schematic of (a) dc–dc buck converter, (b) dc–dc boost converter, and (c) RF-PA circuit. For dc–dc conversion, 3.3 V has been chosen as input, which is the typical battery voltage in current days hand-held systems.

biased in class-AB. Load-pull simulations are performed by tuning the input and output matching networks, such that the maximum power is delivered to the load. For dc–dc converter design, both buck and boost configurations were used.

A. DC–DC Convertor

The buck converter, as depicted in Fig. 7(a), designed here assumes high load condition with load current approaching up to 1 A, which is a typical case in advance SoCs. Here buck converter down converts battery voltage of 3.3 V to the core

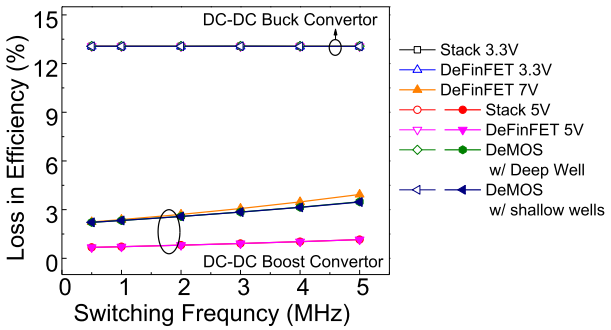

Fig. 8. Percentage loss in power across various HV switch options in simulated dc–dc buck and boost convertors.

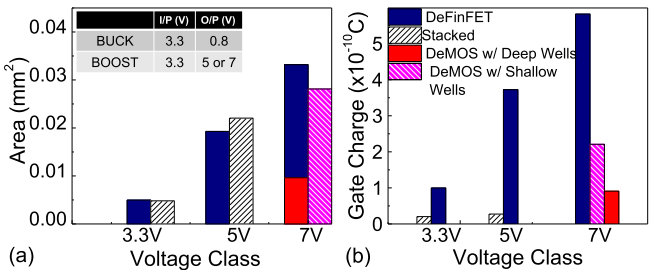

Fig. 9. (a) Device footprint area and (b) gate charge of the power switch compared for both buck and boost converters designed using various drain extended and stack-based HV concepts.

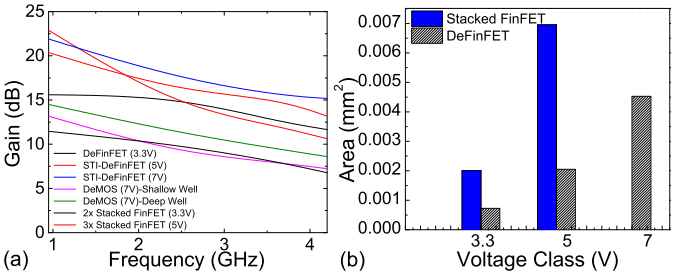

Fig. 10. (a) RF-PA gain with respect to PA frequency for various HV device options and (b) device foot print of stacked and DeFinFET designs used in RA-PA circuit.

voltage of 0.8 V. Circuits were designed using various HV options by keeping their absolute R_{ON} fixed (0.12 Ω). Given the absolute R_{ON} of individual HV device was considered fixed and in sub-14 nm technology parasitic capacitances are minimal, Fig. 8 shows the percentage loss in efficiency in buck converters designed using various HV device options was found to be identical. However, a difference in percentage loss in efficiency while up converting a battery voltage of 3.3 V to PA supply voltage of 6 V was noticed while using a reference circuit depicted in Fig. 7(b). In this case, DeFinFET was found to be superior when compared to staked design as well as planar DeMOS options.

It should however, be noted that % loss in efficiency is not the only FOM. Gate charge defines the capacitance loading on the gate driver circuitry. Higher the gate charge, higher the dynamic power loss will be. Moreover, footprint area occupied by power MOS device decides the cost of the chip. Fig. 9(a) shows that the stack concept occupies increasingly higher area compared to DeFinFETs, for voltage classes above 3.3 V. Both however, would consume same area with 3.3 V concept. However, since special biasing circuit is required for stack configuration, its implicit that stacked configuration will consume higher chip area when compared to 3.3 V DeFinFET. Fig. 9(b) shows gate charge contributed by stacked configuration to be significantly smaller when compared to DeFinFET and planar DeMOS. In all cases planar DeMOS always offers lower chip area and lower gate charge when compared to DeFinFET. Therefore, it can be concluded that DeFinFETs are more viable options when compared to the stacked counterparts if chip area is of concern. If dynamic power loss of the gate driver circuitry is of concern then DeFinFET under perform the stacked configuration as well as planar DeMOS.

B. RF-Power Amplifier

RF-PA, as depicted in Fig. 7(c), was realized using dual tone load pull approach in class AB operation. Sizes of all the devices independent of voltage class was adjusted to have a peak current of 1 A. Fig. 10(a) and (b) shows the gain versus frequency and device foot print, respectively, for PF-PA designed using different HV device options. Fig. 10(a) shows while RF-PA gain of planar DeMOS device falls significantly with increasing frequency of operation (gain = 5 at 2 GHz), DeFinFETs offer higher gain with RF-PA operation for an extended range of frequencies (gain = 5 at 6 GHz). The improved gain-bandwidth product in DeFinFET is attributed to Fin-based geometry leading better gate to channel control, which improves transconductance and mitigates nonlinearity in parasitic capacitance. Furthermore, stack-based concept was found to offer RF-PA operation for widest range of frequencies (gain = 5 at 10 GHz). The highest gain-bandwidth product of stacked FinFET design is attributed to intrinsically higher cut-off frequency of FinFET. However, on the other hand, stack-based concept requires a significantly higher (>2-3×) device foot print, which adds to overall chip cost. With increase in voltage handling capability, the stack concept's area requirement increases too, as shown in Fig. 10(b).

Gain-Bandwidth product and device foot area are not the only FOM parameters for RF-PA. Linearity is a key attribute of RF-PA. To investigate linearity third order intermodulation distortion (IMD3) was simulated using a two tone load-pull circuit with 1 MHz spacing frequency. Fig. 11 shows comparison of power delivered, power added efficiency (PAE), gain and intermodulation distortion (IMD3), as a function of input power, of the RF-PA circuit designed using different HV device options for three different frequencies, that is 950 MHz, 2.4 and 4.2 GHz, to study usability of DeFinFET devices for 5G applications. At 950 MHz, the 7 and 5 V DeFinFET devices delivered largest output power as well as gain, whereas 3.3, 5, and 7 V DeFinFETs offer highest efficiency. 7 V DeFinFET offers slightly higher efficiency than 5 V designs. However, 7-V DeFinFETs and deep well DeMOS offer the maximum linearity behavior. It can be notice that at 2.4 and 4.2 GHz, 3.3, 5, and 7 V DeFinFETs perform better than other devices in terms of output power, gain,

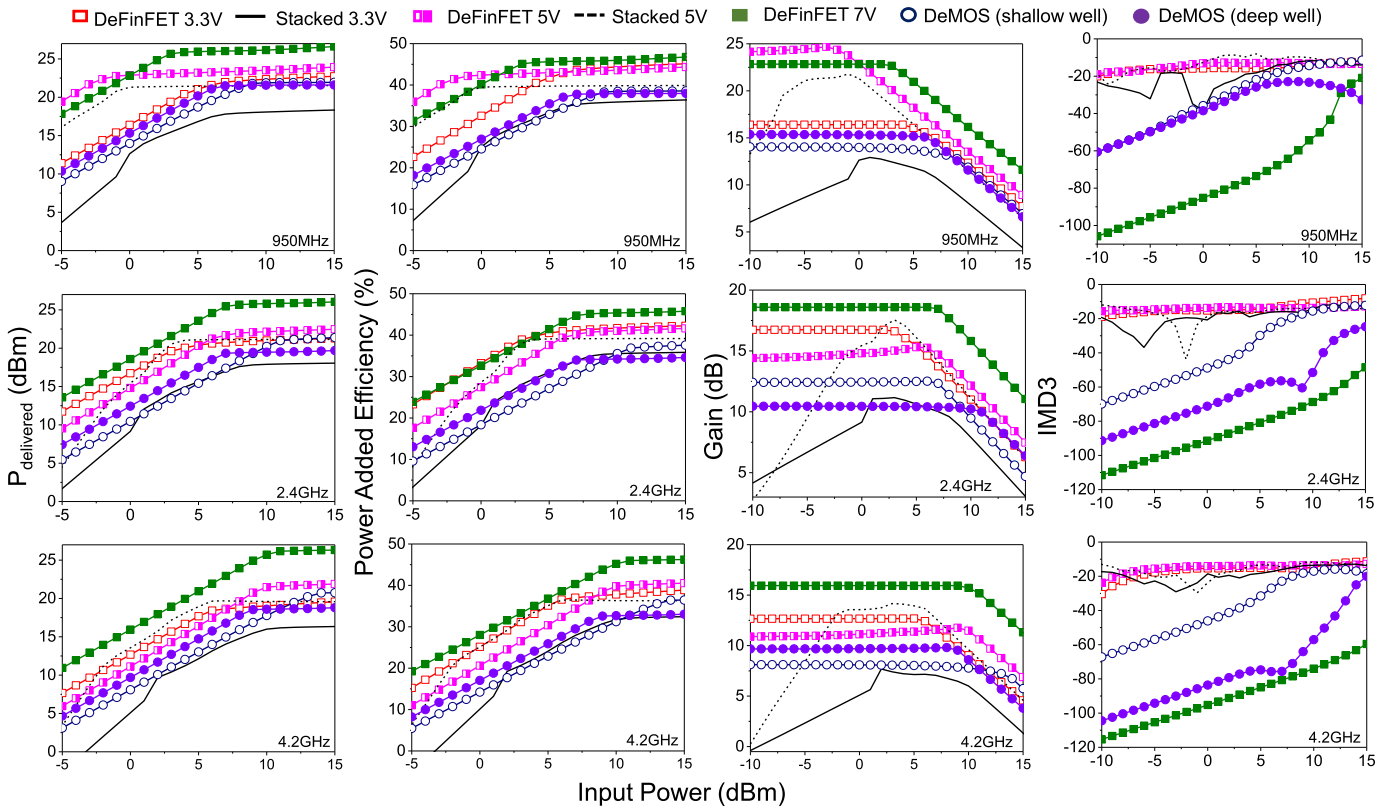

Fig. 11. RF-PA FOM parameters of various HV design options investigated.

and efficiency. Stacked FinFET's RF-PA performance falls significantly, particularly linearity, with increasing frequency. In general stacked FinFETs offered lower power, gain, efficiency, and IMD3 performance than DeFinFET and DeMOS. It can therefore, be concluded that RF-PA performance of STI-DeFinFET in terms of power delivered, PAE and gain for an optimum input power were found to be on par with the same achieved by stacked counterpart. Interestingly, DeFinFETs were found to be superior compared to the planar DeMOS. STI-DeFinFETs were also found to have lower IMD3 when compared to stacked FinFET as well as planar DeMOS. While stack concept offers finite PAE, output power and gain, its inferior IMD3 behavior and higher area requirements questions its applicability for RF-PAs in advance SoCs. This indicates superiority of STI-DeFinFETs over planar as well as stacked-FinFET counterparts and their applicability for SoC designs for 5G applications.

IV. Reliability Assessment

A. ESD Robustness

I/O peripherals are often driven by HV devices, which in turn become vulnerable to ESD events/threats. In such cases, protection of HV devices against ESD surges is quite essential. The other approach is make the driver transistors self-protected, which however, require large driver size. In any case, ESD robustness of these HV/driver transistors must be maximized. Fig. 12(a) shows the transmission line pulsing (TLP) I–V characteristics of various HV options. Fig. 12(b) shows the holding voltage (V_{HOLD}) of stacked

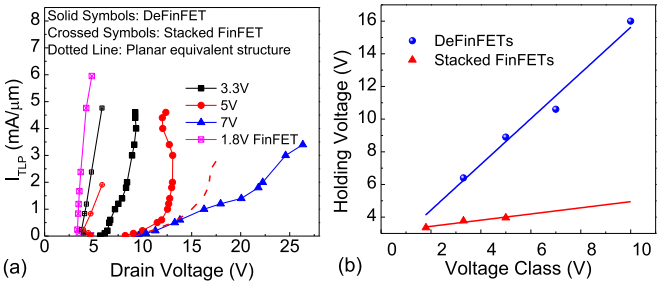

Fig. 12. (a) TLP I–V characteristics of stacked FinFETs, DeFinFETs and their planar counterparts. (b) Holding voltage versus operating voltage for stacked FinFET design and DeFinFETs. 5 V DeFinFET offers optimum self-protection capability in terms of It2 and V_{HOLD}.

design and DeFinFETs, with respect to voltage class. Fig. 12 shows that for stacked concepts, as the voltage rating reaches 5 V, intrinsic breakdown voltage of the DeFinFET limits the holding voltage. Moreover, while ESD failure current falls with increasing number of transistors in the stack, holding voltage doesn't scale linearly with number of transistors in the stacks. This makes stacked design an inferior option in terms of ESD robustness, when compared to DeFinFETs. DeFinFETs depict higher ESD robustness (It2) than the stack design, both in terms of blocking voltage, as well as, ESD failure current per unit device area. Moreover, it should be noted that DeFinFET offers better ESD robustness than their planar counterparts, which in another work is attributed to the presence of spreading filaments in DeFinFET [21].

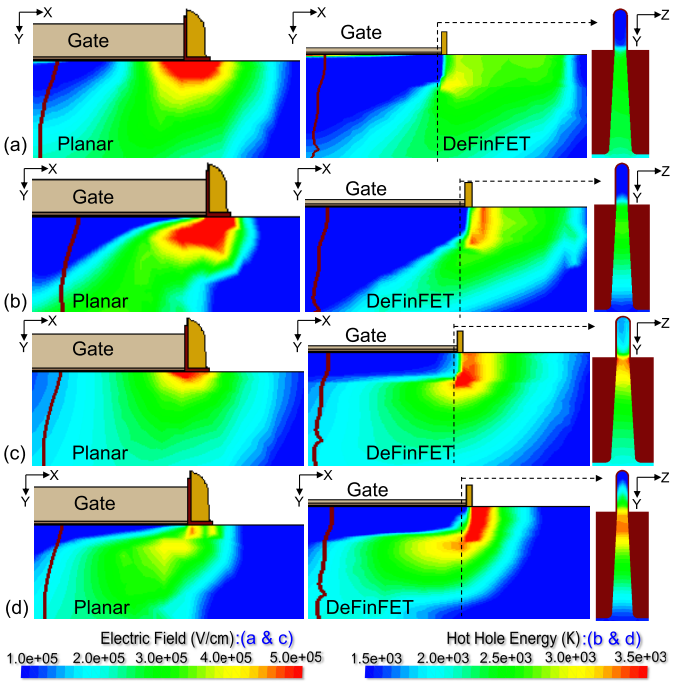

Fig. 13. (a) and (c) Electric field and (b) and (d) hole energy distribution across the drift region of of planar DeMOS (left) and DeFinFET (right) devices, under (a) and (b) ON-state and (c) and (d) OFF-state operation. Here 5 V class of devices were stressed for 10 000 s before extracting electric field and hole energy profile. The hot carrier population was accounted by solving the Spherical Harmonic Expansion of Boltzmann [22] Transport Equation with stress equivalent to maximum allowed drain voltage (V_D) and (a) gate bias = V_{GS} at maximum substrate leakage at $V_D = V_{MAX}$ for ON-state or (b) gate bias = 0 for OFF-state.

B. Hot Carrier Behavior

Hot carrier reliability (HCI) is one of the major bottlenecks for HV devices in SoC applications [7]. Particularly, hot hole generation in drain-extended devices, under both ON and OFF-state stress, leads to early time dependent dielectric breakdown of gate oxide in the gate-N-well overlap region [5]. HCI reliability simulation framework is performed using spherical harmonic expansion of Boltzmann transport equation (BTE) [22], [23] Fig. 13(a) and (b) shows electric field and hole energy distribution across drift region, near the gate edge, in the ON-state operation of planar DeMOS (left) and DeFinFET (right) devices. The same under OFF-state is depicted in Fig. 13(c) and (d). In both the scenarios, DeFinFET device has lower hot hole density due to fully depleted nature of Fin in DeFinFET. Besides, DeFinFET also has lesser influence of hot holes as the hot holes are relatively away from the gate overlap, when compared to DeMOS device. This is attributed to relaxed electric field in the gate overlap (Fin) region in DeFinFET, when compared to planar DeMOS, which is attributed to fully depleted nature of the Fin. Thus, it can be extrapolated that DeFinFETs must have higher immunity toward hot carrier stress when compared to DeMOS device of the same voltage class.

V. Conclusion

HV device integration in FinFET nodes is one of the key requirement to enable advance SoCs in sub-14 nm nodes. Stacked FinFET and DeFinFETs are the possible contenders for HV integration. Device circuit codesign and reliability analysis performed in this work reveals that at lower voltages (3.3 V) stack FinFET design suffice the power management module requirements. However, for applications above 3.3 V operation, DeFinFETs are area efficient for voltage conversion applications. Furthermore, unlike planar technologies, DeFinFET stands as a promising contender for high-frequency high-power PA modules for enabling on-chip 5G functionalities in FinFET nodes. DeFinFETs were found to have a superior overall PA performance when compared to stacked (and planar) counterparts. DeFinFETs were also found to be highly reliable against ESD and HCI stress, when compared to stacked counterpart.

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