Engineering Schemes for Bulk FinFET to Simultaneously Improve ESD/Latch-Up Behavior and Hot Carrier Reliability

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***Abstract*— This article presents a simultaneous impact of selective contact silicidation, silicide, and junction engineering on bulk FinFET's electrostatic discharge (ESD) reliability, latch-up (LU) robustness, and hot carrier-induced (HCI) degradation. The investigations are performed using 3-D TCAD simulations. To maximize the robustness against HCI reliability and to improve the ESD/LU performance simultaneously, essential technology guidelines are derived based on physical insights developed. With the incorporation of proposed S/D contact silicide and junction engineering, the ESD robustness of FinFETs can be improved by a factor of 6× compared to conventional approaches. Besides, this is found to improve the overall HCI reliability of bulk FinFETs. Based on these design guidelines, hybrid contact/junction engineered scheme is proposed for the overall robustness of FinFET system-on-chips (SoC).**

***Index Terms*— Bulk FinFET, electrostatic discharge (ESD), hot carrier-induced (HCI) degradation, silicidation.**

I. Introduction

BULK FinFET has become the dominant CMOS technology in semiconductor industry in the past few years owing to its improved scalability and high performance [1]. While bulk FinFET enjoys a lower footprint and higher performance [2], [3], FinFET nodes, however, have become vulnerable to electrostatic discharge (ESD) [4], self-heating [5], overvoltage, and hot carrier-induced (HCI) degradation [6]–[13]. Besides, bulk FinFET nodes also have missing high voltage components [14], [15] and advance ESD protection devices [16], [17]. If these issues are addressed, the projections are that Bulk FinFET will become the mainstream technology for system-on-chip (SoC) platforms.

ESD, latch-up (LU), and HCI reliability of these devices have earlier been studied in detail [4], [6]–[13], [16], [18]. These investigations, however, were often conducted independent to each other, without deriving any tradeoff between ESD, HCI, and LU robustness. The impact of the guidelines proposed to improve HCI reliability has not been explored yet in the context of ESD reliability. Similarly, the impact of design/technology/layout engineering approaches proposed to improve the ESD behavior of bulk FinFETs has yet not been explored in HCI context. For example, the recent study has shown that, by exercising contact silicidation and junction profile engineering, the efficiency of the parasitic bipolar of bulk Fin-based SCR ESD protection devices can be improved [16], [17]. However, the implications of silicide/junction/contact engineering on HCI reliability are not known yet. The question is that can the technology approaches developed for improving the ESD behavior of Fin-SCRs be deployed to FinFETs used in core or I/O circuits? How these approaches would affect the HCI reliability? Similarly, silicide blocking (SB) and drain junction engineering are frequently used techniques to improve the ESD behavior of I/O and core transistors. However, the implications of techniques such as SB and drain junction engineering on HCI reliability are missing in the literature. These explorations, however, become relevant to realize ESD as well as HCI robust I/O and core devices in the same technology while enabling robust ESD protection devices and high LU robustness of overall technology platform. This is essential for the overall robustness of FinFET SoCs.

Keeping these points in mind, this article focusses on exploring newer device design methodology and guidelines to achieve the overall robustness of FinFET technology for system-on-chip platforms. In this article which improves and extends the earlier findings in [19], we have addressed these missing aspects to derive novel contact/junction engineering schemes and design guidelines to achieve the overall robustness of bulk FinFET technology. Section II presents the TCAD simulation methodology adopted for this article. Furthermore, Sections III and IV discuss the impact of various design/layout/technology parameters on tradeoff between ESD

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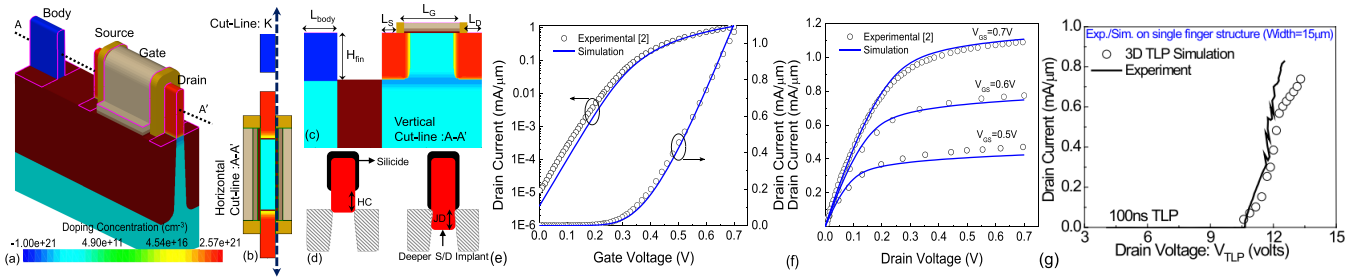

Fig. 1. (a) Isometric view, (b), and (c) cross-sectional view of FinFET platform used for ESD, LU, and HCI reliability investigations, (d) contact engineering by partial silicidation as a function of HC, and junction engineering by using deeper implants (JD) for improved ESD robustness [16], [17], (e)–(g) TCAD calibration of mobility models, quantum confinement effects in MOS operation, and avalanche breakdown as well as high current conduction. For all investigations, H_{STI}, H_{FIN}, and W_{FIN} were considered to 70, 42, and 8 nm, respectively. An effective oxide thickness (EOT) of 2 nm and L_G of 50 nm were considered for FinFET devices, which are typical dimensions for an I/O device in FinFET node, which is expected to experience both HCI and ESD stress. Note: here, JD $>$ 0 represents S/D junction formed inside the inactive Fin, whereas JD $<$ 0 represents partially doped active Fin with S/D junction formed inside the active Fin.

and HCI reliability. With the corresponding findings, a novel hybrid contact silicidation/junction profile engineering design scheme is proposed in Section V, to improve the overall robustness of bulk FinFET technology. Finally, the new findings are concluded in Section VI.

II. Computational Methodology

ESD and HCI investigations are performed using 3-D electrothermal TCAD simulations [20]. Fig. 1(a)–(c) shows the isometric and cross-sectional views of bulk FinFET platform considered in this article for ESD and HCI investigations. Device engineering parameters such as junction depth (JD) and contact height (HC) are shown in Fig. 1(d). The HC, or the partial contact silicidation height, is defined as the height from the lower portion of the active Fin region, above which the Fin is silicided. The JD is defined as the diffusion depth of the source/drain implants, beneath the active region of the Fin. These parameters were earlier introduced in [16] and [17]. TCAD simulation setup used for this article was calibrated against the experimental data to account for carrier transport in Fin region, quantum confinement effect, avalanche breakdown, and high current conduction, as shown in Fig. 1(e)–(g). To accurately account for the self-heating and heat dissipation effects under both ESD and HCI stress investigations, self-consistent heat equation was solved while accounting for 1) back end of the line (BEOL) metal interconnect stack; 2) Si substrate thickness; and 3) neighboring Si region offering thermal diffusion around the active Fin device. These strongly influence the thermal boundary condition around the active Fin device under stress. Transmission line pulse (TLP) I–V simulations were performed to study the ESD behavior using 100-ns pulse stress (rise time = 10 ns) with increasing pulse amplitude after each pulse stress. Stress-measure-stress routine was performed for HCI stress simulations with 50 000-s long stress pulse with device's I–V extraction in between the stress routine. The hot carrier population and thereby induced degradation were accounted by solving the spherical harmonic expansion of Boltzmann transport equation with stress equivalent to maximum allowed drain voltage (V_D) and gate bias = $V_D/2$ [21], [22]. The stress voltage levels were chosen to establish the maximum HCI degradation in accordance with a recent analysis on the HCI behavior of bulk FinFETs [6]. In order to accurately reflect the physics of Si-H bond breakage and interface trap generation process, hot carrier stress (HCS) degradation model was applied, through the depassivation of hydrogen (H) and subsequent H transport toward the silicon-oxide interface [20], [23], [24].

III. Contact and Junction Engineering: ESD and HCI Tradeoff

Fig. 2(a) and (b) shows the TLP I–V characteristics of grounded gate FinFET. Fig. 2(d) and (e) shows the same for Fin-enabled SCR devices [schematic shown in Fig. 2(c)]. Fig. 2 shows an improved ESD robustness for HC $>$ 0 and/or JD $>$ 0. With HC $>$ 0 (for JD = 0) and/or JD $>$ 0 (for HC = 0), FinSCR offers improved It2 and deeper snapback, when compared to the designs with HC = 0 nm JD = 0 nm. This is attributed to the improved parasitic bipolar efficiency when contact silicidation was moved away from N^+/P-Well junction, by increasing HC [Fig. 1(d)], as shown in Fig. 2(f). The devices with HC $\leq$ |-JD| (for JD $\leq$ 0), on the other hand, offers the poorest bipolar turn-on and SCR action, which is due to significantly increased minority carrier recombination when contact silicidation overlaps the N^+/P-well junction [16], [17]. Parasitic SCR paths with HC = JD = 0, and in general, HC $\leq$ |-JD| (for JD $\leq$ 0), were found to have the highest LU robustness. The contact and junction engineering apparently were found to alter the channel field profile, as shown in Fig. 3(a), and thermal interface resistance, which results in a change in hot carrier distribution across the channel [Fig. 3(b)]. For example, for HC $>$ 0 and/or JD $>$ 0, a device experiences a lower peak E-field, which results in lower electron energy. On the other hand, as the silicide region gets closer to S/D junction, E-field broadens with an increased peak. This increases the carrier energy across the channel, near the drain-channel junction. This can favorably or adversely affect the hot carrier degradation of FinFETs engineered for improved ESD or LU robustness. Keeping this in mind, it is worth exploring HCI degradation as a function of Fin and S/D engineering, which is discussed in detail as follows.

As shown in Fig. 1(d), partial contact silicidation (HC $>$ 0) effectively lowers the contact area over the source/drain region.

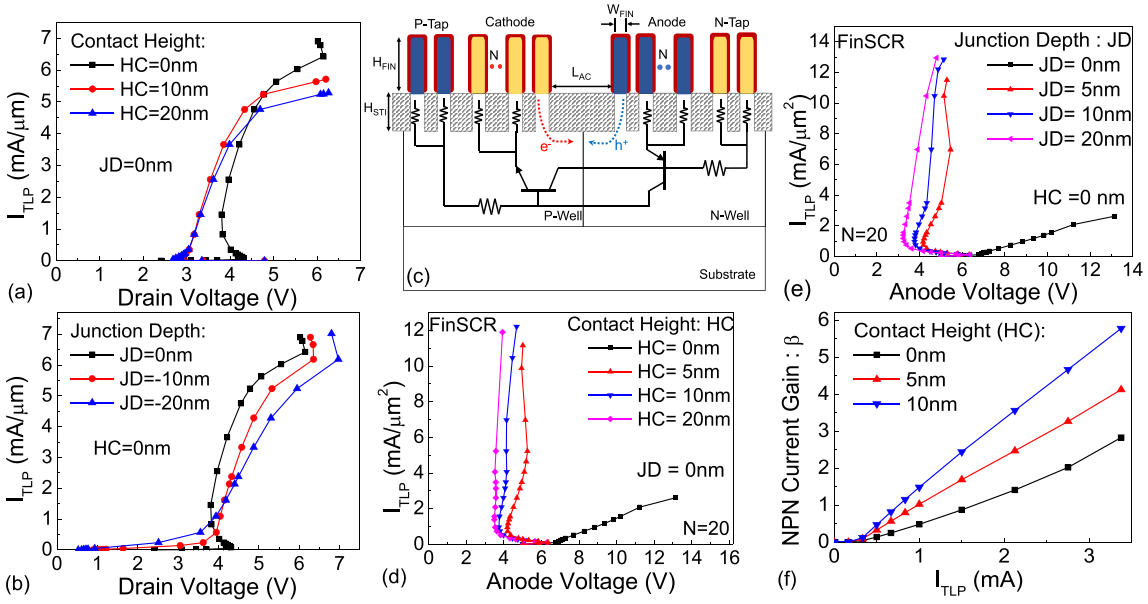

Fig. 2. TLP *I–V* characteristics of (a) and (b) ggFinFET and (d) and (e) FinSCR [depicted in (c)] with contact and junction engineering, respectively. (f) Parasitic bipolar efficiently as a function of HC.

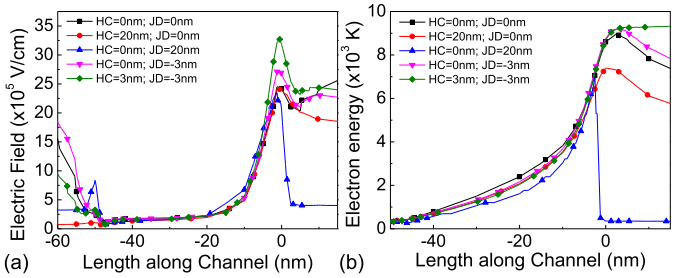

Fig. 3. (a) Electric field distribution and (b) electron energy extracted along the channel, post 50 000 s of stress, as a function of contact/silicide height and relative JDs.

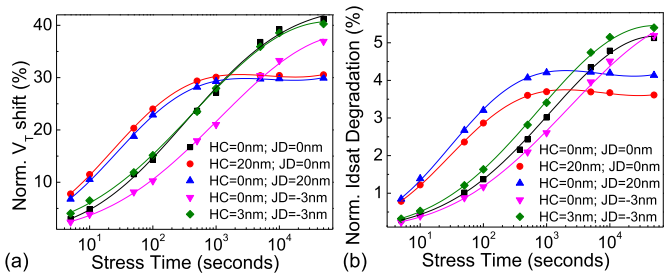

Fig. 4. HCI (a) threshold voltage (V_T) shift and (b) ON-current (I_{DSAT}) degradation with respect to stress time in linear-log scale, as a function of combinations of HC and JD.

This increases thermal resistance, which causes increased lattice heating. It is worth highlighting that, in FinFET, a majority of the heat is dissipated through the BEOL metallization, and hence, any change in the contact scheme is expected to affect the lattice heating behavior [5], [18]. Fig. 4 shows the HCI degradation in terms of the normalized threshold voltage (V_T) shift and normalized drain current (I_{DSAT}) for a range of HC and JD values. It should be noted that three cases are compared here: silicide edge aligned to S/D junction (JD$\leq$0 and HC = |-JD|); silicide region away from S/D junction (JD > 0 or HC > |-JD| for JD $\leq$ 0); and silicide edge crossing S/D junction, i.e., silicidation overlaps the N^+/P-well junction (JD<0 and HC < |-JD|). It can be observed in Fig. 4 that degradation trends, independent of HC and JD values, follow a power law dependence, which eventually saturate at longer stress times. A similar saturating trend was earlier reported in [25], where it was attributed to the progressive fall in the number of virgin Si-H bonds (n_0) and the diminishing difference between n_0 and interface trap generation (N_{IT}).

It is interesting to note that, for initial stress duration, FinFET devices with HC > 0 and/or JD > 0, which had higher ESD robustness compared to other cases, show a higher V_T and I_{DSAT} shift when compared to the standard contact silicidation and junction profile scheme (HC = 0 nm and JD = 0 nm). However, at longer stress times, respective shifts in V_T and I_{DSAT} for HC > 0 and/or JD > 0 cases were found to saturate at the lower values, unlike the conventional case of HC and/or JD = 0 nm. In general, if the silicide edge overlaps or crosses the S/D junction (HC $\leq$ |-JD| for JD $\leq$ 0), the % shift in V_T and I_{DSAT} continues to increase and eventually saturates at higher V_T and I_{DSAT} shift values. It is also worth mentioning that this saturation effect occurs earlier in devices with HC > 0 nm, than fully silicided FinFETs. Therefore, a closer assessment of these peculiar HCI degradation characteristics is required for the accurate lifetime prediction and feasibility of contact/junction engineering for the overall reliability improvement of FinFET technology.

Fig. 5(a) and (b) shows the substrate current and maximum lattice temperature for different HC and JD values. A higher substrate current for devices with HC > 0 and/or JD > 0 signifies a higher impact ionization generated carriers or higher hot carrier density compared to other cases. For the same case, lattice temperature was also found to be the highest,

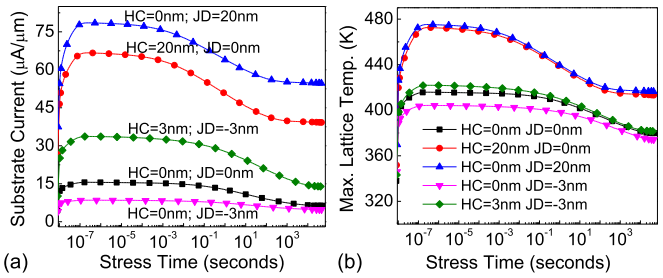

Fig. 5. (a) Normalized substrate current per unit device width (Fin pitch) and (b) maximum lattice temperature, as a function of stress time, for different contact/silicide height and relative JDs.

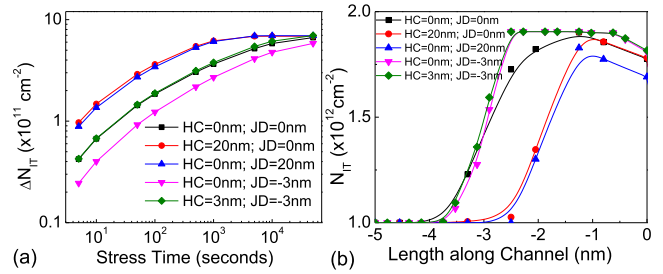

Fig. 6. (a) Change in interface trap concentration as a function of stress time, extracted at the drain-channel edge, and (b) interface trap concentration post 50 000 s stress, extracted along the channel, for different contact/silicide height and relative Junction Depths.

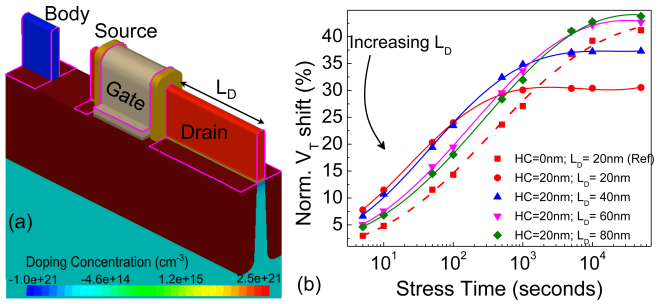

Fig. 7. (a) Fin cross section depicting drain contact length (L_D) and (b) HCI threshold voltage (V_T) shift with respect to stress time for increasing drain contact length (L_D).

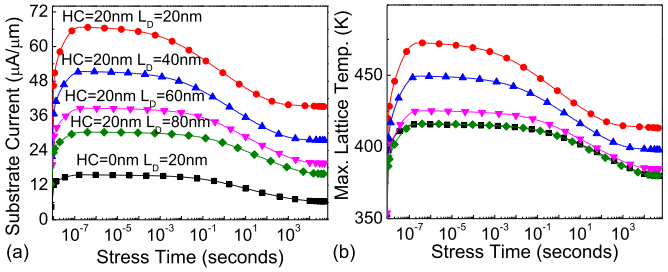

Fig. 8. (a) Substrate current per unit layout width and (b) maximum lattice temperature with respect to stress time for increasing drain contact length (L_D).

which is due to an increased thermal resistance between S/D contacts and metal interconnect. At longer stress times, increased self-heating in the device lowers the hot carrier generation by mitigating impact ionization due to increased electron-phonon scattering. On the other hand, devices having contact silicidation overlapping the S/D junction were found to have reduced substrate current, which signifies mitigated impact ionization due to increased excess carrier recombination, which results in reduced hot carrier density. The same was found to be the least when the silicide region crosses the S/D junction. On the other hand, a complete silicidation of S/D region (HC = 0 for JD= 0) lowers the thermal interface resistance, which lowers the self-heating across the device. This can result in higher interface trap generation at longer stress times. Fig. 6(a) shows the peak interface trap density (N_{IT}) in the channel, as a function of stress time for different combinations of HC and JD values. It shows that devices with HC > 0 and/or JD > 0, due to higher hot carrier density, have higher N_{IT} generation. However, as the contact silicidation gets closer to S/D junction (HC = |-JD| for JD ≤ 0), the N_{IT} generation mitigates due to reduced hot carrier density. The same was found to be the least when silicide crosses the S/D junction (HC < |-JD| for JD < 0), which is attributed to significantly increased excess carrier recombination, which suppresses hot carrier generation and hot electron density. Fig. 6(b) shows an interface trap density (N_{IT}) along the channel extracted poststress (50 000 s) for different combinations of HC and JD values. Attributed to HC- and JD-dependent E-field and hot carrier profiles, interface trap profile, poststress, along the channel also depends strongly on HC and JD values. In case of devices having HC > 0 and/or JD > 0, E-field was found to be lower compared to the other cases but has a higher hot carrier generation, which leads to faster degradation during the initial stress duration. On the other hand, at higher stress times, due to increased electron-phonon scattering attributed to higher lattice temperature, hot carriers do not travel deep into the channel. This causes hot carriers to be localized near drain-channel edge resulting in localized interface trap generation when compared to other cases. This eventually leads to faster saturation in I_{DSAT} and V_T when compared to other cases.

IV. Drain Engineering

A. Drain Contact Engineering

Fig. 7(a) shows an active Fin / channel cross section depicting drain junction length (L_D) of fully silicided FinFET. An increasing drain junction length was earlier found to improve the ESD robustness of fully silicided FETs [26]. This was attributed to mitigated filament instability with increased junction area [26]. This aspect significantly helps in improving the ESD robustness of core circuits, in which SB is not affordable. On the other hand, the implications on HCI reliability are not known yet. Fig. 7(b) shows % V_T shift with stress time. It shows that a device with higher L_D has lower % degradation, compared to devices with lower L_D, during the initial stress period. There is, however, a crossover point and % degradation saturates early in lower L_D devices, to a smaller % degradation value, when compared to devices with higher L_D. On the other hand, increasing L_D increases the % degradation at longer stress times. Fig. 8(a) shows that increasing L_D lowers the substrate current, which signifies reduced carrier energy as well as mitigated impact ionization when L_D was increased. This explains mitigated HCI degradation at lower stress times when L_D was increased. However, on the other hand, increasing L_D relaxes the self-heating across the device, as shown in Fig. 8(b). This allows

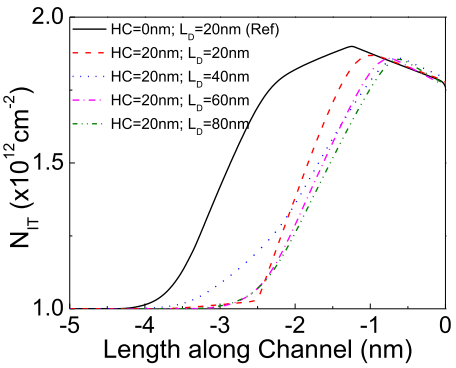

Fig. 9. Interface trap concentration profile extracted along the channel, post 50 000 s stress, as a function of drain contact length (L_D).

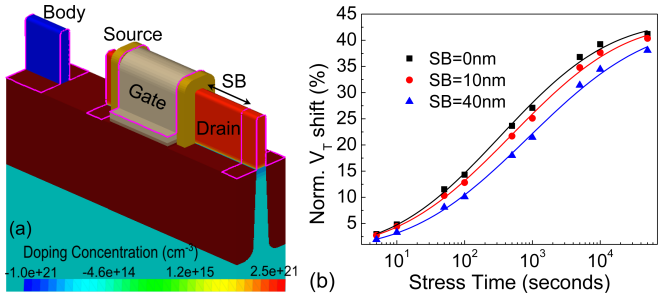

Fig. 10. (a) Fin cross section depicting silicide blocked length. (b) HCI threshold voltage shift as a function of stress time, for different SB lengths.

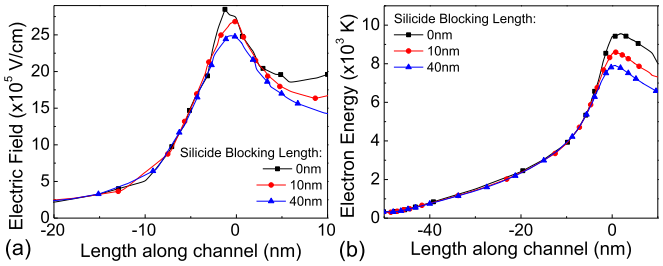

Fig. 11. (a) Electric field and (b) electron energy extracted post 50 000 s stress, for different SB lengths, along the channel.

hot carriers to travel a longer distance into the channel before they scatter with a lattice phonon. An increased hot carrier penetration into the channel extends interface trap generation deep into the channel, which is shown in Fig. 9. In the case of shorter L_D, while a higher impact ionization caused faster interface trap generation and device degradation, early self-heating localized the interface trap generation and caused % degradation to saturate at shorter stress times. On the other hand, due to extended interface trap generation deep into the channel, in case of longer L_D, the device experiences a higher % degradation which continues for an extended period.

B. Silicide Blocking

Silicide Blocking (SB), as shown as in Fig. 10(a), to improve ESD robustness of FinFETs is well known [27], which is attributed to improved parasitic bipolar efficiency with increased SB length [26]. Fig. 10(b) shows a HCI V_T shift as a function of stress time for different silicide blocked

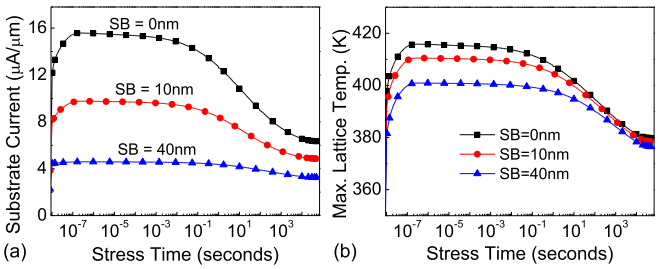

Fig. 12. (a) Substrate current per unit layout width and (b) maximum lattice temperature as a function of stress time, for different SB lengths.

TABLE I
IMPACT OF CONTACT/SILICIDE AND JUNCTION ENGINEERING PARAMETERS ON ESD RELIABILITY, HCI DEGRADATION, LATCH-UP ROBUSTNESS, AND SELF-HEATING EFFECT

Design Parameters	ESD Robustness	HCI Reliability	Self Heating	Latch-Up Robustness
Increased HC	↑	↑	↑	↓
Increased JD	↑	↑	↑	↓
Increased LD	↑	↓	↓	–
Increased SB	↑	↑	↓	–

lengths. It shows that, with increasing SB length, hot carrier degradation relaxes. For example, when SB was increased from 0 to 40 nm, a 12% reduction in percentage V_T shift was found. This is attributed to relaxed peak channel electric field with increased SB, which eventually lowers hot carrier density near the gate oxide along the channel. This is shown in Fig. 11(a) and (b), respectively. Mitigated hot carrier generation is further validated in Fig. 12(a), which shows a reduced substrate current when SB was increased. It should be noted that, as shown in Fig. 12(b) at longer stress times, no significant difference in lattice heating was found with increasing SB. This causes the exponent for % V_T shift with time to be independent of SB, as shown in Fig. 10(b). The same was, however, not the case with other contact/junction/drain engineering (HC, JD, and L_D) parameters, which was due to change in lattice heating when HC, JD, and/or L_D were changed.

V. HYBRID CONTACT AND JUNCTION ENGINEERING FOR OVERALL ROBUSTNESS

Based on the findings so far, as shown in Table I, we propose a hybrid contact and junction engineering scheme, as shown in Fig. 13, to simultaneously improve both ESD and HCI reliability of FinFET platform while minimizing self-heating and LU effects. Fig. 13 shows three unique scenarios. First, silicide edge above S/D junction with deeper junction implants (HC > 0 and JD > 0) is recommended for SCR and diode ESD protection elements. The partial contact silicidation and deeper junction profile improve diode and SCR's turn-on behavior and improved ESD robustness. Here, deeper junction implants can be realized through antipunchthrough (APT) implant, which is typically used in the baseline process for threshold voltage control. Thereby, a deeper junction implant would not add to processing complexity. It should also be

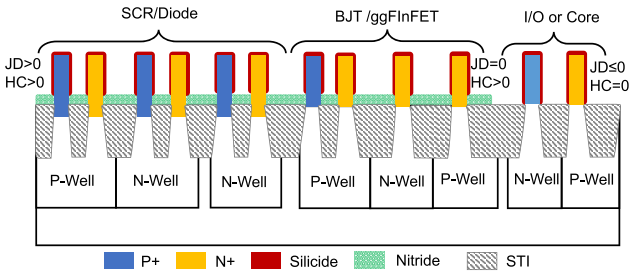

Fig. 13. Proposed hybrid contact/silicide and junction profiles, as a solution toward improved ESD robustness for protection devices while achieving reliable I/O and core devices.

noted that these devices are not affected by hot carrier effects. Next, having the same silicide edge above S/D junctions, however, without deeper junctions (HC $>$ 0 and JD $=$ 0) is proposed for bipolar junction transistor (BJT) and grounded gate FinFET (ggFinFET) devices for ESD protection. Here, partial contact silicidation improves the turn-on efficiency of the parasitic BJT. Moreover, it lowers the reverse leakage and improves ESD robustness as well as HCI immunity of ggFinFET. Finally, silicide edge aligned with S/D junction (JD$\leq$0 and HC $\geq$ |-JD|) with standard junction profiles is recommended for I/O and core FETs. This will mitigate HCI degradation and suppress the parasitic SCR to improve the LU robustness of core and I/O circuits. It should be noted that, in order to implement partial contact silicidation (HC $>$ 0), an additional processing step is to be incorporated, which is shown in Fig. 13.

VI. Conclusion

In this article, the impact of contact and junction engineering on the ESD and HCI reliability of bulk FinFET devices is explored using 3-D TCAD simulations. It was found that the ESD robustness of FinFETs can be improved by increasing salicided contact region's height (increasing HC) above the base of Fin and/or by introducing deeper junctions (increasing JD), i.e., pushing the S/D diffusion below the base of Fin. A strong influence of ESD design parameters such as HC, JD, and L_D on device's HCI reliability was discovered. In this direction, we have shown that the HCI degradation characteristics consist of a presaturation and postsaturation region, where the presaturation characteristic depends on carrier energy and impact ionization rate, i.e., higher field results in higher impact ionization and higher energy leading to faster degradation, whereas postsaturation behavior depends on lattice heating, i.e., higher field results in higher self-heating, which causes hot carriers to scatter/relax faster leading to mitigated HCI degradation. Attributed to this competing degradation trends have been observed in the presence of increased impact ionization as well as increased self-heating. While higher impact ionization would cost a faster device degradation at initial stress times, an increased self-heating leads to faster hot carrier relaxation, before it travels deeper into the channel, which causes faster saturation in degradation characteristics at longer times. Attributed to these competing aspects, HCI degradation characteristics, for devices with HC $>$ 0 and/or JD $>$ 0, show a higher V_T and I_{DSAT} shift for shorter stress duration; however, an early saturation in degradation characteristics was observed when stressed for longer duration. As a result, % degradation was found to saturate at the lower value. However, when the silicide is kept aligned to the junction, a relaxed lattice heating allowed a device to degrade for a longer duration by allowing hot carriers to penetrate deeper into the channel. Increasing drain contact length improves the ESD robustness due to relaxed peak channel electric field and mitigated lattice heating. However, due to the contribution of a longer drain junction in hot carrier generation, the HCI reliability of these devices was found to affect adversely. Furthermore, increased SB length improves the ESD robustness due to relaxed field and mitigated lattice heating, which also leads to lower hot carrier generation and improved HCI reliability. Keeping in mind the findings in this article and HCI/ESD reliability trends explored, a hybrid technology with a mixture of contact silicidation/junction profile engineering is proposed to maximize ESD/LU robustness while improving overall HCI reliability of bulk FinFET technology platform, without compromising with FinFET's performance.

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