Novel Drain-Connected Field Plate GaN HEMT Designs for Improved $V_{BD} - R_{ON}$ Tradeoff and RF PA Performance

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***Abstract*— TCAD studies are performed to develop physical insights into the breakdown behavior of drain-connected field plate-based GaN HEMTs. Using the developed insights, to mitigate the performance bottleneck caused by the lateral drain-connected field plate design, we have proposed novel vertical-field-plate designs. The proposed designs alleviate the channel electric field by uniformly distributing it vertically into the GaN buffer region. As a result, the proposed vertical and dual-field-plate design offer 2× and 3× improvements in breakdown voltage, respectively, compared with the design without field plate. Similarly, compared with a design with a lateral field plate, a 50% improvement in the breakdown voltage was seen with dual-field-plate architecture. RF power amplifier (PA) performance extracted using load-pull simulations demonstrates an improved RF PA linearity at higher drain bias, improved output power, efficiency, and PA gain for HEMTs with dual- and vertical-field-plate designs.**

***Index Terms*— AlGaN/GaN HEMT, field plate design, GaN TCAD modeling, vertical field plate.**

I. Introduction

FIELD plate technology is the most widely adopted technique for increasing the breakdown voltage in HEMT. The field plates result in the uniform space-charge distribution in the lateral direction and, thereby, improve the breakdown voltage of the device. There are several variations of the same reported in the literature, such as gate field plate [1]–[6], source-connected field plate [7]–[11], and drain-connected field plate [11]–[16]. The recently developed trigate [17], [18] and tridrain [19] designs have shown high breakdown voltage by shaping the field profile at the contacts. However, these literature reports used the lateral- or gate-connected field plate configuration, which adds to the Miller capacitance. Furthermore, in order to achieve improved RF performance, it is also imperative to scale down the device without compromising the breakdown voltage. Gate-connected field plate, in fact, limits the lateral scaling [4], [20], [21] to enhance the ON-state performance [6], [22]. In addition, as the device scales down, the contribution of the field-plate-induced parasitic Miller capacitance begins to dominate, resulting in the degradation in RF performance parameters, such as power gain and cutoff frequency. In this scenario, the drain-connected field plate devices can provide better breakdown voltage-RF performance tradeoff, maximizing Johnson's figure of merit (FOM).

In this article, we have, thereby, focused our discussions on drain-connected field plate architectures and have proposed new field plate architecture. Moreover, to access the feasibility of the proposed field plate concept, for large-signal applications, such as power amplifier (PA), we have also carried out extensive large- and small-signal analyses of the proposed designs and have compared its performance with the conventional architectures. This article is arranged as follows. Section II presents a computational modeling approach used in this article. Section III discusses the lateral- and vertical-field-plate designs and provides physical insight into each design type. Section IV presents the novel dual-field architecture in detail. This is followed by Section V, which presents the design guidelines. Section VI provides comparative analyses of RF performance figures of merit and RF PA performance. Section VII finally concludes this article.

II. Computational Framework

A well-calibrated Technology CAD setup, as described and used in our earlier works [23]–[25], has been used here. Breakdown simulations were performed with critical electric field values for GaN set to 3×10^6 Vcm^{-1} while considering the Chenoweth law for impact ionization [26]. For accurate modeling, polarization-induced charge is considered at all the heterointerfaces. Electron mobility, contact resistance, surface trap charges, and so on were calibrated with experimental data, which has been elaborated in our earlier work [23]. The carbon-doped HEMT stack used for TCAD simulations is adapted from [27]. The HEMT structures studied here are shown in Fig. 1. A conventional HEMT design without any field plate is depicted in Fig. 1(a). Drain-connected lateral- and vertical-field-plate architectures are shown in Fig. 1(b) and (c), respectively. Fig. 1(d) discloses the proposed dual-field-plate design, employing both vertical and lateral field plates. For all the simulations, the gate-to-source distance (L_{sg}) = 1 μm, SiN passivation thickness = 50 nm, gate length (L_g) = 0.7 μm, and buffer thickness (t_{Buffer}) = 3 μm are used unless specified otherwise.

Manuscript received January 24, 2020; revised February 18, 2020; accepted February 19, 2020. Date of publication March 12, 2020; date of current version March 24, 2020. This work was supported by the Department of Science and Technology (DST), Government of India, under Grant DST/TSG/AMT/2015/294. The review of this article was arranged by Editor G. Verzellesi. *(Corresponding author: Ankit Soni.)*

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Digital Object Identifier 10.1109/TED.2020.2976636

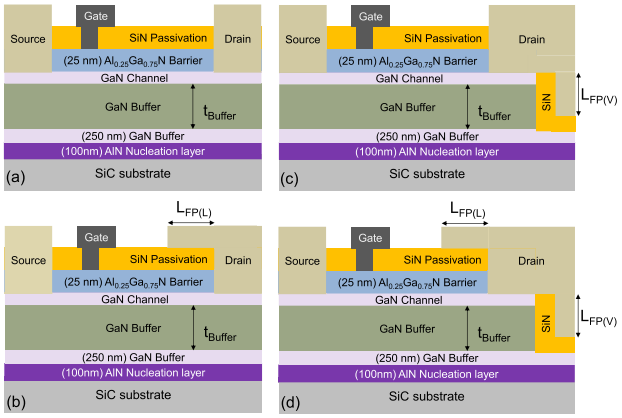

Fig. 1. Cross-sectional illustration of the simulated structures used in this article. (a) Cconventional design without field plate (no FP). (b) Drain-connected lateral field plate (lateral FP). (c) Drain-connected vertical field plate (vertical FP). (d) dual-field-plate design (dual FP).

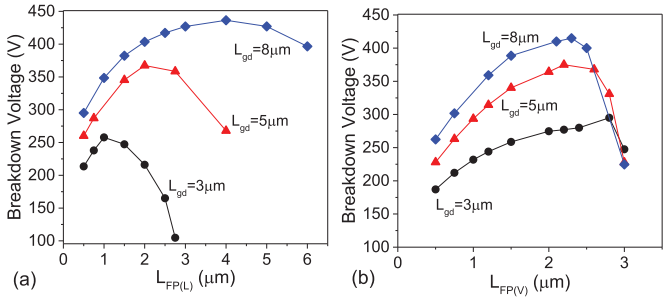

Fig. 2. Variation of breakdown voltage as a function of field plate length and L_{gd} for (a) lateral-field-plate design and (b) vertical-field-plate design.

I–V and C–V family of curves extracted using TCAD are used to extract HEMT model card using Keysight's IC-CAP device modeling suit and Advanced Spice Model for High Electron Mobility Transistor (ASMHEMT) model card [28]. Besides, the S-parameters extracted using model card were also matched with TCAD extracted S-parameters. Post-dc, C–V, and S-parameter matching, load-pull simulations were carried out using Keysight's Advanced Design System (ADS) for PAs biased in class-AB.

III. Drain-Connected Field Plates: Design and Physical Insights

A. Lateral-Field-Plate Design and Limitations

The drain-connected lateral field plate [11]–[16] relaxes the peak field at the drain contact, which, in turn, improves the breakdown voltage. Fig. 2 shows the breakdown voltage as a function of lateral-field-plate length for the various gate-to-drain distances (L_{gd}). A clear roll-off in the breakdown voltage can be seen when the field plate length was increased, which is severe for shorter L_{gd} values. This effect is mitigated as the drift region length is increased. Fig. 3(a)–(c) shows that with the increase in the field plate length, the peak electric field peak shifts away from the drain contact and moves toward the gate. Improvement in the breakdown voltage with an increase in field plate length, as shown in Fig. 2(a), is attributed to the relaxation of peak field and the resultant decrease in impact ionization rate, as shown in Fig. 3(d). However, as the field plate moves closer to the gate, the peak electric field at the gate edge increases significantly. The impact ionization rate for $L_{FP} = 1.5\ \mu$m is significantly higher near the gate compared with the other two cases. The high impact ionization rates lead to enhanced carrier generation at the gate, leading to an early breakdown of the device. This is a critical issue, as the lateral-field-plate designs do not yield any breakdown voltage improvement beyond certain field plate length. Hence, the maximum breakdown voltage is limited by L_{gd}.

B. Vertical Field Plate

On the other hand, in the case of vertical-field-plate design, the breakdown voltage increases consistently as a function of field plate lengths, as shown in Fig. 2(b). Fig. 3(e)–(g) shows that the vertical field plate acts as a parallel-plate capacitor in conjunction with the buffer. With the application of positive drain bias, it depletes the localized region situated in the deep buffer. This additional space-charge region provides additional voltage blocking capability to the device by redistributing the electric field vertically into the buffer and not toward the gate. The impact ionization originates away from the channel and, hence, delays the avalanche breakdown process. Fig. 2(b) shows a fall in the breakdown voltage beyond a certain field plate depth. It is attributed to high electric field crowding across the etched buffer and substrate and resultant increase in impact ionization, as shown in Fig. 3(g) and (h), respectively. It should be noted that the vertical field plate is as effective as the lateral field plate and not limited by the drift region length, however, defined by the buffer thickness.

IV. Proposed Dual-Field Plate

The ability of vertical field plate to distribute electric field away from the channel, used in conjunction with the lateral field plate, can provide a significant boost in breakdown performance of the device. Fig. 1(d) shows a dual-field-plate architecture deploying both lateral and vertical field plates. Fig. 4 shows that the dual-field-plate design greatly suppresses the electric field at the drain edge by shifting the peak E-field away from the drain contact in both lateral as well as vertical directions. The E-field relaxation increases the design margin by pushing the breakdown limit to a higher voltage. Fig. 5 compares the breakdown voltage of all the designs explored in this article. The lateral- and vertical-field-plate lengths are optimized for the maximum breakdown voltage for fixed L_{gd} (=3 μm). With the introduction of lateral and vertical field plates, the breakdown voltage is improved by $\sim$1.8$\times$ and $\sim$2$\times$, respectively, compared with the conventional design. The dual-field-plate design, however, results in highest breakdown voltage, that is, $\sim$3$\times$ higher compared with conventional HEMT architecture without field plate. Besides, it also results in 6$\times$ reduction in source-to-drain leakage compared with lateral-field-plate architecture.

V. Design Guidelines

A. Impact of Buffer and Drift Region Scaling on Field Plate Design

The impact of device scaling on the field plate design for each case is studied to obtain an optimum design window for maximizing the breakdown voltage. In the case

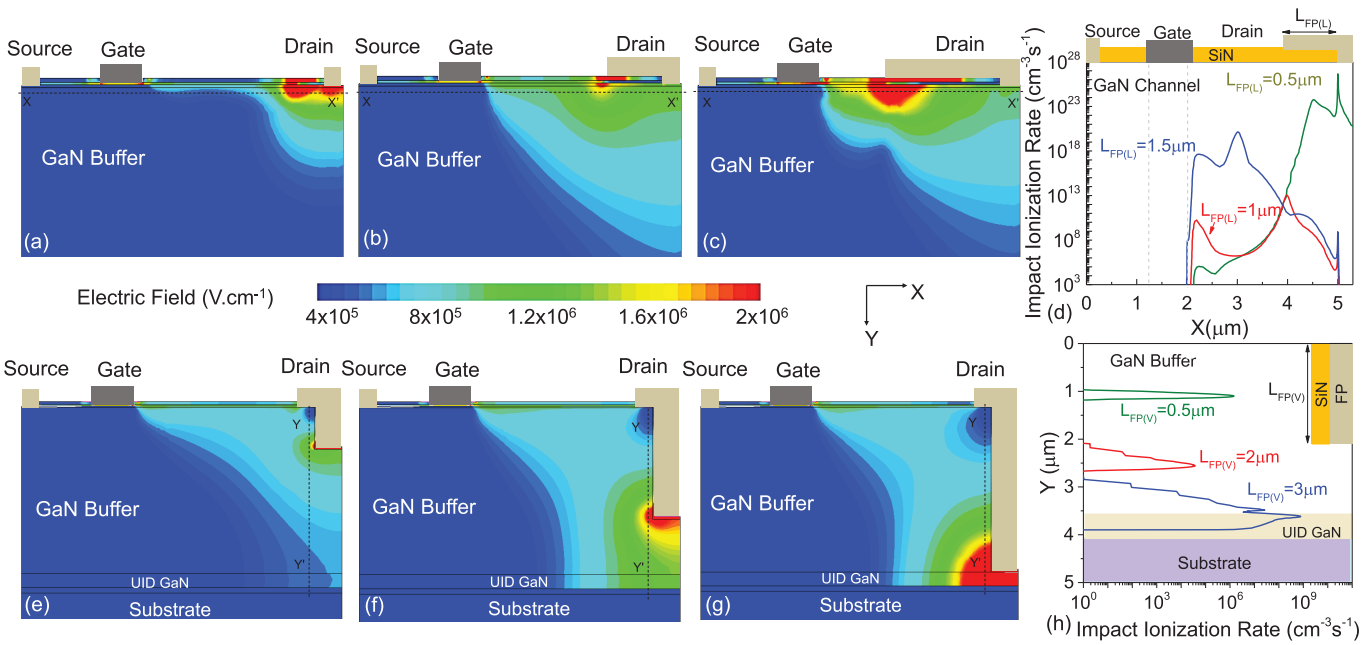

Fig. 3. Electric field contours extracted for the lateral-field-plate design with field plate length (a) $L_{FP(L)} = 0.5\ \mu$m, (b) $L_{FP(L)} = 1\ \mu$m, and (c) $L_{FP(L)} = 1.5\ \mu$m; for vertical-field-plate design and (e) $L_{FP(V)} = 0.5\ \mu$m, (f) $L_{FP(V)} = 2\ \mu$m, and (g) $L_{FP(V)} = 3\ \mu$m. The impact ionization rates as a function of field plate lengths are represented in (d) and (h) for lateral (cut along X–X') and vertical field plates (cut along Y–Y'), respectively. Here, L_{gd} is 3 μm and $t_{Buffer} = 3\ \mu$m. Drain voltage is 200 V, applied in the channel OFF-state.

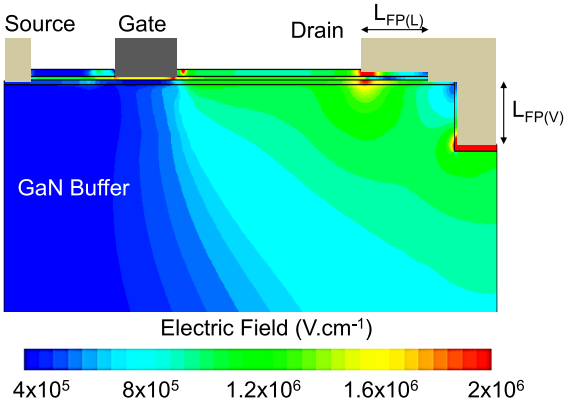

Fig. 4. Electric field distribution in dual-field-plate structure. Here, drain voltage is 200 V, applied in channel OFF-state; $L_{FP(L)} = 1\ \mu$m and $L_{FP(V)} = 0.5\ \mu$m.

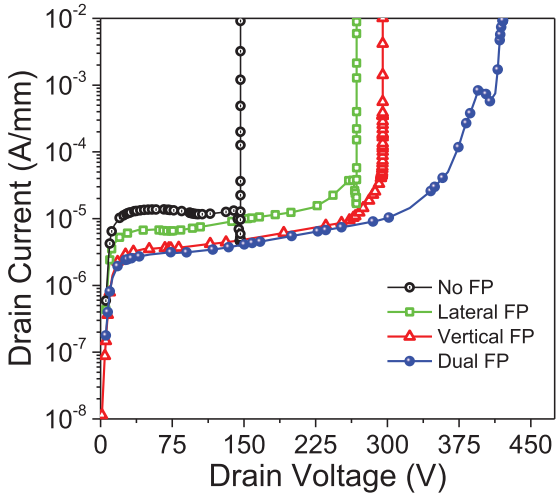

Fig. 5. Simulated OFF-state breakdown voltage characteristics for conventional, lateral, vertical, and dual-field-plate designs. The simulations are performed at $V_{gs} = -6$ V for buffer width $t_{Buffer} = 3\ \mu$m and $L_{gd} = 3\ \mu$m for all the devices.

of lateral-field-plate design and for moderate gate-to-drain lengths ($L_{gd} = 5\ \mu$m), the breakdown voltage is found to be a weak function of buffer thickness, as shown in Fig. 6(a). The breakdown voltage improvement with field plate length is limited by impact ionization at the gate edge above a certain field plate length, which, apparently, is a function of buffer thickness. For instance, a thin buffer ($t_{Buffer} = 1.5\ \mu$m) has a slower breakdown voltage roll-off at higher field plate lengths compared with the thicker buffer ($t_{Buffer} = 3\ \mu$m). This is attributed to relative impact ionization at the drain and gate sides in both cases. In the case of thin buffers, the electric field at the drain contact is significantly high compared with that of a thick buffer. It leads to a reduction in the electric field peak at the gate edge. This ensures that the fall in breakdown voltage with field plate length is not as abrupt as it is observed in the case of larger buffer thickness. The lateral field plate proves to be far less effective in maximizing the breakdown performance for scaled devices. As shown in Fig. 6(b), for the entire range of buffer thickness, the breakdown voltage roll-off is encountered much earlier. In addition, the breakdown voltage becomes virtually independent of the buffer thickness, as the lateral breakdown dominates due to the shorter gate-to-drain distance.

On the other hand, there is a substantial scaling of breakdown voltage as a function of buffer thickness in the case of vertical-field-plate designs for both unscaled [see Fig. 6(c)]

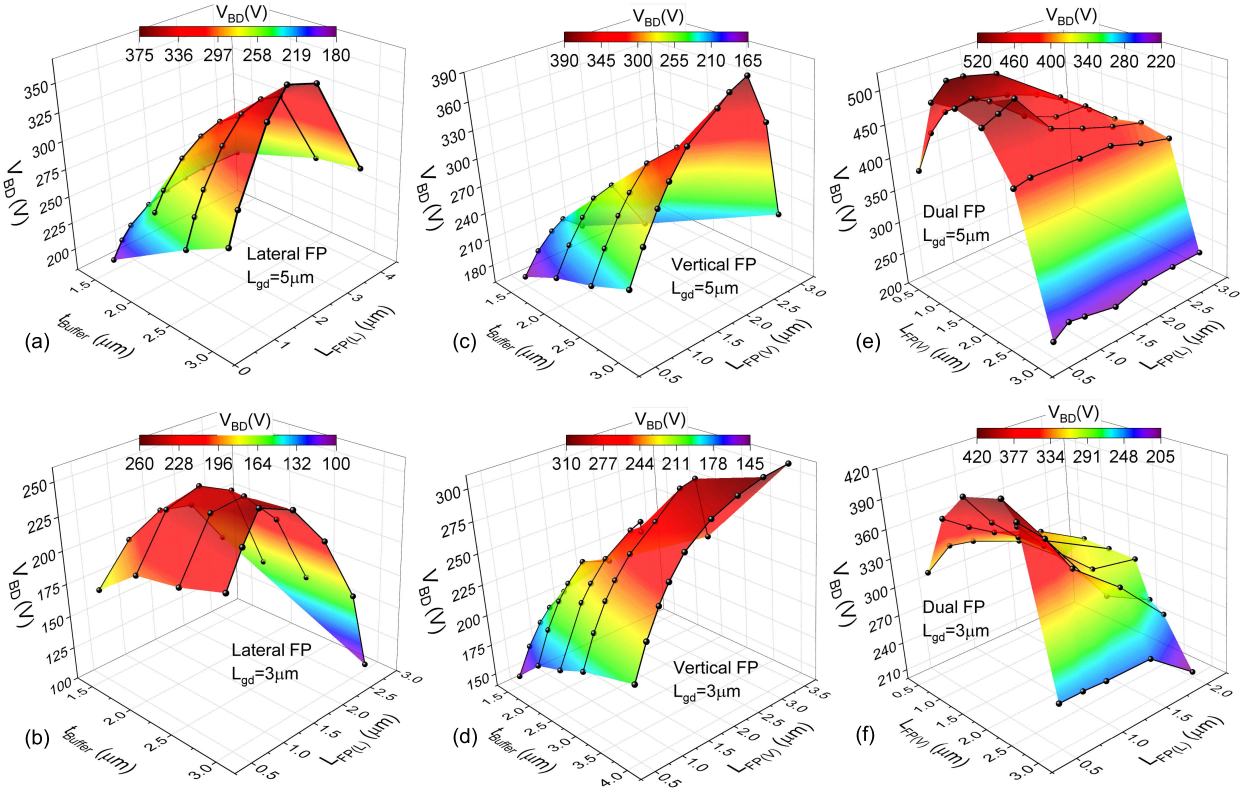

Fig. 6. Impact of buffer thickness and field plate lengths on breakdown voltage for (a) lateral-field-plate design ($L_{gd} = 5\ \mu$m), (b) lateral-field-plate design ($L_{gd} = 3\ \mu$m), (c) vertical-field-plate design ($L_{gd} = 5\ \mu$m), and (d) vertical-field-plate design ($L_{gd} = 3\ \mu$m). Dependence of the breakdown voltage on lateral- and vertical-field-plate lengths for dual-field-plate design with (e) $L_{gd} = 5\ \mu$m and (f) $L_{gd} = 3\ \mu$m.

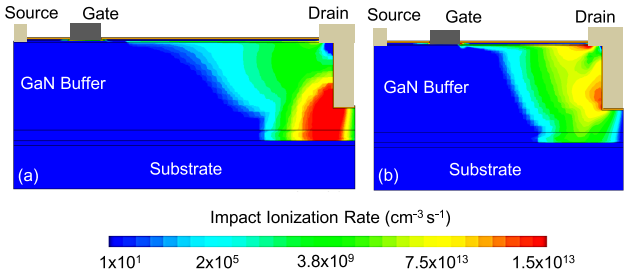

Fig. 7. Impact ionization rate contours in the case of vertical-field-plate structure for (a) $L_{gd} = 5\ \mu$m and (b) $L_{gd} = 3\ \mu$m.

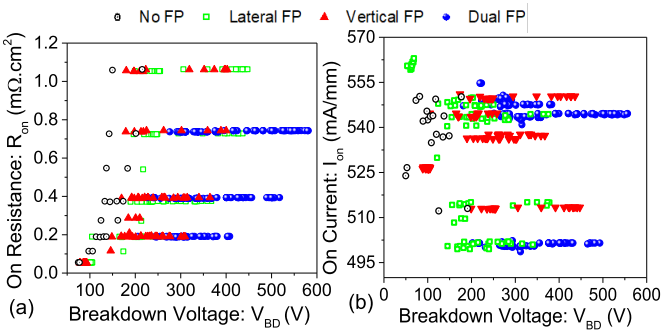

Fig. 8. (a) ON-resistance (R_{ON})—breakdown voltage (V_{BD}) tradeoff and (b) ON-current (I_{ON})—breakdown voltage (V_{BD}) tradeoff for no-field plate, lateral, vertical, and dual-field-plate architectures. For the design of experiments (DOE), following parameters were varied, i.e., L_{gd} (1–8 μm), t_{Buffer} (1.5–3 μm), and corresponding field plate lengths/depths.

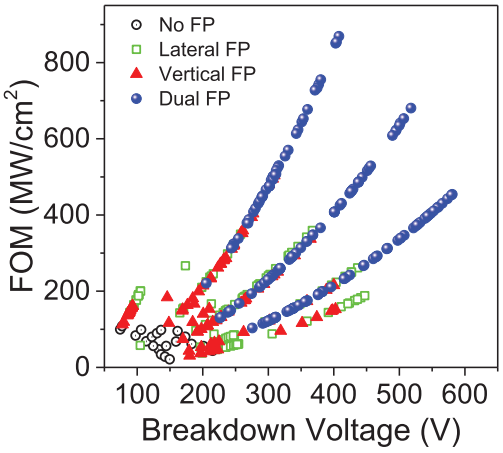

Fig. 9. Comparative power FOM for various designs. The dual-field-plate design offers highest FOM along with high breakdown voltages. For DOEs, following parameters were varied, i.e., L_{gd} (1–8 μm), t_{Buffer} (1.5–3 μm), and corresponding field plate lengths/depths.

and scaled devices [see Fig. 6(d)]. This is attributed to the electric field relaxation in the vertical direction into the buffer, which was missing in the lateral-field-plate structure. The breakdown voltage is no longer limited by the L_{gd}, which was the key reason for the ineffectiveness of the lateral field plate in scaled devices. For larger gate-to-drain distances ($L_{gd} = 5\ \mu$m), a breakdown voltage roll-off is observed in vertical-field-plate design too when field plate depth was increased. This is due to the increased localization of the electric field deep into the GaN buffer. Interestingly, as shown in Fig. 6(d), for the scaled device ($L_{gd} = 3\ \mu$m), breakdown voltage consistently improves with field plate depth, and the

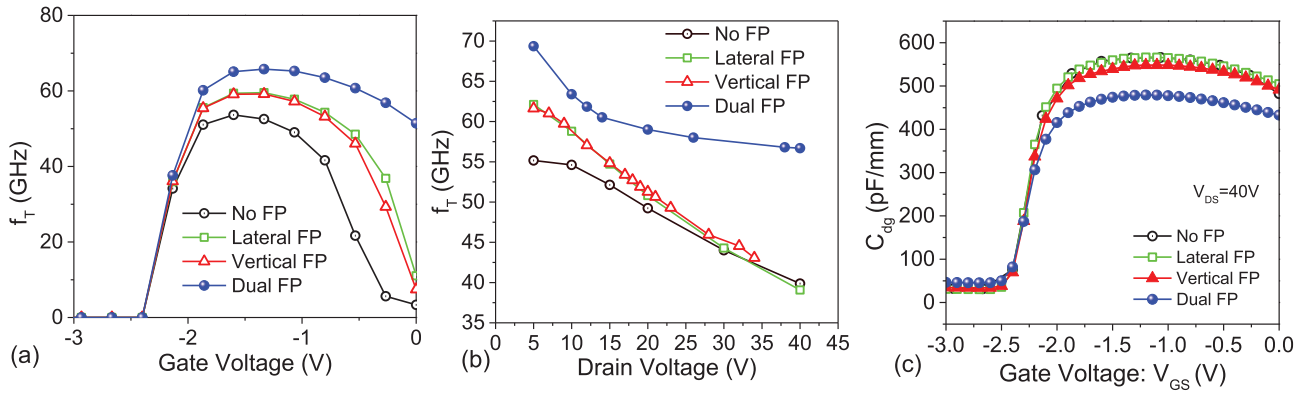

Fig. 10. (a) Cutoff frequency (f_T) as a function of gate bias, (b) maximum cutoff frequency roll-off with respect to the drain voltage, and (c) Miller capacitance (C_{dg}) as a function of gate bias. Plots are extracted for $L_{sg} = 0.3$ μm, $L_g = 0.1$ μm, and L_{gd}, and field plate lengths are optimized for each design in order to achieve breakdown voltage of 150 V while maximizing the ON-state performance.

TABLE I
RF HEMT DIMENSIONS FOR $V_{BD} = 150$ V

HEMT Designs	L_{sg} (μm)	L_g (μm)	L_{gd} (μm)	$L_{FP(L)}$ (μm)	$L_{FP(V)}$ (μm)
No FP	0.3	0.1	3	0	0
Lateral FP	0.3	0.1	2	0.6	0
Vertical FP	0.3	0.1	2	0	0.5
Dual FP	0.3	0.1	1	0.6	1

roll-off in breakdown voltage is found when the field plate length approaches the total buffer thickness. This is explained in Fig. 7. Fig. 7(a) shows that for longer drift lengths, the field is localized around the field plate deep into the buffer, whereas, as shown in Fig. 7(b), as the drift length is scaled, the electric field is shared between the drain field plate and gate edge. The field distribution across the gate and drain sides of the drift region further boosts the breakdown voltage, which is the key advantage of vertical-field-plate design for scaled devices.

In the case of dual-field-plate design, as shown in Fig. 6(e) and (f), the breakdown voltage roll-off with both lateral-field-plate length and vertical field depth is seen. Optimization of field plate lengths is carried out using simulations for the dual-field-plate design. These are the function of trends seen earlier in individual cases. The effect of the lateral field plate becomes weak as the vertical field plate extends deep into the buffer as the hotspot shifts away from the channel. Hence, within the design window, individual field plate lengths are optimized to give maximum breakdown voltage. Attributed to this, an optimum window for scaled devices can be seen for moderate length and depth of the lateral and vertical components of the field plate, respectively. The maximum breakdown voltage obtained in the case of $L_{gd} = 3$ μm shows 1.6× and 1.35 × improvements compared with lateral- and vertical-field-plate designs, respectively. A similar improvement is also observed for longer drift region devices ($L_{gd} = 5$ μm).

B. Power FOM

Fig. 8 shows the ON-resistance (R_{ON}) and breakdown voltage (V_{BD}) tradeoff for the three field plate designs. Fig. 8(a) shows that the dual-field-plate design offers highest breakdown voltage for a given R_{ON}. This attribute enables device

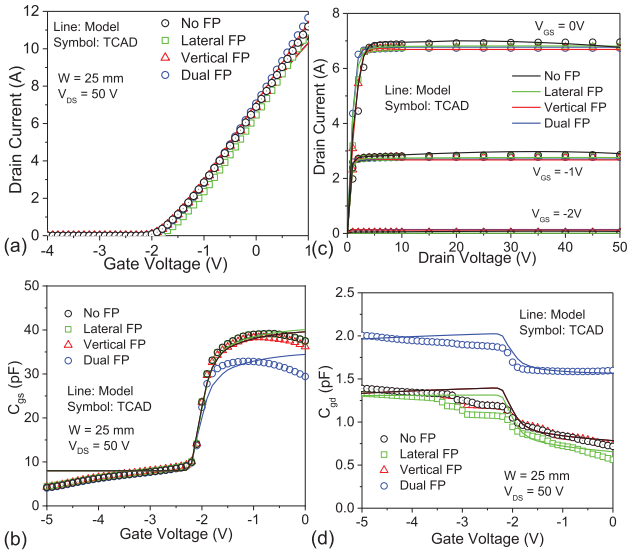

Fig. 11. TCAD and model data plotted together depicting a good match between TCAD and model. (a) Transfer characteristics, (b) output characteristics, (c) gate–source capacitance (C_{gs}), and (d) gate–drain capacitance (C_{gd}). TCAD data are represented by symbols, whereas the model data are represented by lines. Plots are extracted for $L_{sg} = 0.3$ μm, $L_g = 0.1$ μm, and L_{gd}, and field plate lengths are optimized for each design in order to achieve breakdown voltage of 150 V while maximizing the ON-state performance.

scaling without compromising the breakdown voltage. Similarly, Fig. 8(b) shows that the dual-field-plate design offers the highest breakdown voltage for a given ON-current (I_{ON}) through the device. We have also compared the power FOM for the three designs, which is given as $\frac{V_{BD}^2}{R_{ON}}$, as shown in Fig. 9. For a given buffer thickness and gate-to-drain spacing, dual-field plate offers the highest FOM compared with other designs. These trends validate the superiority of dual- and vertical-field-plate designs over the lateral-field-plate design.

VI. RF FOM

In the previous section, we looked into the proposed field plate device's FOM from the power switching applications' point of view. For RF applications, it is imperative to study the small signal as well as the large-signal performance of proposed designs. To address this, individual devices were

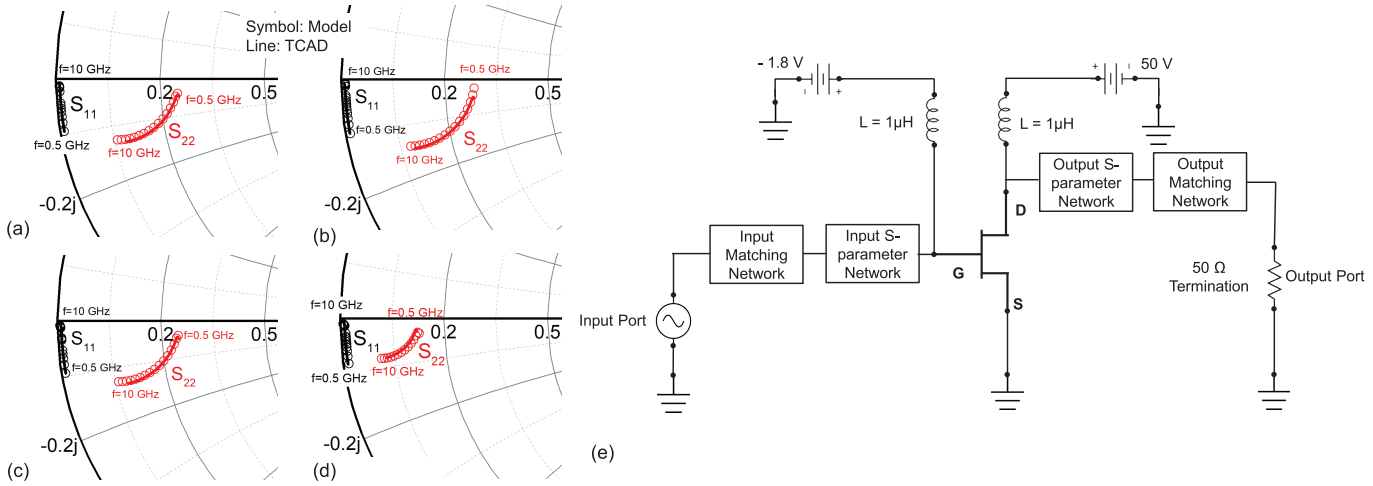

Fig. 12. S_{11} and S_{22} extracted using TCAD and model, plotted together depicting a good match between TCAD and model. (a) No-field plate, (b) lateral field plate, (c) vertical field plate, and (d) dual-field-plate design. (e) Load-pull setup consisting RF PA biased in the class-AB operation. S-parameter is extracted for the frequency range from 0.5 to 10 GHz. For RF PA/load-pull simulations and S-parameter extraction using model, Keysight's ADS suit was used.

optimized for a breakdown voltage of 150 V while maximizing the ON-state performance. The corresponding device dimensions are given in Table I. RF FOM parameters are extracted for the optimized designs and are discussed as follows.

A. Small-Signal (Intrinsic) Performance

Transistor's unity gain frequency or cutoff frequency (f_T), which is a measure of small-signal performance and is strong function of device parasitics, is given as follows [29]: $(1/2\pi f_T) = (C_{\rm gs} + C_{\rm gd}/g_m) + C_{\rm gd}.(R_s + R_d).[1 + (1 + (C_{\rm gs}/C_{\rm gd}))(g_d/g_m)]$, where $C_{\rm gs}$ and $C_{\rm gd}$ are the gate-to-source and gate-to-drain capacitances, respectively, g_m is the transconductance, g_d is the output conductance, and R_s and R_d are the source and drain resistances, respectively. Fig. 10 (a) and (b) shows dual-field-plate device to have the highest f_T, as well as superior linearity as a function of the gate and drain bias, respectively. Here, superior linearity is represented by mitigated f_T roll-off as a function of the gate and drain sweep, respectively. Fig. 10(c) shows the Miller capacitance as a function of gate voltage. Lateral- and vertical-field-plate devices have higher Miller capacitance compared with the dual-field-plate device. This is attributed to shorter field plate length required for a given breakdown voltage in the case of dual-field-plate design compared with the lateral- and vertical-field-plate designs. Hence, the Miller capacitance contribution of the field plate is significantly reduced in the dual-field-plate design, leading to improved linearity and RF performance.

B. Large-Signal (RF PA) Performance

For RF PA analysis of the proposed and conventional field plate designs, I–V and C–V data of optimum devices are used to develop HEMT model parameters using the Keysight's IC-CAP device modeling suit and the ASMHEMT model [28]. The optimization was elaborated earlier, where ON-state performance was maximized while keeping breakdown voltage fixed to 150 V. Fig. 11 shows a good match between TCAD and model data for all optimized devices. Furthermore, the S-parameters extracted using model cards were also matched with TCAD extracted S-parameters. A good match between S-parameters extracted using TCAD and model, for all the four configurations studied, is evident in Fig. 12(a)–(d). Post-dc, C–V, and S-parameter matching, load-pull simulations were carried out using Keysight's ADS for the class-AB operation of PA, as shown in Fig. 12(e). For the PA design, a transistor width of 25 mm is used in simulations.

For RF PA analysis, load-pull simulations are performed by tuning the input and output matching networks, such that the maximum power is delivered to the load. The output power versus operation frequency for HEMTs having different field plate configurations is shown in Fig. 13(a). Gain and drain efficiency are compared in Fig. 13(b) and (c), respectively. The lateral-field-plate device shows a significant reduction in output power, gain, and drain efficiency compared with the device without the field plate. This is attributed to very high drain capacitance in the case of the lateral-field-plate device, which is otherwise missing in the no-field plate case. This is a bottleneck in employing lateral-field-plate devices at high frequencies. However, in the case of the vertical-field-plate design, the field plate is implemented normal to the channel. The device with a vertical field plate shows higher output power at lower frequencies. At higher frequencies, no difference between the case with vertical field plate and no-field plate can be seen. As far as gain and drain efficiency with respect to frequency are concerned, no noticeable difference between the case with vertical field plate and no-field plate can be seen. In this case, as the field plate is perpendicular to the channel, the field plate to channel capacitance component is mitigated. Hence, the large-signal FOM parameters closely match with the no-field plate case. On the other hand, the dual-field-plate design is clearly found to be superior in all aspects of RF PA performance. It offers higher output power and gain compared with other designs. Despite the fact that the

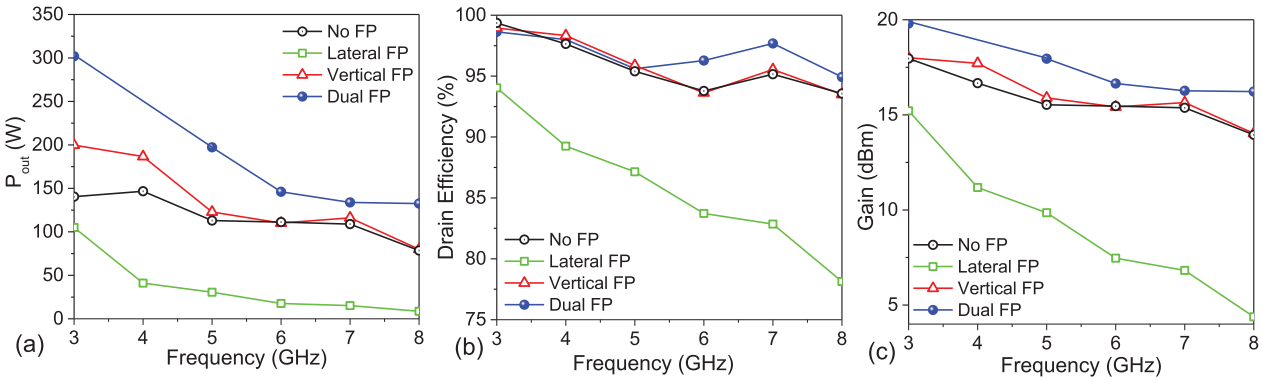

Fig. 13. (a) Output power extracted at fixed input power of 35 dBm for different field plate designs. (b) Drain Efficiency and (c) gain for frequency range from 3 to 8 GHz.

dual-field-plate design contains lateral field-plate to channel capacitance component, substantially improved characteristics are attributed to its highly scaled nature compared with other designs for a given breakdown voltage. The ability to scale translates to higher ON-current, which, in turn, results in higher output power, gain, and efficiency. It is also worth highlighting that output power, drain efficiency, and gain roll-off with frequency were the least in dual-field-plate HEMT compared with other designs. This is attributed to the highly linear Miller capacitance behavior of the dual-field plate.

VII. Conclusion

In this article, physical insights into the breakdown behavior of drain-connected field plate-based GaN HEMTs are developed using detailed TCAD simulations. In the case of lateral-field-plate design, a significant breakdown voltage roll-off with field plate length was found. This is due to the peak electric field shift from drain edge to gate edge with an increase in peak electric field post localization near the gate edge. This issue was found to be mitigated in the drain-connected vertical field plate. The vertical field plate spreads the space charge across the GaN buffer, which, in turn, distributes the electric field deep into the GaN buffer, leading to improved breakdown voltage for fixed drift length. However, in vertical-field-plate design breakdown voltage becomes limited by buffer thickness, which leads to breakdown voltage roll-off for higher field plate depth. In both cases, the breakdown voltage was found to reduce when drift length or gate-to-drain distance was reduced. Besides, a uniform sharing of the electric field between the gate and drain edge (i.e., across the drift region) was missing in these two designs. This was addressed by the proposed dual-field-plate design, which allows the electric field to be shared across the gate and drain edges, particularly for scaled design in an optimum design window. This allowed HEMT scaling while using dual-field-plate design to boost ON-state performance without compromising with breakdown performance. Physical insights and design guidelines to derive the optimum design window are also presented in this article. As a result, the proposed dual-field-plate design shows significantly improved V_{BD}–R_{ON} Tradeoff, small-signal RF performance, and RF PA performance for a wide range of frequencies.

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