Adaptive Dielectric Thin Film Transistors-A Self-Configuring Device for Low Power Electrostatic Discharge Protection

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***Abstract*— Large area and flexible electronic systems are widely used in applications such as displays, image sensors, wearable electronics and energy harvesting systems. A key element in many of these systems is the electrostatic discharge protection circuit. The conventional protection circuit uses large aspect-ratio diode connected thin film transistors that offer a low resistance path to the surge current but also does the same to signals during normal system operation resulting in power loss. Here we describe as well as demonstrate the feasibility of a novel idea for electrostatic discharge protection involving an adaptive dielectric thin film transistor that self-configures itself to a low resistance state during an electrostatic discharge event and a high resistance state during normal operation without external control. This results in 1000-10000 times the power savings compared to diode connected TFTs.**

***Index Terms*— Thin film transistors, electrostatic discharge, thin film circuits.**

I. Introduction

THIN film transistor (TFT) based large area and flexible electronic systems require electrostatic discharge (ESD) protection [1]–[4]. An ESD event is a rapid transfer of finite charge between two systems resulting in a current surge that could damage the core circuit [5]. The charge source could be viewed as being located at the peripheral contact pad and an ESD protection circuit is placed at this location to shunt the surge current and protect the core circuit (Fig. 1(a)).

The conventional ESD protection circuit uses two, large-aspect ratio, diode connected TFTs in anti-parallel configuration [6]–[12]. This circuit offers a low resistance path to the surge current but also does the same to signals during normal system operation resulting in power loss [10], [11]. Additional circuits are required to keep the protection circuit turned off during normal operation [10], [13]–[16].

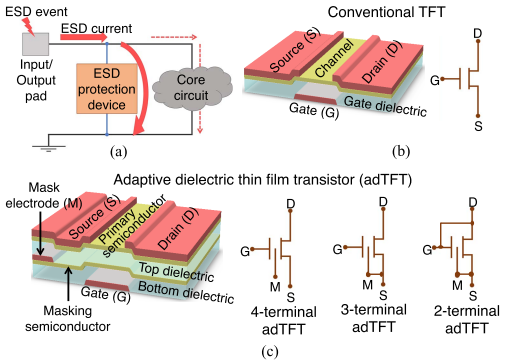

Fig. 1. (a) ESD protection. (b) Conventional TFT. (c) Adaptive dielectric TFT (adTFT).

In this work we discuss the feasibility of using a new device architecture called the 'adaptive dielectric thin film transistor (adTFT)' for ESD protection. The adTFT self-configures itself to a low resistance state during an ESD event and a high resistance state during normal operation without external control resulting in power savings by a factor of $10^3 - 10^4$ compared to the conventional diode connected TFT while showing similar ESD robustness. The adTFT therefore condenses into a single device all the circuit complexity required to achieve this performance thereby saving routing complexity and layout area.

II. Design and Operation of the adTFT

The device architecture and circuit symbol of the conventional TFT and adTFT are shown in Fig. 1(b) and Fig. 1(c), respectively. Like a conventional TFT, the adTFT has a gate (G), source (S) and drain (D) electrode with a source/drain-gate overlap. The semiconductor between source and drain, henceforth called the 'primary semiconductor' for clarity, conducts the adTFT drain-source current. However, unlike the conventional TFT, the adTFT has a composite dielectric with a thin semiconductor film sandwiched between two insulating films resulting in an insulator-semiconductor-insulator stack. This sandwiched semiconducting film, referred to as the 'masking semiconductor', is connected to a reservoir of charge via the 'mask electrode (M)'. Due to an underlap between the mask electrode and gate, channel formation in

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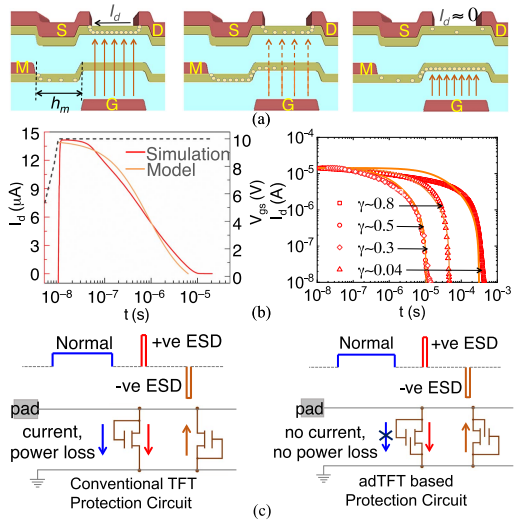

Fig. 2. (a) Operation of the adTFT. (b) Model versus simulation. For models, $k \approx 2 \times 10^{-19}$ A.cm^3/V^2, $\lambda \approx 5.97 \times 10^5$ (Vs)$^{-1}$. (c) ESD protection circuit with conventional TFTs and adTFTs. During normal operation, the adTFT based protection circuit does not consume power.

the primary semiconductor is faster than in the masking semiconductor. Two 2-terminal adTFTs (diode connected configuration) are used anti-parallelly to construct an ESD protection circuit.

The operation of the 3-terminal adTFT is best described by considering a step input in the gate-source voltage, V_{gs}. Fig. 2(a) illustrates the expected device behavior. As V_{gs} increases, carriers injected from the source result in channel formation in the primary semiconductor and a significant I_d. The masking electrode also responds to the increase in V_{gs} by injecting carriers into the masking semiconductor. Due to the gate-source overlap and the gate-mask underlap of length h_m, the former process is faster. However with enough time, a channel eventually forms in the masking semiconductor and shields the primary semiconductor from the gate field resulting in a decrease in I_d to leakage levels.

The dynamics of I_d can be modeled by treating the masking semiconductor as a zone of trapped charge that influences the threshold voltage, V_T. The mask current that charges the masking semiconductor is space charge limited [17]. The dynamic response of V_T to the step input in V_{gs} in the time interval $0 < t \leq (V_{T0}^{-1} - V_{gs}^{-1})/(\gamma(1-\gamma)^2\lambda)$ can be shown to be $V_T(t) \approx V_{T0} + V_{gs} - \left(V_{gs}^{-1} + \gamma(1-\gamma)^2\lambda t\right)^{-1}$. Here, $\lambda = k/(C_i(L + 2L_{ov})Wh_m^3)$, V_{T0} is the threshold voltage when the masking semiconductor is not charged, C_i the gate dielectric capacitance per unit area, W the channel width, L the channel length, L_{ov} the source/drain-gate overlap length and k a fitting parameter defining the mask current (units A.cm^3/V^2). Since the coefficient $\lambda \propto h_m^{-3}$, decreasing the gate-mask underlap length, h_m, results in rapid screening and reduction in I_d with time. The parameter $0 < \gamma < 1$ defines the location of the masking semiconductor in the dielectric stack. When $\gamma \to 0$, the masking semiconductor is located at the gate interface and has a high initial potential resulting in a large mask current. However, its impact on V_T is low due to its location. When $\gamma \to 1$, the masking semiconductor is located at the primary semiconductor interface with a low initial potential and therefore a low mask current while having a high impact on V_T. The maximum screening rate is therefore

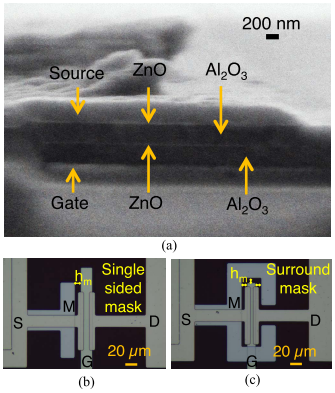

Fig. 3. (a) SEM cross-section of the adTFT (b) Micrograph of the single sided mask adTFT (c) Micrograph of the surround mask adTFT.

expected when the masking semiconductor lies close to the middle, i.e. when $0.3 \leq \gamma \leq 0.5$. Fig. 2(b) compares the I_d calculated using the models with TCAD simulations.

Based on the above discussion, it is seen that the adTFT can be used as a power efficient ESD protection device (Fig. 2(c)). During an ESD event, the rapid increase in V_{gs} resulting in a large I_d would shunt the surge current. During normal operation, the masking semiconductor would have sufficient time for channel formation thereby making I_d negligible and saving power.

III. Fabrication

The gate electrode was e-beam evaporated 75 nm Al on the Corning glass substrate. The adaptive dielectric stack was composed of 235 nm Al_2O_3 (top dielectric)-30 nm ZnO (masking semiconductor)-235 nm Al_2O_3 (bottom dielectric). The bottom and top dielectric were formed by e-beam evaporating Al_2O_3 at 7.5×10^{-2} mTorr with 4 sccm O_2 gas flow followed by annealing at 175°C for 30 mins. The masking semiconductor was rf sputtered ZnO at 2 W/cm^2 in Ar:O_2 (9:1) environment at 7 mTorr. The mask electrode was an e-beam evaporated stack of 10 nm Ti and 100 nm Al. The primary semiconductor (35 nm ZnO) was deposited by a process similar to the masking semiconductor. The source/drain (5 μm gate overlap) were an e-beam evaporated stack of 10 nm Ti and 100 nm Al.

Fig. 3(a) shows the cross-section SEM of the adTFT at the gate-source overlap region. Two types of adTFTs were fabricated - 'single sided mask' adTFT with the masking electrode on one side of the device (Fig. 3(b)) and the 'surround mask' adTFT with the masking electrode surrounding the device (Fig. 3(c)). The experimental control was an adTFT without the masking electrode. These devices behaved similar to conventional TFTs and are labeled as such.

IV. Results and Discussions

The dc current-voltage (I-V) characteristics of the conventional TFT (control), the 4-terminal adTFT (with the mask electrode open or floating) and the 3-terminal adTFT ($W = 200$ μm, $L = 10$ μm and $h_m = 10$ μm) were measured with $V_{ds} = 1$ V and V_{gs} swept in 0.1 V steps at ≈ 0.47 V/s. As seen in Fig. 4(a), the 4-terminal adTFT behaved similar to the conventional TFT due to the floating mask electrode whereas the 3-terminal adTFT behaved as predicted by the physics described in Fig. 2(a).

The dynamic performance of the 3-terminal single sided mask adTFT ($W = 300$ μm, $L = 10$ μm,

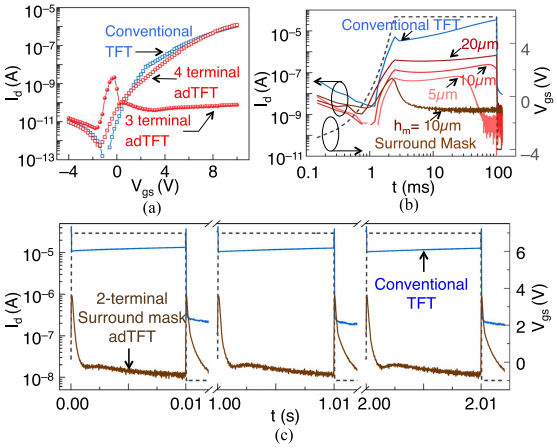

Fig. 4. (a) dc I-V characteristics of conventional TFT (control, blue) and adTFT (red). (b) Pulsed I-V characteristics of the conventional TFT (control, blue), single sided mask adTFTs with different h_m (in varying shades of red) and surround mask adTFT (brown). (c) Transient response of 2-terminal (diode connected) surround mask adTFT to a periodic gate pulse.

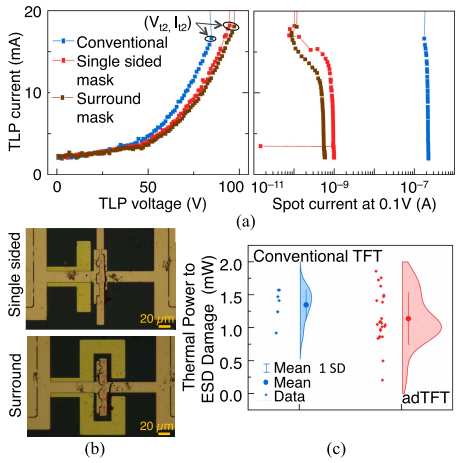

Fig. 5. (a) TLP I-V characteristics (b) adTFTs after failure (c) Power to thermal breakdown in conventional and adTFTs.

$h_m = \{5, 10, 20\}$ μm) and 3-terminal surround mask adTFT ($W = 300$ μm, $L = 10$ μm, $h_m = 10$ μm) in response to a single gate pulse (−4 V to 6 V, rise/fall time of 2.5 ms, pulse width 100 ms) is shown in Fig. 4(b). The single sided mask adTFT showed a lower masking time (i.e. quicker screening) with decreasing h_m, as predicted by the physics. The surround mask architecture showed a lower masking time compared to the single sided mask architecture due to carrier injection from multiple sides. The surround mask architecture would therefore improve power savings if normal system operation constituted pulsed line voltages (e.g. displays) as opposed to constant voltages.

Fig. 4(c) shows the response of the diode connected surround mask adTFT and a diode connected conventional TFT to a periodic gate signal (10 ms pulse width, 50 μs rise/fall time). It is noted that the peak $I_d \approx 1$ μA is smaller than typical ESD currents (100 mA-1 A). This is due to the slow rising pulse ($\sim$ 50 μs) where the shielding action diminishes I_d. An ESD event would be faster and I_d higher. Such conditions were tested via transmission line pulse (TLP) measurements (Fig. 5) [18]–[20].

Fig. 5 shows TLP measurements with the conventional TFT and adTFTs. Diode connected devices were subjected to a

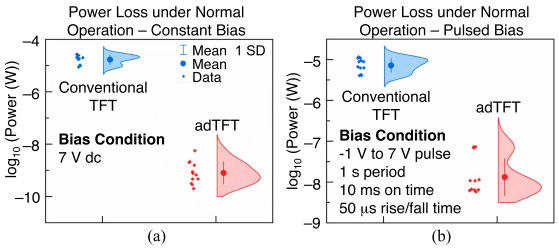

Fig. 6. Power loss in conventional TFTs and adTFTs during normal operation. Line voltage during normal operation being (a) dc (b) pulsed.

train of increasing voltage pulses (1 V increment, 100 ns pulse width, $\sim$ 1 s period, $\sim$ 10 ns rise/fall time) and the average I_d was measured during the pulse on period. After each pulse, dc spot current measurements at $V_{ds} = 0.1$ V monitored device degradation. Fig. 5(a) compares the TLP I-V characteristics for conventional TFT, single sided mask adTFT and surround mask adTFT (all devices $W = 200$ μm, $L = 5$ μm, $h_m = 10$ μm). Spot currents in adTFTs were low due to the shielding effect. All devices failed due to self heating with the source/drain thermally damaged and mask electrode not damaged (Fig. 5(b)). The failure point, (V_{t2}, I_{t2}), was observed to be (84.7 V, 16.6 mA), (94.7 V, 18.2 mA) and (97.2 V, 18.1 mA) with the power to thermal breakdown, $V_{t2}I_{t2}$, being 1.41 W, 1.72 W and 1.75 W, for the conventional TFT, single sided mask adTFT and the surround mask adTFT, respectively. ZnO based adTFTs showed a surge current shunting capacity of 0.08 mA/μm for $L = 5$ μm.

Fig. 5(c) and 6 show the statistics of device performance and highlight the primary advantage of the adTFT. Diode connected adTFTs showed similar ESD protection ability compared to the diode connected conventional TFTs as observed from the power to thermal breakdown (Fig. 5(c)). Since $V_{t2} \propto L$ and $I_{t2} \propto W$, the power to thermal breakdown of devices with different geometries were compared after normalizing with respect to WL. Despite similar ESD performance, diode connected adTFTs show more power saving during normal system operation as compared to diode connected conventional TFTs. To compare the power consumption of devices with different geometries, results were normalized with respect to W/L. Depending on whether normal operation consisted of dc (7 V dc) or pulsed operation (-1 V to 7 V pulse, 1 s period, 10 ms on time, 50 μs rise/fall time), the adTFT based protection circuit consumed $\approx 10^4$ and $\approx 10^3$ times less power compared to a conventional TFT based protection circuit, respectively (Fig. 6(a) and Fig. 6(b)). Since the power consumption in the conventional TFTs developed in this work is equivalent to other reports with metal oxide semiconductor TFTs [11], it is expected that the adTFT based protection circuits would have similar impact in terms of power savings across these materials. Finally, the layout area for conventional TFT based protection circuits sclaes as $\sim 2W(L + 2L_{ov})$, whereas the adTFT based protection circuit has a layout area that scales as $\sim 2W(L + 2L_{ov} + h_m)$.

V. Conclusion

This work discussed the architecture and physics of a new device called the adaptive dielectric thin film transistor (adTFT). When used for ESD protection, the adTFT permitted a large drain current during the rapid ESD event thereby shunting the current surge and drew little current during normal operation thereby saving power.

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