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ABSTRACT

In this work, we report the phase transition behavior of hydrogenated amorphous silicon on the application of nanosecond timescale high-field pulse electrical stress. The transition of amorphous silicon to nanocrystalline silicon, confirmed through Raman spectroscopy, is marked by an abrupt change in the pulse I-V characteristics. The mechanism of the phase transition at high electric field involving the avalanche generation of charge carriers and optical phonon generation is discussed. The role of defect states in optical phonon localization and eventual phase transition is explored. The phase transition in the case of devices with a drain-gate underlap is also studied. The role of self-heating in accelerating the phase transition has also been explored. The impact of channel dimensions on the onset of the phase transition is also discussed. Characterization of the resultant nc-Si is done through deconvolution of the Raman spectra, and the quality of nc-Si created is found comparable to earlier studies.

I. INTRODUCTION

Hydrogenated amorphous silicon (a-Si:H) is one of the most well-studied disordered semiconductors with versatile applications in large-area electronics. a-Si:H based devices can be fabricated with a low thermal budget (maximum temperature being less than 623 K) and, hence, can be used for flexible electronics applications.[1–4] These devices have also been used in a wide range of applications including sensing,[5,6] display drivers,[7,8] solar cells,[9] and light emitting diodes.[10] There are also a range of applications that utilize the phase transition of a-Si:H into a more crystalline state, and the phase change in a-Si:H through optical stimuli has been extensively studied using laser excitation[11–16] and solid phase crystallization.[17,18] These techniques, however, suffer from their fair share of limitations. The speed of phase transition through optical stimuli is limited by the spot size of the laser beam and its movement over the sample and ranges about a few hundred centimeters per second.[19] This can limit the economic viability of this technique when large substrate sizes are involved. Similarly, high temperatures involved in solid phase crystallization can limit the choice of substrates and form a bottleneck for flexible electronics based applications.

While it is important to understand the physics involving device operation and material properties of a particular technology, understanding the reliability constraints also has paramount importance lest device instabilities can hamper the usability of the technology. Thorough investigations have been performed to study various reliability issues in a-Si:H and nc-Si based thin film devices,[20–30] although a complete understanding of high-field behavior is still missing.[31,32] The application of a high field across the a-Si:H layer can lead to dense distribution of optical phonons (the optical phonon energy in a-Si:H is 58 meV) and could also lead to generation of defect states across the conducting channel.[31] This could lead to complex instability behavior, which may not be encountered during low-field operation.

At high-field application across the channel, phonon generation takes place. Phonon population in a channel is an intrinsic property, and, thus, to understand the phonon behavior in a channel, it is not merely sufficient to control the extrinsic parameters like ambient

temperature. To efficiently characterize the phonon behavior, it is important that: (1) The electrical signal applied to the device is applied for a very short interval so as to not cause excessive self-heating. (2) The device response is captured during the application of the electrical signal so as to understand the device behavior under thermal nonequilibrium. The application of a short electrical signal allows probing intricate features of device behavior.

In the course of this work, we have studied the high-field behavior of a-Si:H using an inverted staggered thin film transistor (TFT). The observed phase transition, which presents a unique reliability challenge at high-field conditions, has been studied in detail in this work. It is also worth noting that the observed phase transition behavior also provides an interesting approach to shift the phase of a-Si:H in short time intervals and with no requirement of extrinsic heating. We shall thus also discuss the quality of the resultant material generated and the impact of varying pulse conditions on the phase transition onset level. To understand the phonon behavior and its role in phase transition, electrical signals with pulse duration in the range of a few nanoseconds have been applied. This leverages the investigations at time scales comparable to thermal diffusion time and allows the device behavior to be characterized under thermal nonequilibrium conditions. It also provides an added advantage of providing better resolution of time scales involved in the phase transition.

II. EXPERIMENTAL DETAILS

Hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) used in the course of this work are fabricated in-house and have an inverted staggered configuration. The devices are based on a glass substrate. The aluminum-chromium layer deposited through electron-beam evaporation is used as the gate contact. The gate dielectric and active channel are formed by 200 nm thick silicon nitride and a 150 nm thick a-Si:H layer, respectively, both of which are deposited using a chemical vapor deposition process enhanced by plasma. The active layer and gate dielectric are subsequently patterned using reactive ion etching. Finally, the source and drain contacts are formed using molybdenum-aluminum metal layers, deposited using a DC based sputtering process and are subsequently patterned using a chemical wet etch process. To improve the quality of contact between the metal source-drain contacts and the semiconducting channel, a layer of highly n-doped a-Si:H is deposited between the metal and semiconductor layers. Figure 1 shows the typical DC current-voltage characteristics of a-Si:H TFTs used in the course of this work.

Figure 2 shows a schematic cross section of the setup used to study high-field nanosecond timescale pulse induced phase transition in a-Si:H. The experimental setup comprises an electrical part used for electrical investigations of nanosecond timescale high-field behavior and a LabRam HR Raman spectroscopy setup used to study any material changes in a-Si:H. The pulse electrical stress is applied on the drain contact of the device, while the source and gate contacts are grounded. The electrical setup has a characteristic impedance of 50 Ω. The device current is measured using a high bandwidth current sensor with a sensitivity of 0.5 mV/mA. The device response was then captured using a digital phosphor oscilloscope with a sampling rate of 25 gigasamples per second. The pulse

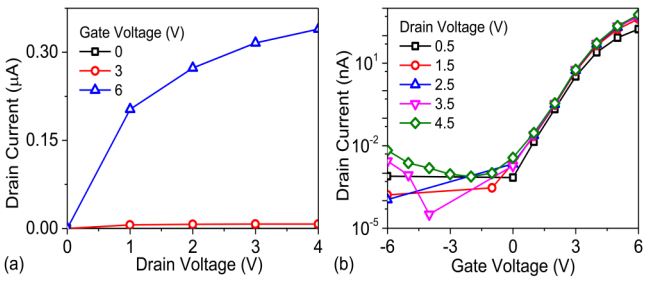

FIG. 1. Typical DC I-V characteristics of a-Si:H TFTs.

voltage is applied in steps with a predetermined step size, pulse width, and rise time. The voltage and current waveforms are then averaged for every pulse in a predetermined averaging window, with the average values used to plot a quasistatic pulse I-V curve [Fig. 2(b)]. As the voltage across the device is increased, Raman spectra of the device is measured using a Horiba LabRam HR spectrometer setup. A 532 nm diode-pumped solid-state (DPSS) laser with a laser power density of 4.5 mW/μm^2, and a spot size of 1.18 μm is used as the light source. The laser power density was kept intentionally low to avoid any detrimental effects of light on the a-Si:H layer. Transmission electron microscopy (TEM) is performed on a back-etched a-Si:H TFT fabricated on a silicon substrate in place of glass (shown in the supplementary material). TEM is performed using a Thermo Titan Themis setup employing a extreme field emission gun at 300 kV. The sample used for TEM

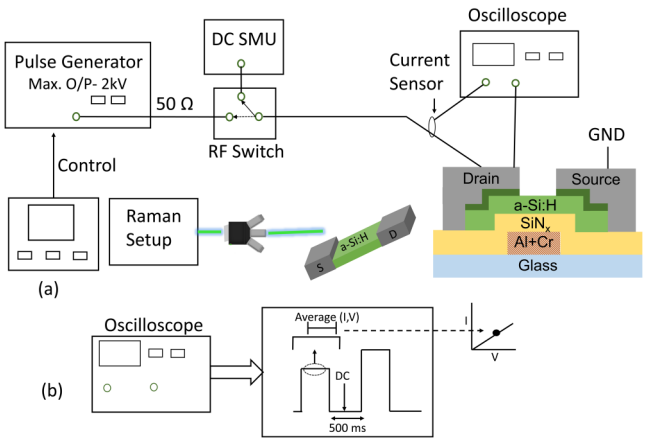

FIG. 2. (a) Schematic view of the experimental setup used in the course of this work. Pulse characterization is done using a four probe pulse setup as shown. Post each electrical pulse, an off-time of 500 ms is undertaken to facilitate the establishment of thermal equilibrium. A RF switch is used to alternate between the pulse voltage and a low voltage DC bias, which is used to study any device degradation in the aftermath of each electrical pulse. (b) The quasistatic pulse I-V is plotted by averaging the current and voltage waveform in a predetermined averaging window, and the resultant I,V values are used as a single data point in the I-V characteristics.

is prepared using a Helios G4 UX focused ion beam (FIB) setup. Platinum is coated over the sample to provide a conductive surface. Using the silicon substrate instead of glass provides an advantage of a conductive back surface for the gallium ions (during FIB milling) and electrons (during TEM characterization).

III. RESULTS AND DISCUSSION

A. Phase transition in a-Si:H TFTs

Figure 3(a) depicts the quasistatic pulse current-voltage (I-V) characteristics of an a-Si:H device. The voltage pulses applied to the device have a pulse width of 100 ns and a rise time of 10 ns. It can be observed from Fig. 3(a) that the device I-V characteristics depict two distinct modes of operation: Region 1 with a low device current and a high device resistance and Region 2 with a significant device current and a lower device resistance. The drain current is immeasurably low in region 1 of operation due to high device resistance, which is a consequence of low mobility of charge carriers in a-Si:H (the least count of pulse setup is in the range of microamps). To understand the reason behind the observed abrupt increase in the device current, Raman spectroscopy is done across the a-Si:H channel, postcurrent increase and at multiple stress levels in region 1 of operation as is shown in Figs. 3(b)–3(e). The Raman spectra at voltage levels A, B, and C show a high full-width at half maxima (FWHM) and is centered around 480 cm^{-1}, which corresponds to the transverse optical phonon peak of amorphous silicon. This is in contrast to the Raman spectra of the channel layer at voltage level D (region 2), where the transverse optical phonon peak shifts to 516 cm^{-1} and presents a much lower FWHM, signifying a reduction in the degree of disorder as compared to other voltage levels. These observations point to the fact that with increase in the voltage across the a-Si:H channel, phase transition of a-Si:H to a state of increased crystallinity takes place. The observed phase transition eventually leads to a higher device current in region 2 [Fig. 3(a)]. It is also observed that the phase transition is an abrupt phenomenon, and there is no accumulative effect as the voltage levels are increased. To further understand the observed behavior, SEM spectroscopy of the device is performed. Figure 3(f) shows the SEM images of the device. As the magnification levels are increased, it is observed that in the case of device discussed, the phase transition does not take place across the entire channel width and only takes place in a concentrated area of the channel. On further probing, nanosized particles of c-Si are observed, further confirming phase transition. It is also observed that there is some degree of damage to the metal contacts as well, which is a result of joule heating due to high current levels involved. TEM characterization is also performed to gain further insights. It can be observed from the small area electron diffraction pattern (the inset of Fig. 4) that there are bright spots in a diffuse ring, signifying the presence of nanometer sized silicon crystallites in an amorphous background. This is observed in HRTEM imaging (Fig. 4), where both crystalline and amorphous components are observed. To further confirm the phase transition behavior, AFM imaging is performed. Figure 5 shows the AFM topographical images of the

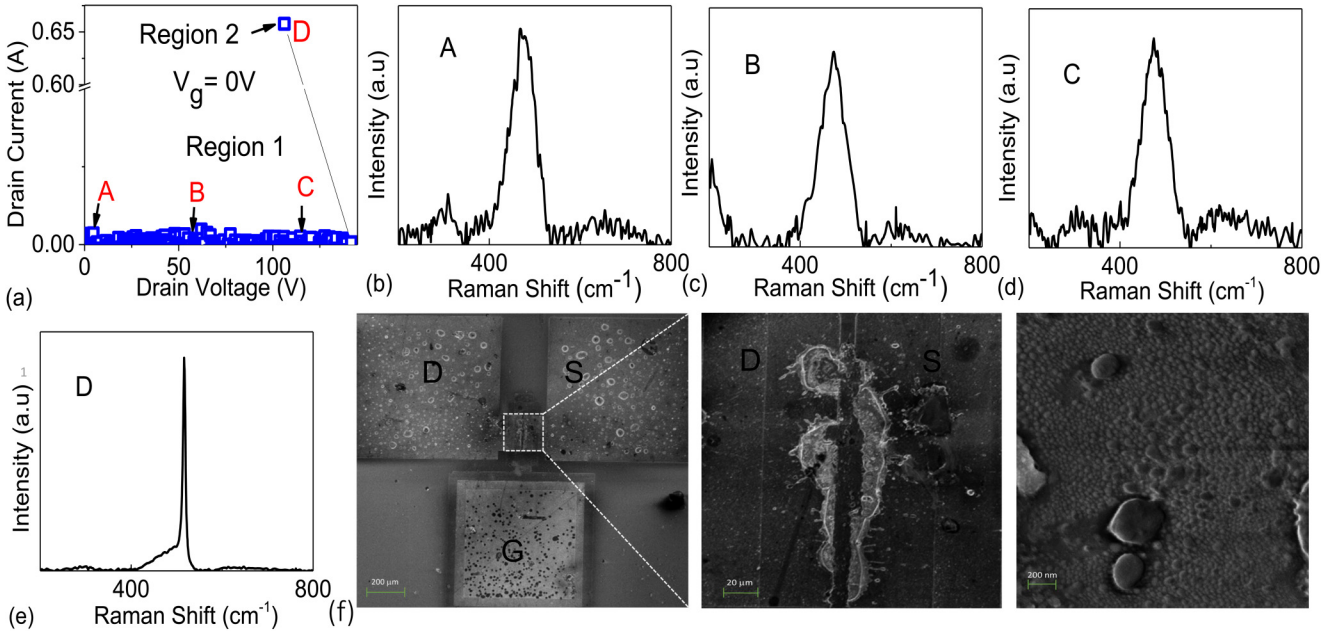

FIG. 3. (a) Nanoscale time resolved pulse I-V characteristics of a-Si:H thin film transistors displaying two separate behavioral modes. (b)–(e) Raman signature at various voltage levels. Raman signature at initial conditions (point A), at 60 V level (point B), and at 120 V (point C) level shows an amorphous a-Si:H, while the Raman signature at region 2 points toward a phase transition to a nanocrystalline state. (f) Post-transition SEM micrograph of a-Si:H TFTs showing partial phase transition in the a-Si:H channel. Observed damage to contacts is due to high current in region 2. Nanocrystalline silicon particles are observed.

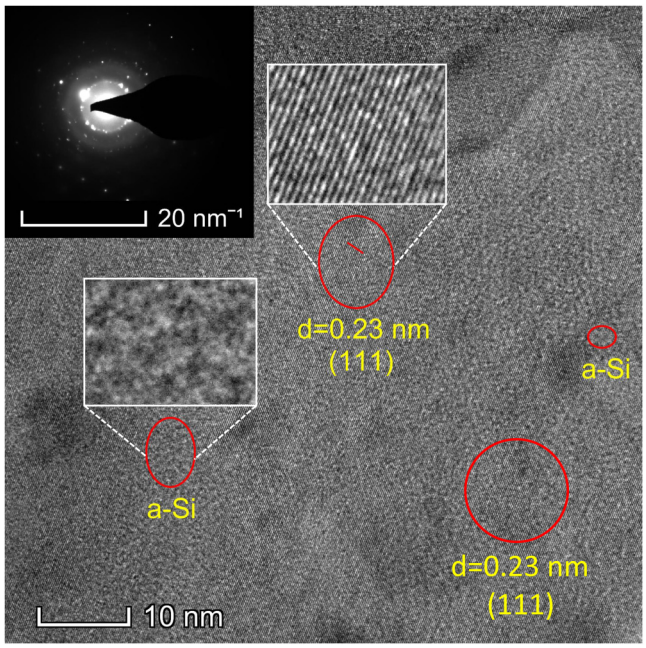

FIG. 4. HRTEM image of nc-Si postphase transition with the selected area electron diffraction pattern (inset).

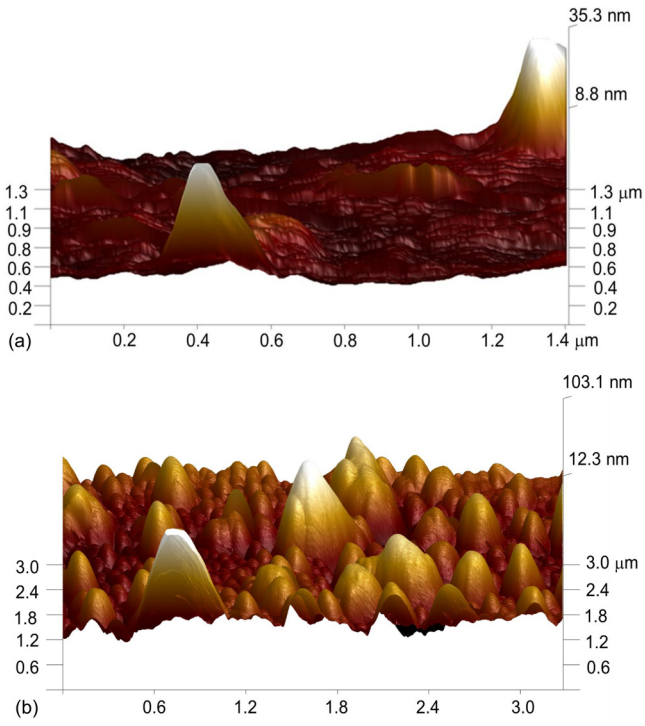

FIG. 5. AFM topography of (a) the a-Si:H layer and (b) the nc-Si layer, showing the presence of nanometer sized particles.

a-Si:H channel and nc-Si layer. It is observed from Fig. 5(b) that nanometer sized particles are present in the nc-Si surface, which are not observed in the a-Si:H channel. These particles are formed by grouping multiple nc-Si crystallites and possibly metal atoms. This is further confirmed through energy dispersive x-ray spectroscopy (EDS; shown in the supplementary material).

The device discussed above has a channel length of 6 μm and enters region 2 at a voltage level of around 141 V, leading to a critical electric field of 23.5 V/μm. Optical phonon energy in a-Si:H is approximately 58 meV and at a field of 23.5 V/μm, and optical phonons are generated every 2.45 nm in the channel. This dense distribution of optical phonons across the channel leads to an increase in the channel temperature, which eventually results in the observed phase transition of the channel a-Si:H. Phonon population depends on electron-phonon interactions and at high electric fields impact ionization due to collision between highly energetic electrons and a-Si:H network increases, which leads to energy redistribution between the network and electron. This results in either (or both) further generation of energetic charge carriers or that of phonons, both of which would further increase the phonon population in the channel region. At critical field levels, the avalanche generation of charge carriers takes place, resulting in a dense optical phonon distribution across the channel, thus leading to phase transition of the channel layer. Transient voltage and device current at various electric field levels are plotted in Fig. 6. It can be observed that the shift in voltage and current waveforms has a time lag of a few nanoseconds. This time lag is attributed to the time delay between the onset of avalanche generation phenomenon and eventual phase transition.

Now that we have understood the physics behind the phase transition, the question arises as to whether the phase transition takes place uniformly across the channel or not. Further observation of the transient current waveforms (Fig. 6) reveals that the current increment takes place in the time period of a few nanoseconds and eventually reaches a maximum value. The device current in this time period follows a linear increase and can be explained through localized onset of transition, leading to an incremental decrease in device resistance, which further spreads across the channel region until a maximum value is achieved. To probe this behavior, capacitance-voltage measurements of a-Si:H TFTs were

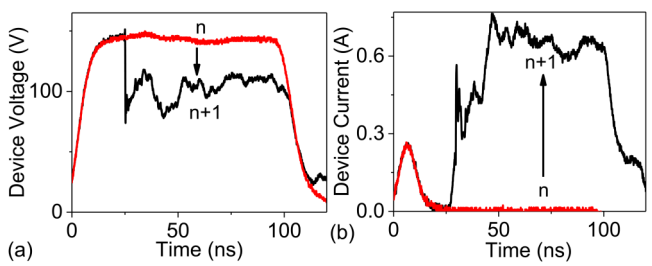

FIG. 6. Transient (a) device voltage and (b) device current as a function of time during the 100 ns wide stress pulse. The pulse preceding the phase transition is referred to as n. There is a drop in device voltage and an increase in device current as the phase change takes place accompanied by a rise in device current.

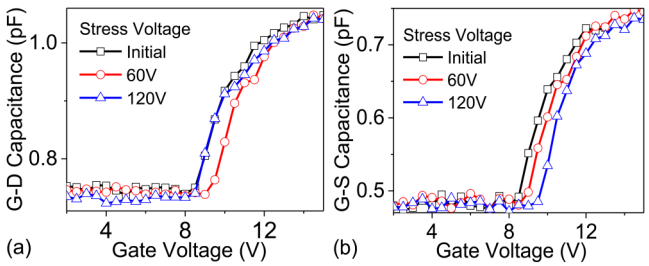

FIG. 7. (a) and (b) Capacitance-voltage characteristics of a-Si:H TFTs at different voltage levels. As the applied voltage levels are increased, both drain-gate and source-gate capacitance shift in a parallel fashion, signifying charge trapping in the dielectric. Further increasing the stress, drain-gate capacitance presents a stretched behavior, signifying localized defect formation near the drain side of the channel.

done at various voltage levels. Figure 7 presents the results of capacitance-voltage measurements. It has been observed that at lower stress levels, both source-gate capacitance and drain-gate capacitance show a similar shift due to charge trapping in the dielectric layer. Further increasing the voltage across the device, the source-gate and drain-gate capacitance diverge, and while source-gate capacitance presents a monotonous shift, the drain-gate capacitance presents a turnaround in a stretched out manner. This leads to the fact that as the voltage across the device is increased, defects are generated in the channel in a spatially nonuniform fashion near the hot contact. These defects lead to scattering of optical phonons and restrict the heat transport from the hot contact, thus leading to local increase in temperature near the contact.[33] Thus, the phase transition initially takes place in the region near the hot contact (drain), where the defects are generated, and electric field has the highest magnitude and further spreads across the a-Si:H channel, leading to an observed increase in current until it reaches the cold contact (source), at which point the current assumes its peak value. The decay of optical phonons in a-Si:H is done through hopping to a phonon mode of lower energy, and the energy difference is taken up by a low frequency phonon.[34] This leads to a decay time of around 70 ns for an optical phonon in a-Si:H,[35] which implies that the phase transition due to localized heating would happen before the phonon relaxation could also take place.

B. Phase transition in drain underlap devices

At this point, we have analyzed the phase transition behavior in a-Si:H at high-field conditions. The role of high-field charge carrier generation and phonon generation was explored, and it was discussed that the observed phase transition was a result of dense phonon distribution across the channel at high-field condition. It was also discussed that the defects restrict the heat flow and localize the phonons near the hot contact, leading to the onset of phase transition near the hot contact. To further analyze this behavior, devices with underlap between the gate edge and hot contact edge were characterized (referred to as drain underlap devices). Figure 8 shows the schematic cross section of the TFTs with a drain-gate underlap.

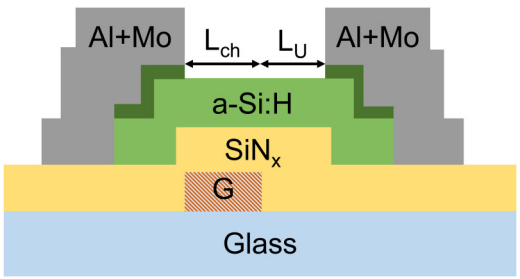

FIG. 8. Schematic cross section of TFTs with a drain-gate underlap. L_{ch} denoted the channel length, while L_U is the length of the underlap region.

Figure 9 presents the relation of phase transition onset voltage (referred to as onset voltage) with varying underlap length and channel length. It can be observed that as underlap length increases, a-Si:H channel undergoes phase transition at a higher field level. This can be described as follows: In conventional devices, the electric field has maxima at the edge of the drain and gate contact, while in the case of the drain underlap devices, the underlap region (L_U) relaxes the electric field and reduces the field maxima. This translates to higher applied voltage levels for phase transition as compared to conventional devices.

C. Factors affecting phase transition behavior

In Secs. III A and III B, we have studied the physics of phase transition involving phonon generation and defect creation under the application of nanosecond timescale high-field electrical pulses. In this section, we analyze the phase transition behavior by varying pulse parameters and device dimensions and studying their impact on the device behavior.

Figure 10(a) depicts the variation of onset voltage with channel width and length. It is observed that the onset voltage scales with channel length while showing little dependence on channel width. This can be attributed to the reduction of electric

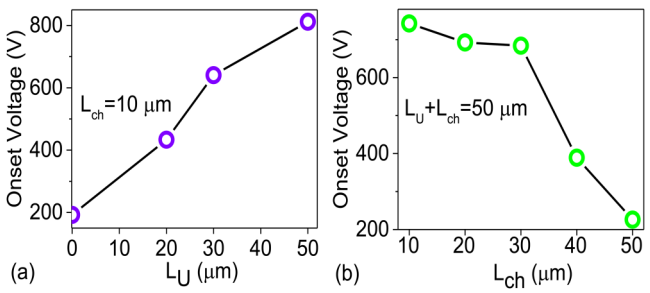

FIG. 9. Variation of phase transition onset voltage with (a) underlap length. The underlap region provides field relaxation and increases the onset voltage. (b) Channel length for devices with constant source-drain distance. As the channel length increases (underlap length reduces), onset voltage reduces.

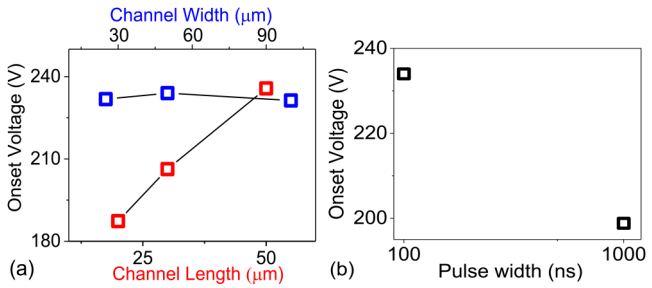

FIG. 10. (a) Variation of phase transition onset voltage with channel dimensions. (b) Variation with pulse width. The observed behavior points to an electrothermal nature of phase transition under high-field nanosecond pulse conditions.

field in the channel with channel length. Channel width, however, does not manipulate the electric field and thus presents no impact.

Figure 10(b) depicts the impact of pulse width on the onset voltage. Increasing the pulse width leads to an increased phonon generation, further reducing the critical electric field required for the onset of phase transition. It has also been studied that an increased degree of self-heating also increases the defect concentration.[36] As discussed earlier, defects restrict heat transport and further accelerate the onset of phase transition. These combined observations from Fig. 10 also concur with the electrothermal nature of the phase transition in a-Si:H as described so far.

Figure 11 shows the quasistatic I-V characteristics of the devices, where the pulse stress has been applied to the device at varying gate biases. It can be observed that the device operating in the on-state ($V_G = 8$ V) undergoes phase transition at a higher electric field as compared to the device operating in the off-state ($V_G = -6$ V). This can be explained by the fact that the device in accumulation offers a lower channel resistance. This reduction in resistance presents itself as a higher field required to induce the phase transition of a-Si:H.

D. Characterization of resultant silicon

So far in this paper, we explored the mechanism of phase transition in a-Si:H and studied the impact of pulse parameters on the phase transition behavior. We also observed that the high-field phase transition takes place in a time period of a few nanoseconds across the micron scale channel length (speed in the range of 1000 m/s) and that there is no requirement of external annealing. In this section, we shall take a look at the properties of the resultant nc-Si.

Analysis of the Raman spectra postphase change is done by deconvolution of the spectra into the gaussian components corresponding to amorphous silicon, nanocrystalline silicon (nc-Si), and that of grain boundary effects (discussed in detail in the supplementary material). This analysis provides important quantitative information about the quality of the resultant material. Figure 12 depicts the distribution of crystallite sizes of nc-Si along the channel area. It is observed that, for the device discussed, a part of the active layer is still amorphous in nature. As we move along the channel width, silicon begins to crystallize with crystallite sizes in the range of a few nanometers (and thus nc-Si). It is also observed that the extent of crystallization is higher on the hot contact side as compared to cold contact. Bond angle deviations and crystallization factors of nc-Si are depicted in the supplementary material and are in the range of 2°–10° and 0.4–0.93, respectively. This is comparable to what has been reported earlier for nc-Si[37] and shows that the discussed phase transition technique provides a decent quality of nc-Si. Analysis of HRTEM images (Fig. 4) shows that the interplanar distance of 0.23 nm is observed in the crystalline component, which points to the presence of the [111] plane in the

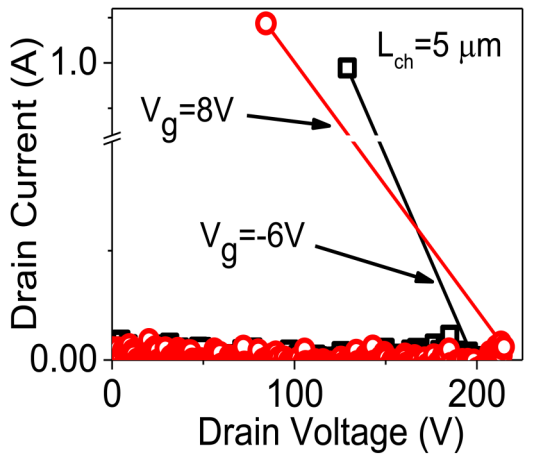

FIG. 11. Pulse I-V characteristics of a-Si:H devices under different gate biases. The device in accumulation shows a higher onset voltage due to reduced channel resistance.

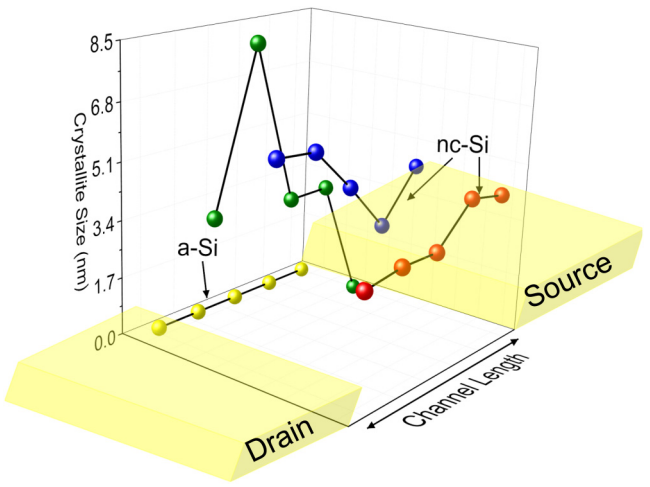

FIG. 12. Crystallite size distribution of nc-Si along the channel area. Crystallite sizes are in a range of a few nanometers.

resultant nc-Si.[38] It is, however, also interesting to note that the [220] plane is also observed on analysis of HRTEM images at other points in the sample (shown in the supplementary material).

IV. CONCLUSION

In this work, we have investigated the phase transition of a-Si:H on the application of nanoscale time resolved high-field electrical pulse stress to nanocrystalline silicon. The phase transition is confirmed through Raman spectroscopy, scanning electron microscopy, and transmission electron microscopy. It was observed that the resultant nc-Si has a mean crystallite size in the range of a few nanometers and that it shows a reasonably short range order. Through Raman spectroscopy, it was reported that the phase transition is an abrupt phenomenon. It was discussed that at high critical fields, a dense distribution of optical phonons is generated in the a-Si:H channel, which eventually leads to phase transition. It was also discussed that this behavior is accelerated by impact ionization at high fields. Analysis of transient current and voltage waveforms revealed a time lag between the avalanche generation and the eventual phase transition. Further analysis of transient current waveforms revealed that phase transition takes place in the entire channel in a period of a few nanoseconds. It was discussed that the onset of phase transition is a localized phenomenon and that it initiates near the hot contact. This behavior was attributed to localized defect formation near the hot contact, since defects lead to heat localization through optical phonon scattering and trapping. We also discussed the impact of self-heating and channel dimensions on high-field phase transition. Finally, it was discussed that reducing channel resistance increases the field required for phase transition.

SUPPLEMENTARY MATERIAL

See the supplementary material for the following: (1) A detailed description of the pulse characterization setup. (2) A cross-sectional image of the sample used for TEM characterization. (3) EDS characterization results of different crystallites. (4) A description of deconvolution of the Raman spectra. (5) The bond angle deviation and Raman crystallization factor of various points discussed in Fig. 12. (6) The HRTEM image of the sample showing the presence of the [220] plane.

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