ESD Reliability Study of a-Si:H Thin-Film Transistor Technology: Physical Insights and Technological Implications

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***Abstract*— In this paper, we present the detailed physical insights into the electrostatic discharge (ESD) behavior of hydrogenated amorphous silicon (a-Si:H)-based thin-film transistor (TFT) technology. Device failure under ESD conditions is studied in detail using electrical and optical techniques. Device degradation under ESD timescales is studied using real-time capacitance–voltage and a spatially variant degradation behavior is reported. Variations in material properties are studied before and after device failure using Raman spectroscopy. Device dimension-dependent failure mechanism is explored. Impact of stressing conditions and presence of top passivation on failure behavior is also explored. Failure physics of technologically relevant device architectures including diode-connected transistors (gated diodes) and drain underlap TFTs and their increased ESD robustness is discussed. Finally, ESD behavior of a-Si:H-based TFTs is discussed.**

***Index Terms*— Amorphous silicon, defects, dielectric breakdown, drain underlap, electrostatic discharge (ESD), gated diodes, thin-film devices.**

I. Introduction

THIN-FILM transistor (TFT) technology plays a pivotal role in flat panel displays [1], flexible electronics [2], bioelectronics [3], and sensing applications [4]. TFTs can be fabricated on substrates such as glass and novel flexible substrates. The presence of these substrates restricts the thermal budget of the fabrication process and requires the use of those materials that have low processing temperatures. Hydrogenated amorphous silicon (a-Si:H) is one such material that can be processed at low temperatures (< 350 °C) and has been used for a variety of applications including sensing [5], [6] and in display driver circuits [7] and is one of the widely used material for TFT technology.

ESD is a transient phenomenon caused due to the transfer of static charge from one body to another on account of their potential difference. ESD events can cause direct, indirect, or latent failures in microelectronics devices and becomes even more serious due to the increasing level of integration in VLSI technology. A device can be exposed to ESD events at any phase of its lifetime including fabrication up until its final usage [8]. ESD events occur in the timescale of a few nanoseconds and form a significant fraction of overall failure rates observed [9]. In light of these reasons, it is important to understand and explore the ESD reliability of a-Si:H TFTs. While preliminary work has been done to understand the instabilities in the operation of a-Si:H TFTs [10]–[16] and the ESD behavior of amorphous semiconductor-based TFTs, including a-Si:H TFTs [17]–[23], a gap still exists in the understanding of the ESD behavior of these devices, both from a physical and technological point of view. This work, which is an extension of our earlier work [24], provides insights into physics and technological aspect of ESD behavior of a-Si:H technology starting with details of the TFT fabrication and characterization techniques in Section II. In Section III, the physics of device degradation under ESD stress is discussed by exploring device electrical and material characteristics with stress. Section IV presents the factors that impact the ESD behavior of a-Si:H TFTs including stress time, device dimensions, and applied gate bias. Furthermore, Section V presents the ESD behavior of a-Si:H diode-connected transistors (gated diodes), drain underlap devices, and TFTs on account of their potential applications in a-Si:H-based technology. Finally, these findings are concluded in Section VI.

II. Device Fabrication and Characterization

Fig. 1 shows the cross section of back-channel passivated and back-channel etched TFT used in this work. Corning glass, cleaned using Piranha solution is used as the substrate. The fabrication process starts with the processing of Aluminum/Chromium gate which is formed by electron-beam evaporation on a glass substrate and is patterned using a wet etch process. Post-metallization of the gate electrode, a series

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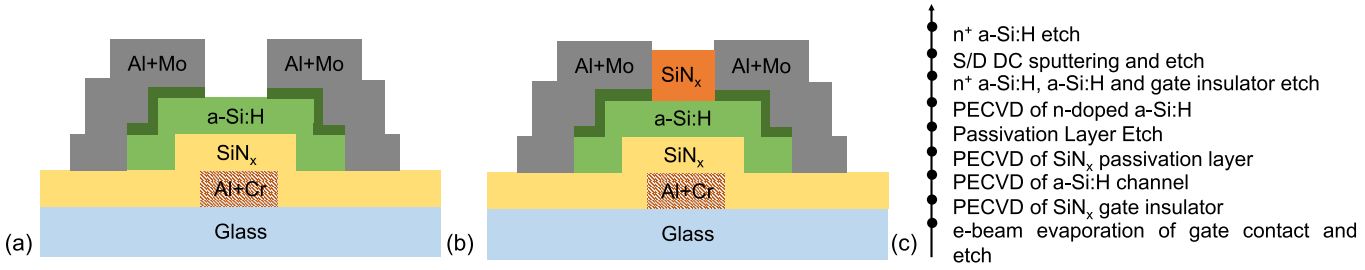

Fig. 1. Cross section schematic of (a) Back-channel etched. (b) Back-channel passivated TFT used in this paper. (c) Flow of the fabrication process used for back-channel passivated devices.

of plasma enhanced chemical vapor deposition (PECVD) processes are carried out to deposit 200 nm thick layer of silicon nitride (SiN_x), a 150 nm thick layer of a-Si:H, and 300 nm thick layer of SiN_x. The a-Si:H forms the channel material, whereas the gate dielectric and the passivation layer are formed by SiN_x. Following the patterning of the passivation layer, a 30 nm thick layer of n-doped a-Si:H layer is deposited using PECVD. Subsequently, the active layer and the gate insulator are patterned using reactive ion etching (RIE). The source/drain electrodes (Molybdenum/Aluminum) are deposited using dc sputtering and patterned by the wet etch process. Finally, RIE is employed to etch out the n-doped a-Si:H layer from the channel region. The devices were annealed at 423 K for a period of 1 h before further characterization.

ESD characterization is done using a commercial 50-Ω transmission line pulse (TLP) setup [25], with an ultralow current sensing capability. A voltage pulse generator, which can force up to 2 kV with pulse widths ranging from 1 ns-1.5 μs, is used to force voltage stress pulses to the device under test (DUT). The current response from the DUT is then measured by a current sensor and the transient waveforms are captured using a 4 GHz digital phosphor oscilloscope. A current sensor with a sensitivity of 0.5 mV/mA is used in the course of this work. The four probe measurement setup extracts the I–V characteristics of the DUT by averaging the transient waveform in a predefined averaging window (here, 60%–80% of the pulse width) and the averaged data are used to plot a quasi-static I–V characteristics of the DUT. Stress-induced device degradation is tracked using a one point dc measurement at a low voltage bias, called spot measurement. The voltage pulse generator and dc source measuring unit (SMU) are connected to a state-of-the-art mechanical reed switch, which is used to alternate between the pulse and the dc mode. The setup is calibrated using a standard surface mount resistor and a Zener diode. Unless stated otherwise, ESD stress pulses of width 100 ns and rise time 10 ns are applied on the drain contact while the source and gate contacts are grounded.

Exploration of stress-induced device degradation and changes in material properties are done by integrating the TLP with the dc measurement and Raman spectrometer setup. Real-time current–voltage (I–V), capacitance–voltage (C–V) are done to understand the role of surface and/or bulk traps in device degradation. Micro-Raman spectroscopy is used along with SEM imaging to study the stress-induced material changes taking place in the device, which has been done using

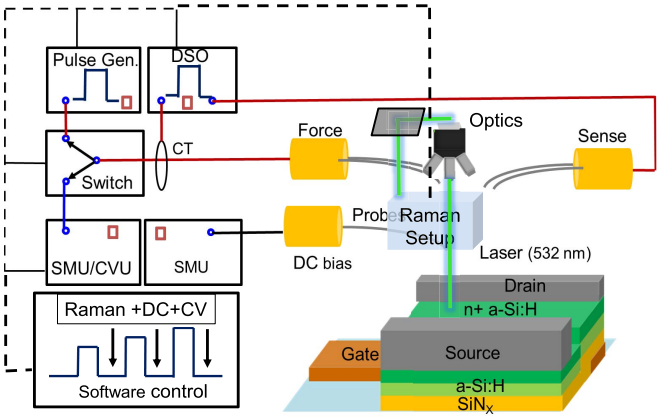

Fig. 2. Illustration of the setup used to explore stress-induced device degradation. TLP setup comprises of a voltage pulse generator, a current sensor (CT) with a sensitivity of 0.5 mV/mA and 4 GHz oscilloscope (DPO). The voltage and current waveforms across the DUT were averaged to obtain I–V characteristics. A mechanical switch is used to alternate between TLP pulse and low bias dc. TLP setup is integrated with a dc measurement setup comprising of a source measure unit and capacitance-voltage unit and Raman spectrometer. These measurements are done at desired voltage levels to explore degradation and material changes with stress.

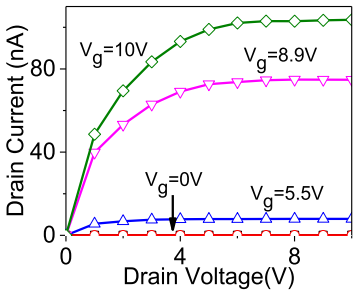

Fig. 3. Typical dc characteristics of a-Si:H TFTs. The device used here has a channel width of 100 μm and a channel length of 10 μm. The saturation current is around 100 nA at the gate bias of 10 V. Source/Drain contact form an ohmic contact with the active layer due to the presence of highly n-doped a-Si:H layer.

a 532 nm laser at a laser power density of about 4.5 mW/μm^2 and a spot size of about 1.18 μm. Fig. 2 shows the illustration of the setup comprising of TLP setup integrated with dc characterization and Raman spectrometer setup used in the work. Fig. 3 shows the dc characteristics of devices under test.

III. ESD Behavior of a-Si:H Thin-Film Transistors

A. TLP Characteristics and Device Failure Mechanism

Fig. 4 depicts the TLP characteristics of a-Si:H TFTs. Two modes of operation are apparent in the TLP

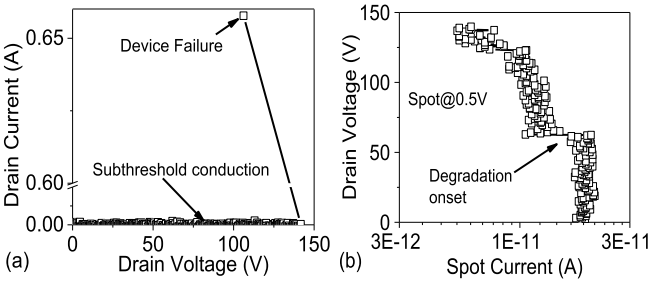

Fig. 4. (a) TLP I–V characteristics and (b) spot current characteristics depicting breakdown and degradation behavior of TFTs. TLP current in a-Si:H TFTs is lower than the least count of the setup due to low mobility in a-Si:H. Spot measurements show that the device degradation sets in after the stress level of 60 V.

I–V characteristics: 1) sub-threshold conduction, where the DUT operates in linear region with a high ON-resistance and 2) device failure, characterized by voltage snapback and a sudden increase in the TLP current. Due to the low mobility of charge carriers in a-Si:H, a-Si:H TFTs offer a high ON-resistance in the linear region, resulting in drain current being lower than the least count of the TLP setup. It can also be observed from the spot characteristics that the device degradation starts to take place once the drain is stressed at voltage levels higher than 60 V, which is the threshold of degradation in these devices.

The device failure is marked by an abrupt increase in device current and drop in the voltage level across the device [Fig. 4(a)]. Device failure is attributed to localized avalanche generation assisted thermal breakdown. As the device is stressed, localized regions with a higher rate of impact ionization compared to other regions in the channel are formed across the device. As the stress field further increases, avalanche generation takes place and leads to the increased scattering of a-Si:H lattice with the charge carriers, leading to an increased local temperature. A rise in the temperature will further lead to thermal generation of charge carriers and detrapping of charge carriers from the defect states in a-Si:H. This further aids the avalanche generation and forms a positive feedback loop, eventually leading to a thermal breakdown of the device. It is worth highlighting that the failure observed in these devices could be present either in the complete channel width or in a localized region, depending on the channel width in the devices. SEM micrograph in Fig. 5 shows a device with a partially damaged channel region. Transient waveforms are shown in Fig. 6, depicting the reduction in the voltage level across the device and an increase in the device current at the damage. The observed time delay($\simeq$5 ns) in transient voltage and current waveforms (Fig. 6) is caused due to a time lag between the onset of the avalanche generation and thermal failure in the device. The failure phenomenon is summarized in Fig. 7. As the device failure takes place, the current across the channel increases and further causes peeling and melting of the contacts in the proximity of the damaged channel region due to Joule heating [26] as is shown in SEM micrograph in Fig. 5. Fig. 8 shows the Raman spectra of the device before and after the failure takes place. It can be observed that the Raman peak shifts from 480 to 516 cm^{-1} indicating a phase transition from amorphous to the nanocrystalline state

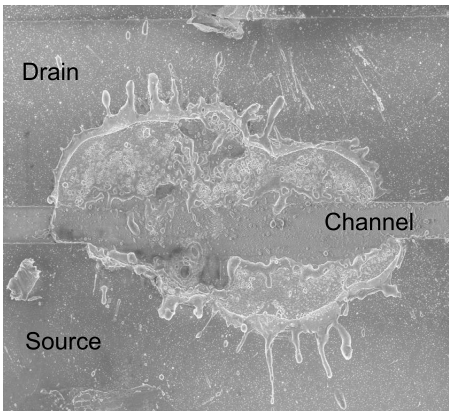

Fig. 5. Post-failure SEM micrograph of TFT device with a damaged active layer. Damage occurs locally in the channel region which creates a short between source and drain. Joule heating due to excess current during failure leads to contact melting.

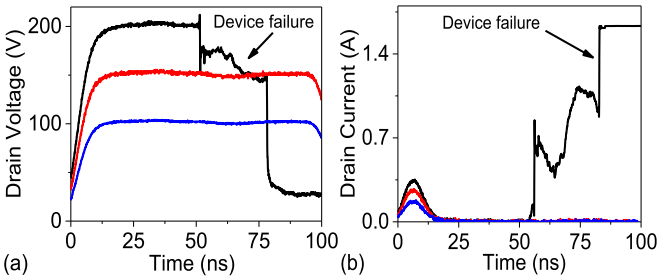

Fig. 6. (a) Transient voltage and (b) current waveforms of the device under ESD stress. Transient voltage and current waveforms show an abrupt change with the device damage. There is a time delay between the transient current and voltage waveforms at the damage.

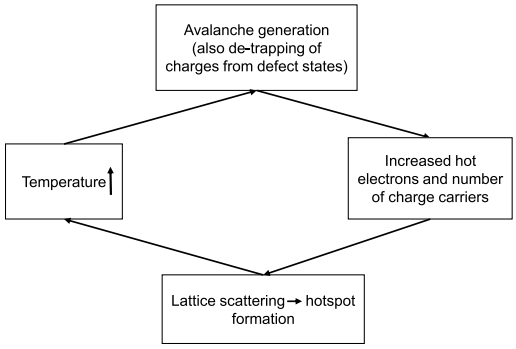

Fig. 7. Schematic of the phenomenon leading up to device failure in a-Si:H TFTs. The device failure is caused due to electric field-induced thermal breakdown.

of silicon [27]. It can also be observed that the full-width at half maximum (FWHM) of the Raman peak also reduces postfailure. Reduction in FWHM postfailure shows a reduction in the disorder of the system, which further corroborates the conversion of amorphous silicon to a more crystalline form as failure takes place. This phase transition takes place due to temperature increase taking place during the avalanche generation-induced thermal failure.

B. Pre-breakdown Degradation

To understand the physics behind the degradation in devices' electrical and material characteristics when subjected to ESD stress, real-time C–V, and Raman spectroscopy is done using the setup illustrated in Fig 2. Fig. 9 shows the C–V characteristics of the device under varying ESD stress

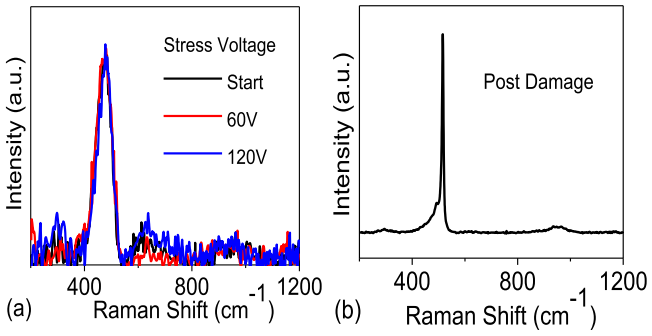

Fig. 8. Raman spectra (a) before and (b) after device failure. There is no shift in Raman signal with stress before the permanent device failure depicting the absence of material change as a function of stress. Postdamage, Raman peak shifts to 516 cm^{-1}, depicting a change from amorphous to nanocrystalline state of Si due to excessive channel heating during device failure.

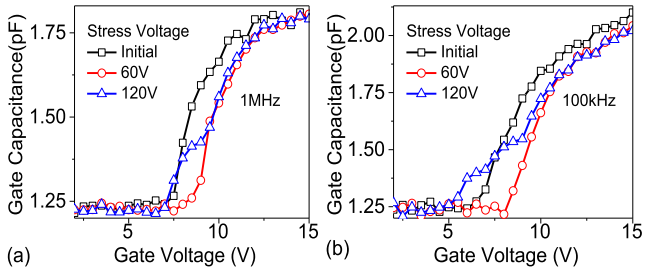

Fig. 9. Capacitance–voltage characteristics of device stressed under 100-ns condition at (a) 1 MHz and (b) 100 kHz. The non-parallel shift at higher stress is attributed to creation of defect states.

levels. It can be observed that initially as stress level increases, there is a parallel shift from the initial characteristics. Further increasing the stress level leads to partial recovery of C–V characteristics. These observations can be explained by the trapping of electrons in the dielectric at lower stress levels and an increase in the concentration of defect states as the stress further increases. The difference in the behavior at 100 kHz and 1 MHz is attributed to the frequency response of the defect states. To further study the spatial variation of the degradation mechanism, C–V characterization is done between the gate–drain (G–D) and gate–source (G–S) contact with other contacts kept open (Fig. 10). It is observed that the recovery of the threshold voltage and C–V characteristics takes place in drain region, whereas a monotonous degradation takes place in the source region of the channel. The recovery of C–V characteristics near the drain contact can be attributed to the dominance of defect creation mechanism at higher stress levels, while electron trapping dominates near the source contact. It is also observed from Fig. 8 that there is no change in the material properties with increasing stress pre-breakdown and that the phase transition takes place only at breakdown field.

IV. Factors Influencing ESD Behavior

Further investigations on the ESD behavior of a-Si:H TFTs are done by varying the stressing conditions and device architecture. Variation in channel dimensions modulates the electric field and can play an important role in determining the failure mechanism. To explore the effect of channel dimensions on breakdown mechanism, devices with varying device

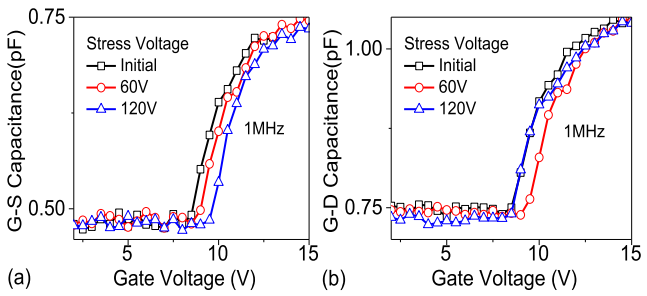

Fig. 10. Capacitance–voltage characteristics of device stressed under 100-ns condition. (a) G–S capacitance. (b) G-D capacitance at 1 MHz. The difference in the G–S and G–D characteristics is due to spatially variant degradation mechanism.

channel dimensions are characterized under ESD conditions. Figs. 11 and 12 depict the TLP I–V characteristics of the device with varying channel dimensions and variation in breakdown voltage with channel dimensions, respectively. It can be observed that as the channel length increases, breakdown voltage initially increases and then saturates. It is also observed that as channel width increases, breakdown voltage initially remains constant and then decreases. These observations can be explained as follows: for smaller channel dimensions, avalanche assisted thermal breakdown dominates the failure, whereas for larger dimensions, dielectric breakdown dominates the failure. The former requires a critical electric field along the channel length for breakdown to take place and hence breakdown voltage scales with channel length but not channel width. Once the channel dimensions have increased to a point where the critical voltage level required for avalanche generation is higher than the voltage level required for dielectric breakdown, dielectric breakdown starts to dominate the failure behavior. It is also observed that devices with a constant width/length ratio have varying breakdown voltages. This is caused due to the difference in actual device dimensions and, hence, failure mechanism. For devices with smaller channel widths, breakdown voltage scales with the channel length; however, for devices with larger channel widths, it is lowered due to an increased probability of failure due to dielectric breakdown phenomenon.

To further explore the thermal nature of breakdown, devices are stressed with pulse widths of both 100 and 1000 ns. It is observed from Fig. 13 that breakdown voltage reduces with pulsewidth. Reduction in breakdown voltage with an increase in pulse widths points toward the thermal nature of device breakdown as has been discussed in Section III. These observations can be explained by the higher self-heating effect when the device is stressed with 1000-ns pulse. The increased self-heating effect also leads to detrapping of charge carriers from the existing trap states and leads to an observed increase in the leakage current with the stress voltage [Fig. 13(b)].

The influence of gate field on the ESD behavior of a-Si:H TFTs is explored by biasing the gate in different regions of transistor operation (Fig. 14). It is observed that with an increase in the gate bias, breakdown voltage increases in such a way that the gate–drain field at breakdown remains constant. Vertical field-induced dielectric breakdown explains the observed behavior.

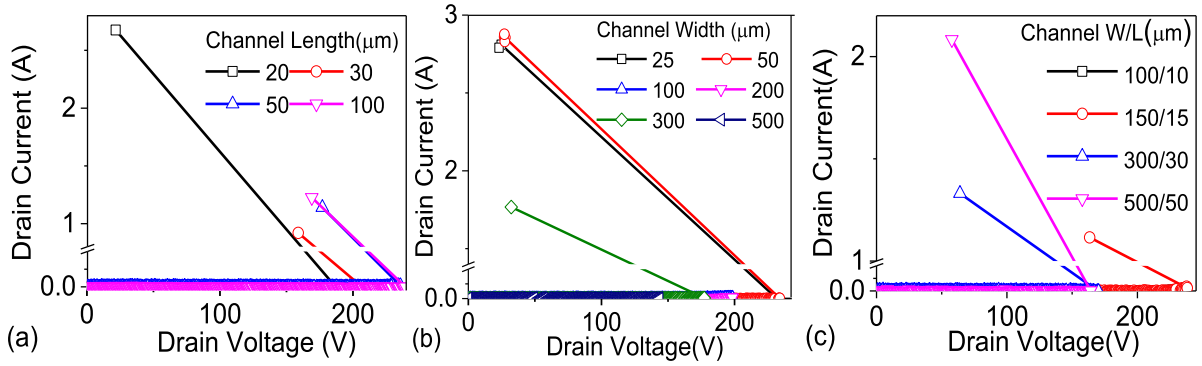

Fig. 11. TLP characteristics as a function of channel dimensions. (a) Variation in channel length. (b) Variation in channel width. (c) Variation in width/length ratio, while keeping the ratio constant. For smaller channel length, punchthrough dominates the breakdown/turn-on and failure, while for larger dimensions, dielectric breakdown dominates the catastrophic failure. For devices with constant width/length ratio, failure threshold did not follow a unique trend. For smaller widths, it improves with channel length; however, for larger widths, it lowers due to an increased probability of failure along the width.

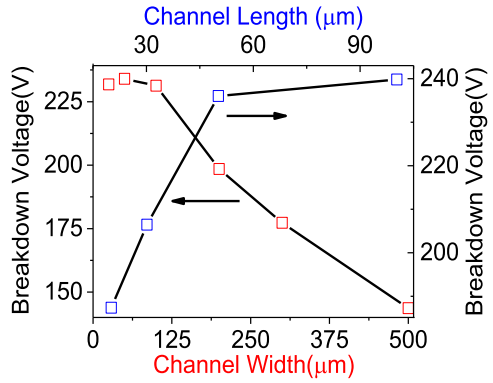

Fig. 12. Variation in breakdown voltage with channel length and width. Field assisted breakdown dominates at smaller dimensions and dielectric breakdown dominates at higher values.

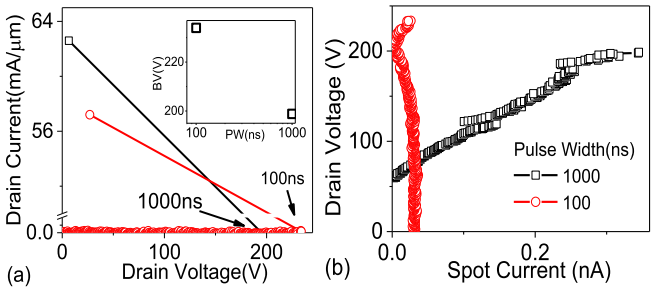

Fig. 13. (a) TLP *I*–*V* characteristics of devices stressed under varying pulse widths. Variation in breakdown voltage with pulse width (inset). (b) Spot current characteristics of devices at different pulsewidth conditions. Increased pulsewidth leads to an increase in detrapping of charge carriers leading to a continuous increase in the spot current.

To understand the impact of top passivation on the ESD reliability of a-Si:H devices, devices with and without passivation are tested. It can be observed from Fig. 15 that the presence of top passivation improves the robustness in these devices. Presence of a passivation layer leads to accumulation of charge carriers near the top a-Si:H-SiN_x interface. There is also a reduction in the concentration of dangling bonds at the top interface due to the presence of the passivation. This reduces the ON-resistance offered by the top interface and in grounded gate conditions, charge transport takes place through this path. Reduction in ON-resistance leads to an increase in the critical field required for the onset of avalanche assisted

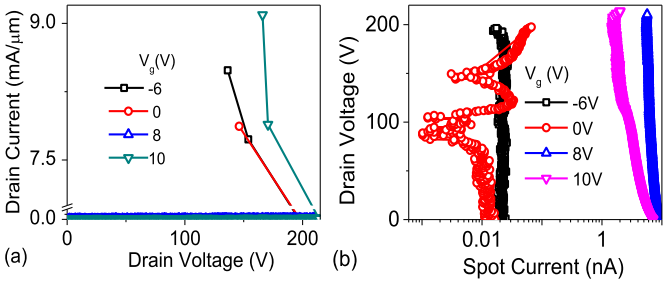

Fig. 14. (a) TLP characteristics. (b) Spot measurements of devices stressed with varying gate biases. With an increase in gate bias, breakdown voltage increases in such a way that G–D field at breakdown remains constant.

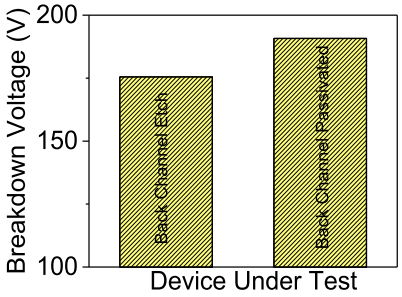

Fig. 15. Comparison of breakdown voltage for devices with and without a passivation layer. The presence of passivation reduces the device ON-resistance and improves breakdown voltage.

thermal failure and hence improves the ESD robustness of top passivated devices.

V. Gated Diodes, Drain Underlap Devices, and Thin-Film Resistors

To further explore the ESD reliability of a-Si:H devices, different types of devices including transistors with drain underlap, transistors connected in diode configuration (Gated diodes), and TFTs are tested under ESD conditions. Fig. 16 shows the cross section of a a-Si:H-based drain underlap devices and thin film resistors used in this paper.

Gated diodes are fabricated by shorting the drain and the gate contact and can play an important role in compensating the threshold voltage shift in a-Si:H-based applications [28], and thus, it is important to explore the ESD behavior of these devices. A similar exploration of ESD reliability of gated

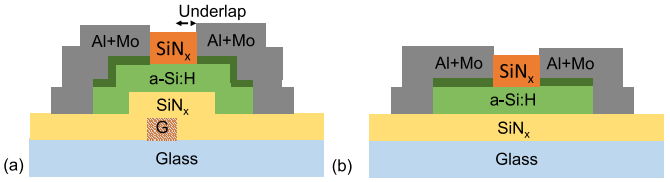

Fig. 16. Schematic cross section of (a) drain underlap devices and (b) thin-film resistors used in this paper.

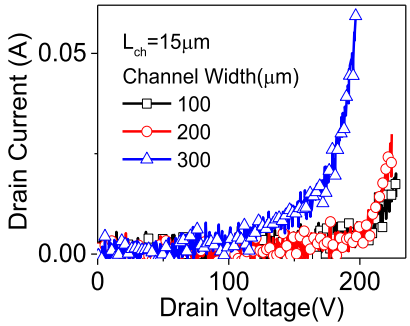

Fig. 17. TLP *I–V* characteristics of gated diodes with varying channel widths. Variation in breakdown parameters (I_{t2} and breakdown voltage) with channel widths point toward field driven phenomenon. Gated diodes offer a lower ON-resistance compared to conventional TFTs.

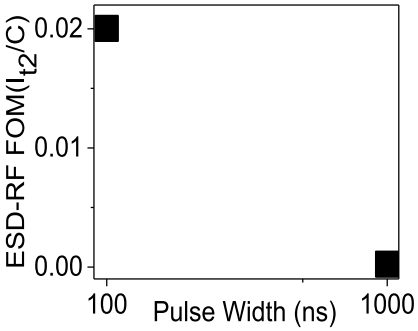

Fig. 18. ESD-RF FOM of a-Si:H-based gated diodes. FOM at 100-ns condition is approximately 0.02 and reduces with stress width.

diodes in CMOS technology is already present [29], [30] Fig. 17 shows the TLP *I–V* characteristics of gated diodes with varying channel widths. It can be observed from Fig. 17 that the gated diodes have a much higher TLP current as compared to conventional TFTs due to the application of a higher gate bias. Application of high gate bias leads to a higher concentration of the carriers aiding avalanche assisted breakdown, leading to the observed behavior. It is also observed that devices with higher channel widths have a higher failure current (I_{t2}), on account of their lower ON-resistance. To further explore the behavior of gated diodes under ESD stress conditions, ESD-RF figure of merit (FOM) (I_{t2}/C), where C is the device accumulation capacitance, is computed for devices stressed under varying stress widths. This FOM gives quantitative information about the switching speed of gated diodes and their ESD robustness and is used to quantify the performance in CMOS technology [29]. Fig. 18 shows the variation in ESD-RF FOM with stress width. With an increase in stress widths, the devices offer a lower I_{t2}, and hence, a reduction in ESD-RF FOM is observed.

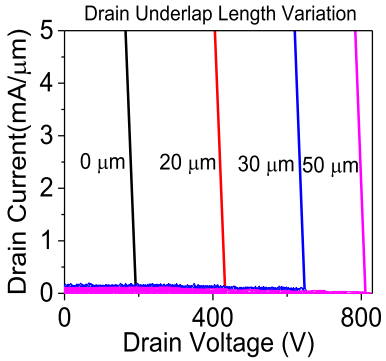

Fig. 19. TLP *I–V* characteristics of various drain underlap device structures with constant channel length. The device current is normalized with device width. Drain underlap devices provide high ESD robustness and can be used as I/O protection devices in a-Si:H technology.

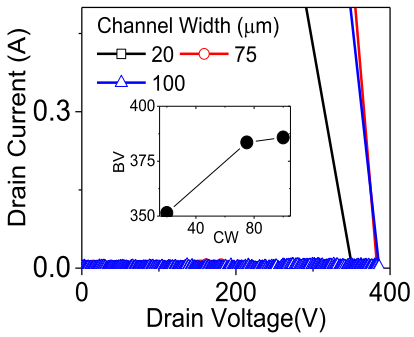

Fig. 20. TLP *I–V* characteristics of a-Si:H resistors. Breakdown voltage versus channel width (inset). Resistors fail due to avalanche breakdown occurring in the channel region. Breakdown voltage also increases up to a critical channel width and then saturates.

Drain underlap devices are TFTs with an underlap region with no gate control. Fig. 19 shows the TLP *I–V* characteristics of drain underlap devices. These devices offer a higher ESD robustness compared to conventional TFTs on account of electric field relaxation offered by drain underlap region, leading to a reduction in net electric field at drain edge and thus improving ESD robustness. As the drain underlap length increases, the electric field at the drain edge reduces and devices have a higher ESD robustness. a-Si:H TFTs play an important role in a-Si:H technology and have been used in various applications including electronic copying [31]. Fig. 20 shows the TLP *I–V* characteristics of a-Si:H-based resistors with different channel widths. Due to the absence of gate contact, a-Si:H TFTs do not experience any band bending at the semiconductor-insulator interface, which results in lower carrier concentration at the interface compared to that in TFTs. As a consequence of lower interface concentration, field-induced breakdown has a smaller role compared to thermal breakdown in these devices. Increase in channel width reduces the ON-resistance and hence improves ESD robustness. It is also observed from Fig. 20 that as channel width increases beyond a threshold, breakdown voltage does not scale with channel width. This can be attributed to the fact that as channel width reaches the threshold, ON-resistance reduction saturates and in this condition, field-induced breakdown dominates the failure phenomenon and the breakdown voltage scales with channel dimensions in accordance with this mechanism.

VI. Conclusion

In this paper, we have presented the detailed physical insights into the ESD behavior of a-Si:H TFTs. Two regions of operation are observed in the TLP characteristics: 1) sub-threshold conduction and 2) device failure. It is observed that device degradation starts at about voltage stress level of 60 V. Pre-breakdown analysis revelaed that charge injection into the gate dielectric dominates the behavior at lower stress voltages, while at higher stress voltages, interface trap generation dominates. It is also studied that defect states generation process is assisted by self-heating occurring in the device at higher stress durations. It is also observed that as electrons are accumulated in the channel region, electron scattering also plays an important part in the device behavior. Degradation recovery at the drain side is observed due to spatially variant interface trap generation although a similar observation is not made for the source side. Using Raman spectroscopy, it is also found that there are no material changes in the device with stress. It is found that device failure occurs due to localized avalanche assisted thermal breakdown through hotspot formation. Contact melting at breakdown is observed in post failure SEM micrograph. Raman spectroscopy results also revealed post failure crystallization taking place at the damaged area. Study of breakdown voltage with stress duration also pointed toward thermal behavior. Impact of channel dimensions on breakdown mechanism is studied and it is observed that devices with relatively smaller dimensions undergo avalanche assisted thermal breakdown, while devices with relatively larger dimensions experience dielectric breakdown. ESD behavior of gated diodes, resistors, and drain underlap structures are investigated in detail. Gated diodes are observed to offer a significantly higher failure current with a lower failure voltage due to the presence of a larger number of channel electrons which aid avalanche breakdown. Technologically relevant parameters like ESD-RF FOM are also studied for gated diodes. It is observed that drain underlap devices provide a much higher ESD robustness as compared to conventional TFT structure since drain underlap provides an electric field relaxation on account of the presence of lesser charge carriers in the underlap region. ESD behavior of TFTs based on a-Si:H is also investigated and it is found that breakdown takes place due to competing thermal- and field-induced breakdown mechanism.

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