First Observations on the Trap-Induced Avalanche Instability and Safe Operating Area Concerns in AlGaN/GaN HEMTs

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***Abstract*— This paper reports the very first systematic study on the physics of avalanche instability and safe operating area (SOA) reliability in AlGaN/GaN high-electron-mobility transistor (HEMT) using submicroseconds pulse characterization, poststress degradation analysis, well-calibrated TCAD simulations, and failure analysis by scanning electron microscopy (SEM) and transmission electron microscopy (TEM). Impacts of electrical and thermal effects on SOA boundary and avalanche instability are investigated. Trap-induced cumulative nature of degradation is studied in detail. The root cause for avalanche instability in AlGaN/GaN HEMTs is investigated. Postfailure SEM, energy dispersive X-ray (EDX), and TEM analysis reveal distinct failure modes in the presence and absence of carrier trapping.**

***Index Terms*— Avalanche instability, failure modes, Gallium nitride (GaN), high-electron-mobility transistor (HEMT), safe operating area (SOA), trapping.**

I. Introduction

ATTRIBUTED to its attractive properties, such as wide bandgap (3.4 eV), high breakdown field (3.3 MV/cm), and low dielectric constant (9), Gallium nitride (GaN) is projected as promising substitute of Si for power device technology. Moreover, high 2DEG density (10^{13} cm^{-2}), high electron peak velocity (2.5×10^7 cm/s), and high electron saturation velocity (1.5×10^7 cm/s) offered by AlGaN/GaN hetero-junction over Si substrate make it promising candidate for high-power and high-frequency applications with much higher performance/cost ratio than its SiC and Diamond-based counterparts. Despite the interesting material attributes and outstanding performance, the lifetime of these devices is limited by various reliability phenomena. Also, the available GaN reliability standards are broadly based on the Si laterally diffused metal oxide semiconductor transistor failure models, which do not often imply to GaN-based devices [1]. Hence, despite commercialization, the reliability of GaN technology is still the major hurdle to its widespread adoption and is a topic of the intense research.

Long-term reliability of these devices has been greatly studied in the literature; however, discussion on the ability of GaN high-electron-mobility transistor (HEMT) to handle high power under extreme conditions and related safe operating area (SOA) concerns are largely missing in the literature [2], [3]. A broader SOA offers robustness against load impedance variations in RF power amplifiers and ensures safe switching margin under high-voltage and high-current injection/short circuit conditions in power circuits and circuit breakers. SOA boundary in GaN HEMT is limited by various failure mechanisms which need thorough investigation. Importance of this paper lies in the fact that SOA reliability and avalanche instability are still considered to be a serious research subject for Si or SiC power MOSFETs [4], AlGaN/GaN HEMT is certainly not an outlier. Therefore, it would not be an exaggeration to say that the SOA specifications given in a GaN HEMT datasheet are insufficient to predict the device reliability under practical stress scenarios [5]. Despite the severity of this topic, very little attention has been paid to it in the literature. Few studies report time-dependent OFF-state failure [6], [7]. Another study points to nonthermal nature of ON-state failure [2]. Keeping in mind the scattered observations and very limited discussion on SOA reliability, this paper is a first systematic study of the physics of avalanche instability and SOA concerns in AlGaN/GaN HEMT.

In this paper, which is an extension of our earlier study [8], a comprehensive study is carried out with pulse electrical characterization, under conditions that are more frequently encountered in practical applications. Variation in SOA is recorded under different stress conditions. Device parameters are monitored on-the-fly during stress to capture the evolution of degradation. TCAD simulation is performed to understand the phenomena, which limit the SOA boundary in AlGaN/GaN HEMT. Postfailure analysis of the damaged device regions are done using scanning electron

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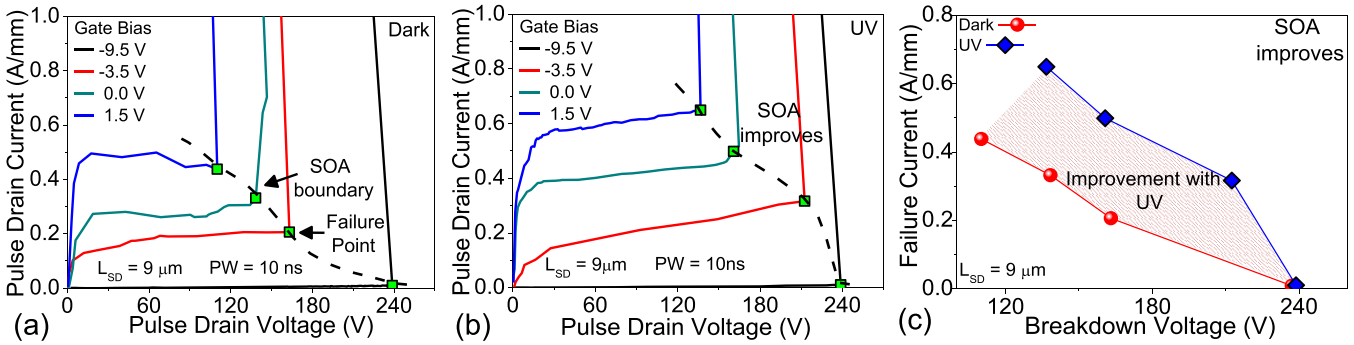

Fig. 1. Pulse *I–V* characteristics of HEMT (a) under dark condition and (b) with UV exposure. Failure point shown here marks the SOA boundary. (c) Variation in SOA boundary of HEMT stressed under dark and UV condition. As evident, SOA boundary of device widens under UV light.

microscopy (SEM), energy dispersive X-ray (EDX), and transmission electron microscopy (TEM) to gain physical insight into the underlying failure mechanism(s). This paper is organized as follows. The details about device fabrication and characterization setup are presented in Section II. Results showing the effect of carrier trapping on SOA boundary and power-to-fail are presented in Section III. Trap-induced HEMT degradation is discussed in Section IV. Physics of SOA failure and avalanche instability is presented in Section V. Results from postfailure analysis of devices are discussed in Section VI. Finally, the key findings and conclusive remarks are drawn in Section VII.

II. Device Fabrication and Characterization

The devices analyzed in this work are normally-ON HEMTs that are fabricated on a AlGaN/GaN layer stack grown on 2-in Si (111) wafer using metal–organic chemical vapor deposition (MOCVD). The stack growth begins with 400-nm AlN nucleation layer followed by 1-μm-thick linearly graded transition region (250 nm $Al_{0.75}Ga_{0.25}N$/250 nm $Al_{0.50}Ga_{0.50}N$/500 nm $Al_{0.25}Ga_{0.75}N$) and 750-nm undoped GaN buffer. Undoped 25-nm $Al_{0.25}Ga_{0.75}N$ donor layer is grown with 1-nm-thin AlN barrier. The material stack is finally capped with 3-nm GaN cap. 100-μm wide devices with 2-μm source-to-gate distance, 3-μm gate length, are processed using UV lithography for different source-to-drain spacings (L_{SD}). Devices are MESA isolated on wafer, using Chlorine chemistry by inductively coupled plasma reactive ion etching. Ti/Al/Ni/Au metal stack is deposited using E-beam evaporation to realize source/drain contacts that are later annealed at ~850 °C to make the Ohmic contact with 2DEG. Finally, Ni/Au Schottky gate is deposited, followed with ~400 °C soft anneal. Passivation was intentionally avoided in few devices to study the impact of surface traps. Submicroseconds pulse *I–V* characterization of devices is performed to determine the SOA boundary and failure threshold using rectangular pulses of different pulse widths (PWs) and fixed rise time (1 ns). The drain is pulsed at different gate biases and drain voltage and current waveforms are captured using a digital storage oscilloscope at 25-Gps sampling rate. Recorded waveforms are averaged over 60% to 90% window of PW to generate a family of *I–V* characteristics of the device under test. To monitor degradation and study the failure evolution, the linear drain-to-source current is spot measured at 50-mV dc drain bias, after every voltage pulse. To study the influence of bulk and/or surface traps on device behavior, the measurements are done both in the presence and absence of a subbandgap UV (365 nm) exposure. Three devices are tested in each case to check the repeatability in observations.

III. SOA Boundary and Carrier Trapping

A device (L_{SD} 9 μm) is tested at 10-ns PW, under dark and in UV light condition. Corresponding pulse *I–V* characteristics are shown in Fig. 1. As shown in the figure, the device breakdown is marked with an abrupt increase in pulse drain current at the failure point. The locus of the failure point over the entire family of curves marks the SOA boundary of the device. A comparison of *I–V* characteristics obtained under dark and UV, shown in Fig. 1 unveils the following: 1) early saturation in drain current and 2) early device failure when tested under dark. As a result, the SOA shrinks under dark condition. When the experiment is repeated under UV light, no current collapse is shown and the drain current exhibits quasi-saturation behavior as depicted in Fig. 1(b). The device fails at higher voltage and current, exhibiting broader SOA. Fig. 1(c) shows the comparison of the SOA boundary of a device extracted under dark and UV. As evident, SOA boundary widens under UV light. Under normal device operation, excessive carrier trapping in gate–drain region causes drain current collapse [9]. Trapping underneath the gate can alter threshold voltage [7], while trapping at AlGaN/GaN interface [10] and in buffer increases R_{ON} [11]. Trap-induced effects degrade device performance, and carrier trapping further increases after degradation [10]. This positive feedback loop continues until the device sees catastrophic breakdown, which is discussed in the next section. The exposure of subbandgap UV light potentially detraps carriers from shallow and deep defect levels present in different regions of the device. Therefore, UV light suppresses trap-induced degradation in the device and improves device SOA. To summarize, the SOA boundary of GaN HEMT is limited under normal operating condition and it gets recovered with subbandgap UV exposure.

SOA boundary of a device is determined by the maximum power handling capability of the device for a given stress

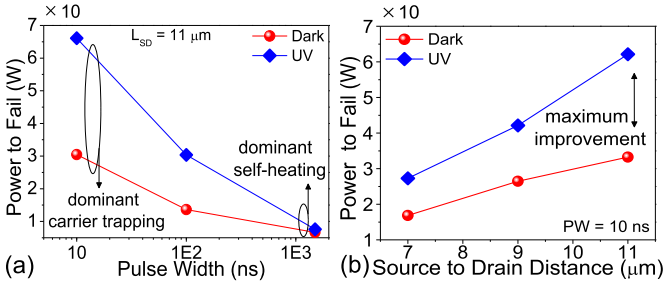

Fig. 2. (a) Power to fail as a function of PW extracted under dark and UV condition. While exhibiting power law behavior presence of UV improves power to fail at shorter pulses. (b) Power to fail as a function of source–drain spacing. It increases linearly with L_{SD} and shifts upward with UV exposure.

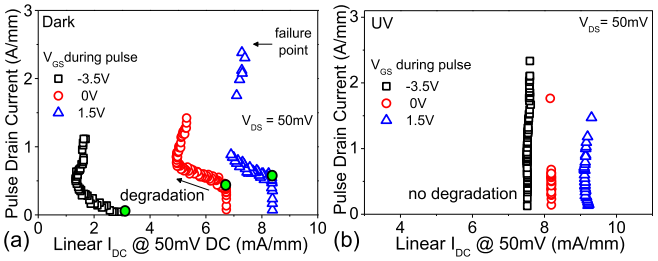

Fig. 3. (a) Linear drain-to-source current measured after each stress pulse of 100-ns duration applied at drain of a device of L_{SD} 7 μm under (a) dark and (b) UV condition. Unique current degradation trend can be observed under dark condition at different gate biases, which is absent under UV illumination.

time, before permanent failure. Here, power-to-fail (P_{FAIL}) is defined as; $P_{FAIL} = I_{FAIL} \times V_{BD}$, where I_{FAIL} is the failure current and V_{BD} is the breakdown voltage. The study is done to understand, how the failure threshold of GaN HEMT changes with stress conditions and device design parameters. A device is stressed at different PWs and P_{FAIL} is measured in each case under dark and UV exposure. Fig. 2(a) shows the variations in P_{FAIL} recorded under different PWs. P_{FAIL} is observed to decrease consistently with an increase in stress time or PW, exhibiting a power law like behavior, both under dark and UV exposure condition. It is worth highlighting that at lower PW (10 ns), P_{FAIL} shows 2× improvement in the presence of UV due to dominant carrier detrapping from barrier and buffer regions, with minimal self-heating. However, the improvement obtained with UV, gradually falls with an increase in PW. Ultimately, at 1000-ns PW, UV exposure shows no change, consequently P_{FAIL} under dark and UV remains the same. Possibly, at higher PW, the thermal effects originating from self-heating are dominant, which overshadow any contribution from trapping/detrapping as discussed above. This is verified from the postfailure analysis of the devices that show the signature of thermal failure at higher PW as discussed in Section IV. Next, devices of different L_{SD} are tested at the same PW. Fig. 2(b) shows the variations recorded in P_{FAIL} with L_{SD}. Linear scaling of P_{FAIL} with L_{SD} is observed. Large L_{SD} has two complementary effects. On the one hand, the effective channel field, for a given drain voltage, reduces at larger L_{SD}, which suppresses the field-driven degradation phenomena such as trapping and inverse piezoelectric effects. On the other hand, larger L_{SD} offers an increased number of defect states across the larger gate-to-drain region, which increases the number of free electrons captured by the trap states resulting a steeper device degradation. This is verified by the fact that under UV light, the maximum improvement in P_{FAIL} is noted in device with largest L_{SD} (11 μm), which is due to the maximum detrapping under UV exposure.

IV. Trap-Induced Degradation

A. Evolution of Device Degradation

The evolution of the degradation in the device is studied by regularly monitoring device's dc behavior in between pulse stresses. In the present study, the linear drain-to-source dc current (I_{dc}) is measured on-the-fly after each voltage pulse applied at drain (V_P). Fig. 3(a) shows the degradation trend in I_{dc} observed under dark condition for different gate biases. It shows that at negative gate voltage (here −3.5 V), when the device is under pinched-off condition, device degradation initiates (as marked by green dot) at lower stress voltages/currents. On the other hand, at under ON-state ($V_{GS} = 0$ and 1.5 V), the onset of device degradation (as marked by green dot) was pushed to higher voltages/currents. This shows the requirement of a critical field in gate–drain region for the device to degrade. With increasing drain stress voltage, the electric field in gate–drain region increases which enhances electron injection from gate to surface and channel to GaN buffer. This reduces 2DEG density to obey vertical charge neutrality and results in a drop in drain current. It should be noted that SOA measurements demands application of ultrahigh voltage, short duration (sub-200 ns) pulses between drain–source terminals of GaN HEMT, under ON-and OFF-states, which would eventually lead to HEMT's failure. At these high voltages, the device would lead to excess hot electron generation via impact ionization (II), which rapidly increases the drain-to-source current beyond typical HEMT's drain current (∼1 A/mm). Since the stress pulse duration is in the sub-200-ns range, the electron-phonon scattering due to self-heating or increased phonon population, which can lower the carrier energy and bring the current back to the nominal range (∼1 A/mm) is largely missing. This behavior explains very high drain current shown in Figs. 3 and 11, which are extracted using pulses applied for 100 ns or lower. Moreover, the excess carrier holes generated from II can potentially deteriorate the gate control, as discussed in the subsequent sections. Furthermore, under ON-state with increased drain voltage, the hot electron density in channel increases. Hot electrons activate traps at AlGaN/GaN interface [12] and further deteriorates I_{dc}. When the same experiment was performed under UV condition, no degradation in device's dc behavior was observed, independent of gate voltage, as depicted in Fig. 3(b). This hints the role of trap states in device degradation. It is worth highlighting, before explaining these trends further, that UV irradiation is expected to detrap all the captured electrons from the deep acceptor trap levels. It is to be noted that a delay of 200 ms is introduced between two consecutive pulses. However, the slow detrapping from deep levels can take several seconds to hours for recovery. In the present case, as I_{dc} degrades monotonically under the dark condition with each pulse, it can be concluded

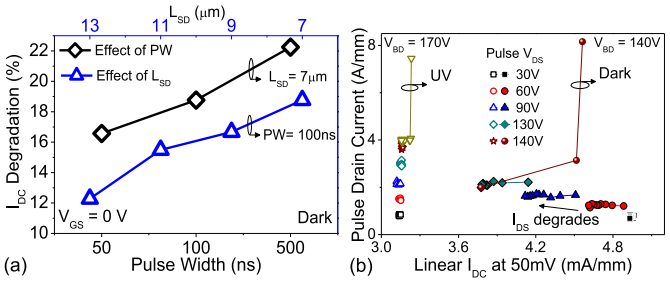

Fig. 4. (a) Degradation in linear drain current measured under dark condition as a function of PW and source-to-drain spacing. (b) Cumulative degradation extracted by applying set of ten constant voltage pulses at drain before increasing its amplitude. A cumulative degradation is visible under dark condition, which is missing in the presence of UV light.

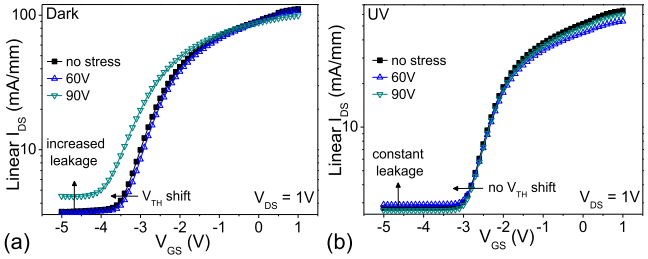

Fig. 5. (a) DC transfer characteristics measured after stressing device using a set of ten pulses under dark and (b) UV conditions. In dark condition, device's OFF-state leakage increases and threshold voltage changes, which is absent in the presence of UV exposure.

that most of the filled traps have detrapping time constant greater than >200 ms.

The degradation trends discussed above can be explained as follows: at higher drain stress, hot electrons in channel generate new defects and get trapped at the surface, in barrier and buffer regions. This is responsible for the degradation in device performance. With UV exposure, carrier detrapping gets enhanced which assists in suppressing the trap originated device degradation. Stress experiments done at different PWs show that degradation increases linearly with PW, due to longer stress time available for carrier trapping. Furthermore, percentage degradation is extracted for devices with different source-to-drain spacings which are tested under the same pulse condition (100 ns). Percentage degradation is found to decrease linearly with L_{SD}, as shown in Fig. 4(a), which is attributed to the reduced channel field at larger L_{SD}.

B. Cumulative Nature of Degradation

As discussed above, device degrades with each pulse due to slow detrapping of the carrier. To confirm this, the following measurements are performed. A HEMT device is stressed under the dark condition with a set of ten consecutive pulses of 100-ns each, of the same amplitude applied at drain, while keeping gate biased at 1.5 V. Then, the pulse amplitude is increased to higher voltage level in subsequent set. I_{dc} is measured after each pulse. Here, for a fixed stress amplitude, the degradation in I_{dc} is noted with an increase in a number of stress pulses as shown in Fig. 4(b). For example, when ten pulses of 90 V are applied, I_{dc} degrades with each pulse as depicted in Fig. 4(b). The same trend continues further at higher pulse voltages. At 140 V, the device faces immediate failure after application of the first three pulses. This paper reveals that degradation in AlGaN/GaN HEMT is cumulative in nature. Therefore, repetitive stressing can trigger device failure at voltage much below the dc breakdown voltage. The cumulative nature of degradation is attributed to local charge accumulation due to slow detrapping. This argument is supported by missing degradation after each pulse under UV exposure, as depicted in Fig. 4(b). Here, UV exposure assists in carrier detrapping and the device experiences abrupt failure at 170 V without accumulative prebreakdown degradation.

C. Traps States and Associated e-Field Modulation

DC I–V characterization of devices-under-stress is performed at regular intervals during the test to record the changes in device's characteristics and parameters such as V_{TH}, drain–source leakage, R_{ON}, and I_{SAT}. Fig. 5 shows the dc transfer characteristic of a device stressed using 100-ns wide pulses, under dark and UV conditions. As depicted in Fig. 5(a), stress under dark introduces: 1) V_{TH} shift and 2) increases drain–source leakage. Observed negative shift in V_{TH} reveals positive charge accumulation underneath gate [6] and modified Schottky barrier height due to the increased interface defects [13] with stress. The increased OFF-state leakage results from: 1) reduced V_{TH} [7]; 2) increased buffer leakage [14]; and 3) degraded gate–drain Schottky diode [15]. This degradation can be explained using electron trapping in acceptor states present in GaN buffer, as the same was found to recover with UV light as shown in Fig. 5(b), where the transfer characteristic remain unchanged with stress. To validate this argument, TCAD simulations were performed using setup explain in our earlier works [16]–[18]. Here, donor-type surface trap ($E_C - 0.6$ eV) is considered uniformly distributed over the GaN cap surface. Acceptor-type buffer traps ($E_C - 2.1$ eV) are included with Gaussian distribution with peak density at AlGaN/AlN interface. Fig. 6(a) and (b) shows the redistribution of e-field as the acceptor trap concentration is increased. Electric field both at the surface and the channel was found to shift toward the drain edge when buffer trap concentration was increased. This shift in peak field from gate-to-drain edge enhances II at drain end and causes early device breakdown as discussed next.

Fig. 7 shows the simulated electrostatic potential, extracted at $V_{DS} = 60$ V and $V_{GS} = -6$ V, for (a) high buffer trap concentration (10^{18} cm^{-3}), which is equivalent to condition under dark and (a) low buffer trap concentration (10^{15} cm^{-3}), which is the plausible case under UV exposure since exposure to UV light will detraps the carrier and the trap state will turn neutral. Under dark condition, the field localizes near drain contact, which was found to spread across the entire gate–drain access region in the other case. This is explained as follows: acceptor states when occupied carry a negative charge. During device operation under dark, maximum carrier trapping takes place in the gate–drain region, in the presence of high lateral field. This leads to negative charge accumulation in gate–drain region. In the presence of high density of negative

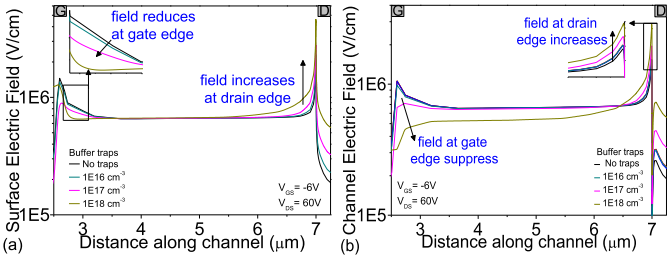

Fig. 6. Simulated electric field profile along the HEMT (a) surface and (b) channel, extracted between gate and drain regions for different buffer trap concentrations.

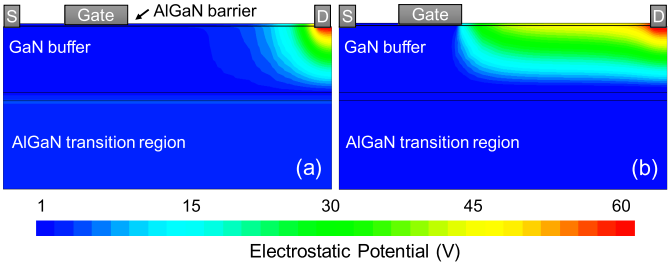

Fig. 7. Electrostatic potential distribution in gate–drain region simulated for (a) high buffer trap density (10^{18} cm^{-3}) and (b) low buffer trap density (10^{15} cm^{-3}) in GaN buffer, extracted at V_{DS} = 60 V and V_{GS} = −6 V.

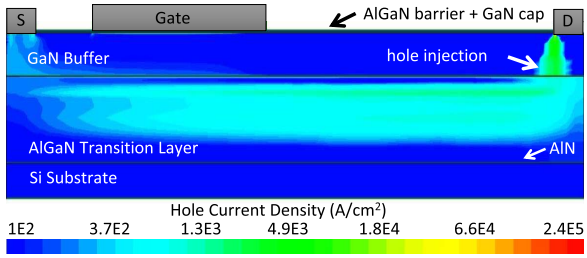

Fig. 8. TCAD contour depicting hole distribution in the device at OFF-state breakdown. Excess holes generated near drain inject into buffer and form parasitic S/D short path in buffer.

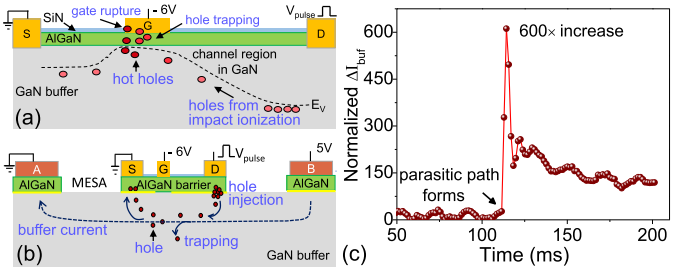

Fig. 9. (a) Device schematic presenting the device failure mechanism under dark condition. Here, GaN cap is not shown for simplicity. (b) Test structure with HEMT device and Ohmic probe contacts (A, B), used to monitor variation in buffer current during OFF-state stress. (c) Change in buffer current measured using test structure in (b) during the OFF-state stress.

charge, crowding of equipotential lines intensify under drain contact [Fig. 7(a)], which enhances e-field near drain (Fig. 6). On the other hand, exposure to UV assists in carrier detrapping and reduces the ionized acceptor trap density and its associated negative charge, in the gate–drain region. This allows the potential to spread in gate–drain region [Fig. 7(b)], which relaxes field crowding at drain end and, consequently, improves breakdown voltage of the device under UV exposure.

V. SOA Failure and Physical Insights

A. Failure Under Dark: Trap Assisted Filamentation

TCAD simulations reveal field distribution in device changes with an increase in trap concentration at surface and in buffer. It reveals a lateral shift in peak electric field from gate-to-drain edge, at high buffer trap density. Uren *et al.* [19] reported a similar field shift in HEMT with C-doped buffer at higher voltages. Field enhancement at drain increases II and electron–hole pair generation at drain end. The excess electrons are collected by the drain while holes follow two routes: 1) a fraction of holes gets accelerated toward source via channel, under channel field influence and accumulate under the gate due to favorable electrostatics [3] as illustrated in Fig. 9(a). Hot holes can also leak from channel to gate under negative gate bias and on the way get trapped underneath gate causing negative Vth shift as shown Fig. 5(a). This deteriorates gate control and increases source-to-drain leakage as reported previously in [6], [7] and 2) the excess holes at drain, also inject into the buffer and are collected by source constituting source–drain leakage via buffer. Injected holes can also get trapped in deep levels at various locations in buffer and transition region. Slow detrapping from such deep levels accumulates trapped charge with time and enhances the local electric field. Eventually, it triggers avalanche [20] forming a highly conducting narrow parasitic hole path or filament as shown in Fig. 8. To experimentally verify the explanation, two Ohmic contacts (marked A, B) are realized on either side of a HEMT device, as shown in Fig. 9(b). Contact-A and B are isolated by a 200-nm-deep MESA isolation on either side of main HEMT so that only buffer current flows through them. While stressing the main HEMT, the buffer current between contact-A and B is monitored over the time. The buffer current abruptly increases by 600 times on the verge of failure, as shown in Fig. 9(c) which marks the formation of filament (Fig. 8) and causes permanent device failure. Postfailure analysis, which is discussed in the next section, corroborates well with the TCAD-based findings.

B. Failure Under UV Exposure: Hotspot Formation

It is clear that high trap density in GaN HEMT favors filament formation and causes lateral breakdown in these devices. At this stage, one may be curious to understand the breakdown mechanism in the absence of carrier trapping or at low defect density. In experiments, we have shown earlier that the absence of carrier trapping can be emulated by using UV exposure. To study the corresponding failure physics, the HEMT structure is simulated without taking the surface and buffer traps into consideration. Note, in TCAD, as surface charge cannot be set to zero since it is essential to realize 2DEG. Therefore, to suppress the effect of surface states, the device is considered passivated with SiN. The simulation shows that in the absence of traps, the electric field peaks

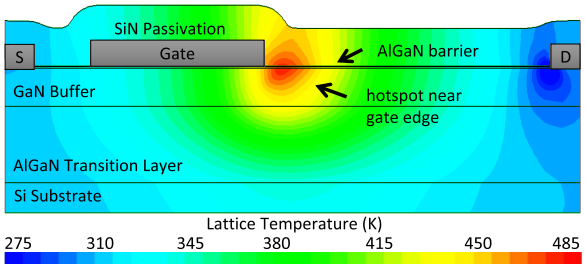

Fig. 10. TCAD contour depicting temperature distribution across the device at device breakdown. Hotspot can be seen near drain side gate edge.

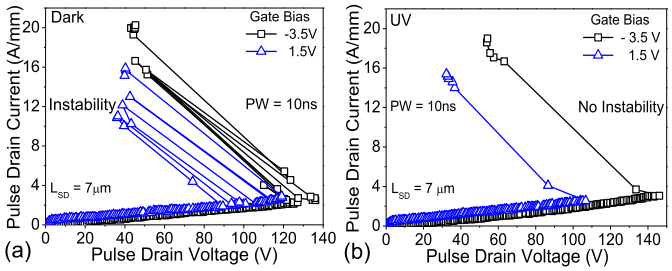

Fig. 11. (a) Snapback instability observed in *I–V* characteristics extracted under dark conditions using 10-ns-wide PW. (b) Snapback instability absent in the presence of UV exposure.

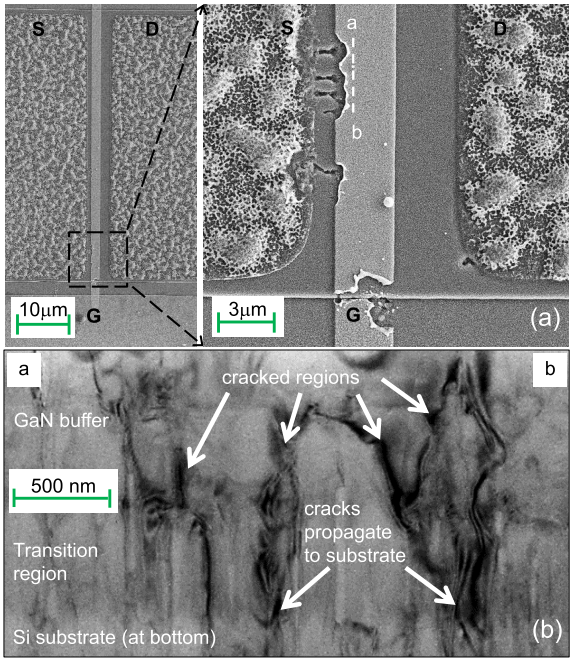

Fig. 12. (a) Postfailure SEM image of a device which failed under dark condition, when stressed using 10-ns wide pulses under OFF-state. It shows multiple damage sites in S-G region. (b) TEM cross-sectional taken along line "a-b" depicts cracks running deep into the buffer and transition regions.

at gate edge toward drain. At high drain voltage, enhanced current density (J) and peak electric field (E) at gate edge forms a hotspot (J.E) as depicted from temperature distribution shown across the device in Fig. 10, extracted at breakdown. Failure analysis presented in the later sections for a device which failed under UV, reveals damage at the gate edge, which corroborates well with the failure physics investigated using TCAD simulations.

C. Trap-Induced Avalanche Instability

When devices are stressed using shorter pulses (PW = 10 ns), an unstable snapback region is observed in the *I–V* characteristics beyond the breakdown point, under dark condition. That is, each time the device enters the snapback mode, which is a state before filamentary failure, it recovers back repeatedly, as depicted in Fig. 11(a). However, when the same test is repeated under UV light, the instability vanishes and the device sees clear failure, at higher voltage, as shown in Fig. 11(b). This hints that the observed instability is related to carrier trapping, which is explained as follows: across the wafer and, hence, along the device width, there is always a finite variation in defect density and spatial stress distribution, originating from the MOCVD growth of GaN/AlGaN. Due to this, trap generation and carrier trapping occur nonuniformly across the device width. This leads to the formation of localized regions, where carrier trapping is higher compared to the rest of the device's active region. Such regions with high trap density, in turn, experience an early shift in electric field peak toward drain, as shown in Fig. 6. This results in the formation of the localized parasitic path(s) as shown in Fig. 8. These localized parasitic paths lead to the formation of multiple current filaments along the device width. Beside failure analysis results discussed in the next session, the avalanche instability due to filament formation can be validated from pulse-to-pulse instability observed in Fig. 11(a), when measured under dark condition. In this case, the device forms a filament, however; it survives failure due to the short duration of applied stress. As a result, the device tries to enter into snapback state multiple times, before experiencing a localized thermal failure at higher currents. However, the same instability is absent under UV exposure as shown in Fig. 11(b). This confirms the role of traps in inducing avalanche instability in AlGaN/GaN HEMT.

VI. Failure Analysis

After pulse characterization, failure analysis of the damaged device regions is done to gain physical insight into the underlying failure mechanism(s). This section reveals, using SEM, EDX and TEM analysis, that under dark condition failure occurs in the gate–source region, while with UV exposure device fails in gate–drain region. This is elaborated in the following.

A. Failure Under Dark Condition

Fig. 12(a) show the SEM image of a device which failed under dark condition in OFF-state. It reveals failure spots in the gate–source region. This is attributed to the accumulation of excess holes under the gate, which are generated from the enhanced II at drain due to trap-induced peak electric field shift as shown in Fig. 6. TEM cross section taken along the

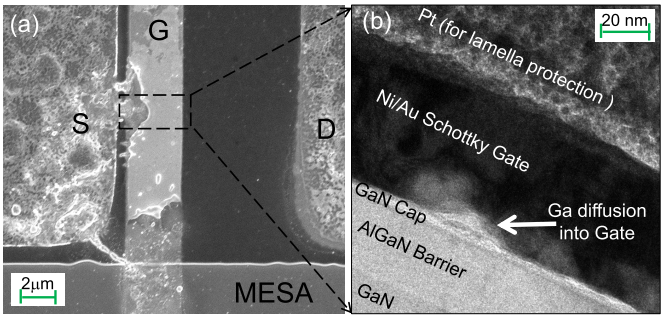

Fig. 13. (a) SEM image of HEMT with 11 μm L_{SD}, which failed under dark condition when stressed with 10-ns-wide pulses under ON-state. (b) Cross-sectional TEM taken in the dotted area of the damaged S-G region reveals Gallium out diffusion from GaN cap into Ni/Au Schottky gate.

damaged location in Fig. 12(a) unveils that the cracked source–gate region runs deep into the buffer and reaches the transition region as clear from Fig. 12(b). This possibly results from the thermal stress generated due to the heavy current flow via localized parasitic conductive paths formed in buffer/transition region at breakdown, as learned from the TCAD study (Fig. 8) earlier. This observation corroborates well with the avalanche injection and filamentation theory presented in the previous section. Device failure under dark condition, stressed under ON-state condition, reveals gate–source failure with gate metal getting melted as shown in Fig. 13(a). The holes that are collected under the gate leak through the Schottky junction and increases the gate–source leakage [6]. Moreover, interface defects at Schottky gate increase under this stress [13]. Therefore, gate wears out/melts at the source side as clear from SEM image in Fig. 13(a). EDX analysis at damage location shows 9% Au which melted from gate region, as confirmed from SEM micrograph. Cross-sectional TEM of the dotted area from damaged source–gate region reveals Gallium out diffusion from GaN cap into Ni/Au Schottky gate. This is possibly due to the localized heating associated with high gate–source leakage.

B. Failure Under UV Condition

Postfailure SEM micrograph of devices which failed under UV condition in OFF-state is shown in Fig. 14(a). As clearly shown, pits originate at multiple locations along the gate edge toward drain. In devices as presented above, in the absence of traps, i.e., in the presence of UV light, the peak electric field lies at gate edge toward drain. The enhanced normal component of the peak field introduces mechanical strain at gate edge due to inverse piezoelectric field [21]. When the stored elastic energy hits a critical value, the mechanical stress relaxes by the formation of crystallographic defects/pits. Fig. 14(b) shows the SEM image of the device which failed while stressing device using 100-ns-wide pulse under UV exposure in ON-state condition. It reveals the signature of hotspots formed along the gate edge toward drain. As predicted from the TCAD study, in a device without traps, the electric field peak lies at drain side gate edge as shown in Fig. 6. This leads to the formation of hotspot at the gate edge toward drain as shown in Fig. 10, which can be distributed along the

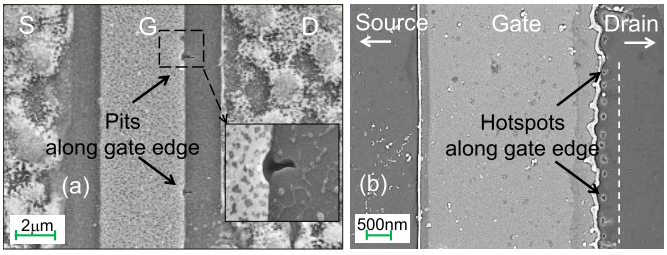

Fig. 14. (a) SEM image of HEMT which failed at 100 ns under UV light in OFF-state condition. Pits get formed at multiple locations along the gate edge toward drain. (b) SEM image of HEMT with 7 μm L_{SD} which failed at 100 ns under UV condition in ON-state. Images reveals continuously distributed hotspots along the gate edge toward drain. Gate metal folds up at hotspot locations. No damage is observed at source side.

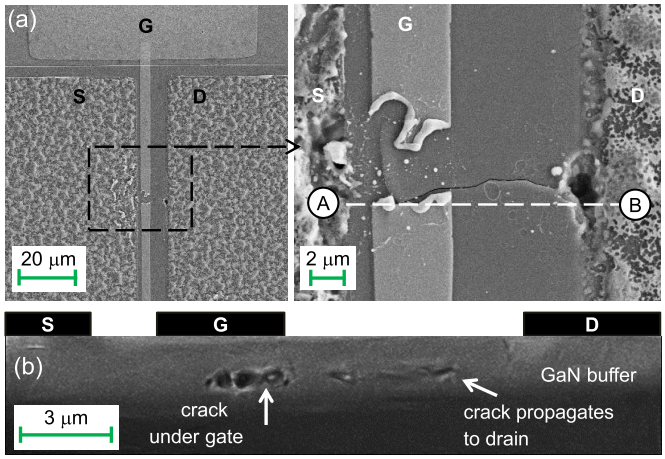

Fig. 15. (a) SEM image of HEMT failed under UV condition, stressed using 10-ns wide pulses depicting damage in G-D region. (b) Cross-sectional SEM image taken along line "A-B" depicts cracks underneath the drain side of gate edge which propagated toward the drain.

device width as clear from Fig. 14(b). This leads to electro-thermal instability and failure in the device. At lower PW, when the device is stressed for a shorter duration, the self-heating across the device naturally gets suppressed. As a result, the device sustains higher electric field and needs higher power to fail. Fig. 15(a) shows the SEM image of HEMT failed in ON-state under UV condition, stressed using 10-ns-wide pulses. It shows cracking in gate–drain region. The peak field and hotspot present at gate edge, generate stress in the vicinity of gate and leads to cracking of top AlGaN/GaN layers. Under the influence of gate–drain electric field, the crack propagates toward the drain as clear from cross-sectional SEM image of source/drain region shown in Fig. 15(b). Moreover, the hot spot under the gate peels-off gate metal as well.

C. Failure by Avalanche Instability

The devices, which fail while stressing them using shorter pulses under dark condition, show instability in snapback region at the breakdown point, which was depicted earlier in Fig. 11(a). Postfailure analysis of a device stressed using 10-ns-wide pulse under dark condition shows multiple damage points (cracks) along the device width as shown in Fig. 12(a). Individual crack/defect center independently pushes the device into the snapback state, however, as the carrier trapping and self-heating at shorter pulse are not sufficient for a hard failure

of the device, the region away from the damaged locations continues to conduct current in the subsequent pulse. This generates electrothermal instability along the device width and leads to unstable device behavior at the verge of breakdown. Devices which failed under UV condition, however, show clear permanent failure with a crack running between gate–drain region as shown in Fig. 15(a). This observation reconfirms that carrier trapping assists in avalanche instability and UV exposure suppresses it.

VII. Conclusion

For the first time, the physics of avalanche instability and SOA boundary in AlGaN/GaN HEMT are studied systematically. It was found that trap generation and carrier trapping lead to electric field shift and its peaking toward drain edge which enhance hole generation via II. Excess holes injected into buffer/transition region form highly conducting localized parasitic path(s)/filaments from drain-to-source under buffer, which increases the source–drain leakage. Moreover, accumulation of hot holes under gate, damaged the gate edge at the source side, triggered Gallium out-diffusion from GaN cap into Ni/Au Schottky gate and leads to failure in gate–source region. With UV exposure, carrier detrapping enhances from surface and buffer regions and peak field restores back at the gate edge toward drain which leads to the formation of pits/hotspots near gate edge toward drain. In this case, failure occurs exclusively in gate–drain region. Carrier trapping leads to cumulative degradation as evident from device degradation with each stress pulse under dark condition. Such a degradation, however, was found absent with UV light exposure. Power-to-fail decreases with an increase in stress time exhibiting a power law like behavior, whereas it linearly scales with source–drain spacing. In case of nonuniform carrier trapping along the device width, drain field peaks in localized regions along the device width. This causes the localized generation of excess holes and leads to the formation of multiple current filaments along the width, which triggers early instability and lowers the SOA boundary. Such a trap-assisted avalanche instability is found to be absent when carrier trapping gets suppressed using UV light exposure while stressing the devices. TCAD and failure analysis results nicely corroborate with the physics of avalanche instability presented.

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