Gaps in the Y-Function Method for Contact Resistance Extraction in 2D Few-Layer Transition Metal Dichalcogenide Back-Gated FETs

Kuruva Hemanjaneyulu, Jeevesh Kumar, *Member, IEEE,* and Mayank Shrivastava, *Senior Member, IEEE*

Abstract—Y-Function method is often used for 2D TMD back-gated FETs, attributed to its simplicity and the lithographic challenges in processing transfer length method (TLM) test structures over 2D TMD flakes. While the contact resistance extracted from the Y-Function method was shown to be comparable to the TLM method in an early work, its applicability was never tested rigorously for the entire experimental range of 2D TMD FETs. This work presents the limitations and failure conditions of the Y-Function method when used for extracting contact resistance in back-gated, few-layer TMD FETs. We have found that the Y-Function method does not apply to the entire experimental range, such as ohmic/Schottky barrier, source-drain electric field, contact resistance, etc., particularly for the layered material-based FETs. The influence of the Schottky barrier and drain bias is investigated thoroughly for four different 2D materials (MoS$_2$, MoSe$_2$, WS$_2$ and WSe$_2$). The experimental findings are then used to narrow down extraction window/conditions for the Y-Function method, which gives contact resistance estimation closer to TLM based approach for few-layer, back-gated TMD FETs.

Index Terms—Y-function method, contact resistance, TMD.

I. INTRODUCTION

CONTACT resistance extraction is essential for investigating the transparency of the contacts or while exploring carrier transport physics. In emerging materials such as layered transition metal dichalcogenides, it is not always convenient to prepare a Transfer Length Measurement structure or four-probe measurement structures to estimate the contact resistance. In such a case, a simpler method is desired, which has recently given popularity to the Y-function method for layered semiconductors. The Y function method was earlier used to extract contact resistance, mobility, and threshold voltages in bulk MOSFETs [1], [2]. The method was recently

validated for MoS$_2$ FETs by Chang *et. al* [3]. Since then the Y-Function extraction method has been used widely in many reports on the layered semiconductors [4]–[9].

Though the Y-Function method was benchmarked with the TLM approach, we have found that it often deviates from TLM-based estimations. This work presents the Y-Function model failure conditions and gaps in contact resistance extraction while investigating different layered semiconductors. While showing the dependency of the model on various factors such as Schottky barrier height, drain bias, etc., this work provides insights on how to better estimate contact resistance using this method.

II. EXPERIMENTAL APPROACH

To address gaps in the Y-Function method, we have realized Transfer Length Method (TLM) test structures over four different TMD channels (MoS$_2$, MoSe$_2$, WS$_2$ and WSe$_2$). This allows us to unify our findings across a wide range of TMDs. TLM test structure inherently allows characterizing FETs with different channel lengths. Data from individual FETs of different channel lengths allows extraction of contact resistance and mobility using the Y-Function method. The TLM structure as a whole is also used to extract intrinsic contact resistance (R_{CY}) and field-effect mobility ($\mu_{FE} = (g_M \cdot L_G)/(C_{OX} \cdot V_{DS} \cdot W)$). A 2D AFM scan of a device under test is presented in Figure 1.

Y-Function method attained the name for its fundamental dependency on a parameter, namely Y-Function $(Y - Function(Y - F) = I_D/\sqrt{g_M})$. This parameter is used to estimate the intrinsic mobility and threshold voltage. The threshold voltage is estimated by the linear extrapolation of Y-F vs. V_{GS} curve from higher gate bias. Here the device is expected to be in deep inversion, towards the X-axis. Moreover, the slope from the linear extrapolation of Y-F vs. V_{GS} is used to extract the mobility $(\mu_0 = ((Slope)^2 \cdot L)/(C_{OX} \cdot W \cdot V_{DS}))$. Finally, using the following two equations, the contact resistance is estimated: $\theta = [(I_D/g_M \cdot (V_G - V_{Th})) - 1]/[V_G - V_{Th}]$ & $Y - Function Resistance = (\theta \cdot L)/(W \cdot C_{OX} \cdot \mu_0)$. The Y-Function Resistance is then plotted as a function of gate bias. The plot must saturate at higher gate biases where the device is expected to be in deep inversion. The average value of Y-Function Resistance in the saturated regime is considered as the Y-Function contact resistance.
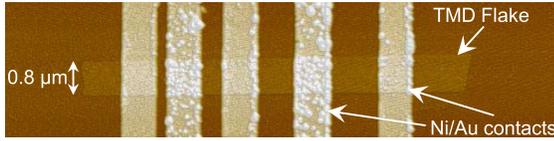
Fig. 1. AFM scan of one of the fabricated TLM device with different channel lengths. TMD Flakes were first exfoliated using a special low residue blue tape over a cleaned SiO_2(90nm)/Si(p^+) substrate. Optically identified flakes were characterized through AFM and Raman spectroscopy for the optimum thickness ($\approx$10nm) and negligible defects. The devices under test were realized using Electron Beam Lithography while using PMMA as the resist material. Before depositing Source/Drain contacts, the flakes were also patterned using RIE Fluorine to develop back-gated FETs / TLM test structures with fixed channel width through out the channel and across all samples. Ni/Au contacts were used (Ni being in direct contact with TMD) in all the devices under test. Since the devices under test are non-encapsulated, all electrical measurements in this manuscript were conducted in ultra high vacuum condition ($\approx10^{-6}$ torr) to avoid atmospheric influence.
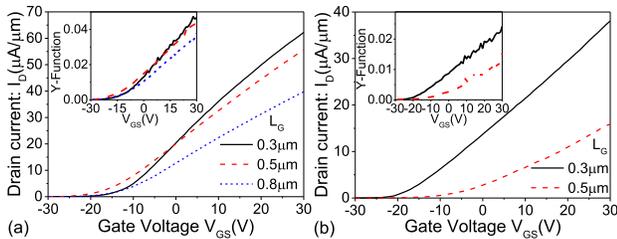
Fig. 2. Input characteristics of devices under test (a) Device-1 & (b) Device-2. Insets present the respective Y-Function with gate bias.

III. MODEL FAILURE

The Y-Function method has been introduced to evaluate contact resistance and intrinsic mobility across a single channel transistor. The method's primary governing condition is the deep inversion, where the drain current deviates well from square law characteristics. For TMD FETs, drain current vs. gate voltage relation should have a dependency of $I_D \propto V_{Gov}^x$. Here $x < 1$ and $V_{Gov} = V_{GS} - V_{Th}$ is the gate overdrive. It satisfies deep inversion with the gate voltage significantly above the threshold voltage of the transistors with sub-micron channel lengths. The characteristics of two different MoS_2 TLM structures with different channel lengths are tested to validate such a dependency. Figure 2 presents the input characteristics of two different sets/categories of devices (Device-1 & Device-2) with different dependence of drain current on the gate voltage. Device-1 set/category depicts characteristics that validate the expression given above, whereas Device-2 set/category doesn't. Across all devices (inset of Figure 2) extracted Y-Function depicted linear variation with gate bias sweep after a certain gate voltage.

While for Device-1, as depicted in Figure 3(a), the extracted resistance was always positive. The same, however, for Device-2 extends to negative resistance values as shown in Figure 3(b) (see the circled region). The later one is misleading. Figure 3(c) & (d) compares the Y-function extracted contact resistance and mobility, as a function of channel length, with the contact resistance and mobility extracted from TLM-based approach and transconductance method, respectively. For Device-1 (Figure 3(c)), the extracted Y-Function contact resistance and long channel mobility match to that extracted from TLM-method. However, the same in the case
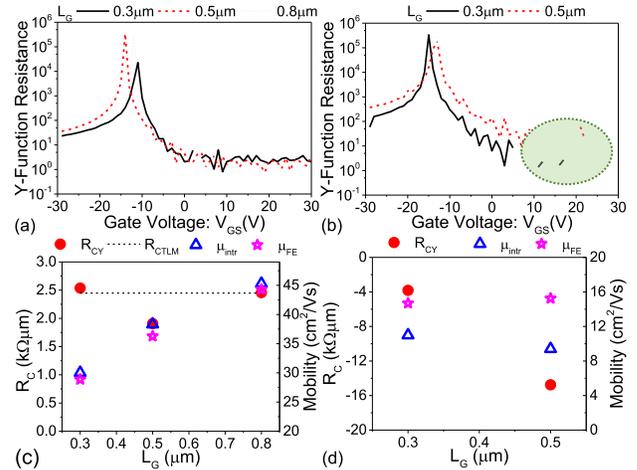
Fig. 3. Y-Function resistance with gate bias for (a) Device-1 and (b) Device-2. Extracted contact resistance (R_{CY}) and intrinsic mobility (μ_{intr}) with respect to channel length compared with TLM-extracted contact resistance (R_{C-TLM}) and field-effect mobilities (μ_{FE}) for (c) Device-1 and (d) Device-2.

of Device-2 didn't find any correlation. This difference is attributed to the input characteristics where the deep inversion condition is not satisfied, leading to misleading estimations. However, it should be noted that both the category of devices were realized over same wafer/die and had the same flake/channel thickness. It implies that the applicability condition for accurately extracting the device parameters from the Y-Function method is not always the same for all devices, despite realizing them under the same condition.

IV. ACCURATE ESTIMATION WINDOW

The subsequent discussions are for devices which falls into the Device-1 category. The observed ambiguity is attributed to a missing account for the Schottky nature of the contact, which is often common in TMD FETs. We have addressed this by extracting Y-Function contact resistance and mobility as a function of the drain-source electric field for different channel lengths. Subsequently we have narrowed down the extraction window by comparing it with TLM extracted contact resistance and field-effect mobility.

Figure 4 depicts Y-function extracted contact resistance (R_{CY}) as a function of drain bias (source-drain e-field) for different channel lengths and different layered semiconductors. For MoS_2 (Fig. 4(a)) and WSe_2 FETs (Fig. 4(d)), R_{CY} falls initially as the drain bias is increased, touches a minimum value, and then rolls back. Whereas, for WS_2 (Fig. 4(b)) and $MoSe_2$ FETs (Fig. 4(c)), R_{CY} falls monotonously as the drain bias was increased. As a function of channel length, for a given drain bias, Y-function extracted contact resistance monotonously increased as the channel length was increased. As observed in MoS_2 and WSe_2 FETs, the dependency is attributed to the inherent Schottky barrier across the metal-TMD interface [10], [11]. The initial increase in V_{DS} lowers the tunneling barrier width, thereby lowering the contact resistance. However, the barrier width would saturate after a particular V_{DS} bias, resulting in the contact resistance minima. Any further increase in the drain bias will deviate the device's operation from the linear regime, which manifests as increased contact resistance extracted using the Y-Function
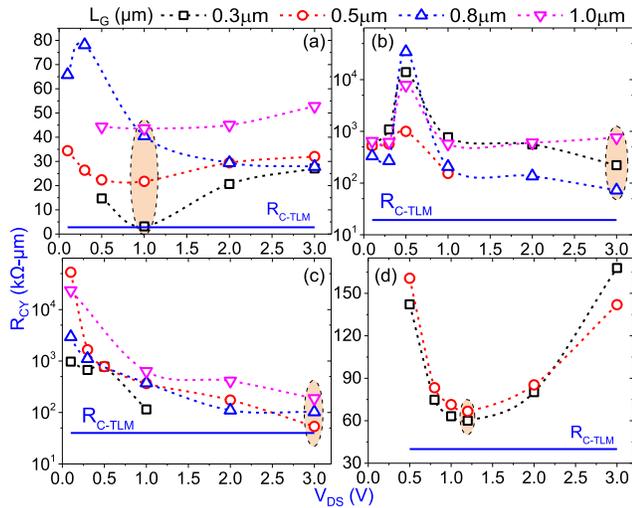
Fig. 4. Comparison of Y-Function extracted contact resistance as a function of drain bias and channel lengths, with intrinsic (TLM extracted) contact resistance for following TMD FETs: (a) MoS_2, (b) WS_2, (c) $MoSe_2$ and (d) WSe_2.

Fig. 5. Comparison of Y-Function extracted channel mobility (Solid Symbol) with field effect mobility (Open Symbol), as a function of drain bias and channel lengths, for following TMD FETs: (a) MoS_2, (b) WS_2, (c) $MoSe_2$ and (d) WSe_2.

approach. For $MoSe_2$ and WS_2 FETs, attributed to higher Schottky barrier height and possibly high tunnelling width, the applied V_{DS} was not sufficient to saturate the tunnel barrier width and drift the operation away from the linear regime. The channel length dependency is attributed to the suppressed influence of the drain field over the tunnel barrier width at the source side when the channel length was increased. To confirm this, the Schottky barrier height of metal$-MoS_2$ and metal$-WS_2$ interfaces were extracted. MoS_2 devices were found to have a lower Schottky barrier height (53.8meV) than WS_2 FETs (83.4meV), confirming the difference explained above.

These trends show that the Y-Function extracted contact resistance's accuracy strongly depends on the channel length, material type, workfunction difference with the contact metal and source-drain field. This dependency introduces significant uncertainty in the extraction approach. In all cases, the Y-Function approach overestimates the contact resistance, and it diverges away from the intrinsic contact resistance (TLM extracted) as the channel length increases. The closest estimate given by the Y-Function approach was only at its minima point for the shortest channel length.

The same method has earlier been used in several reports to estimate transistors' mobility. A similar kind of dependency has been found for estimating the mobility of the device using this method. Figure 5 depicts extracted channel mobility as a function of drain bias and channel length for different channel materials. Mobility also shows a strong dependence on the Schottky barrier present. For MoS_2, extracted mobility initially increases with the drain bias, which subsequently drops to a medium-range value for all channel lengths. On the other hand, field-effect mobility extracted using the transconductance method was seen to drop with increasing drain bias, which eventually saturated to lower values. In the Y-Function method, the variation in mobility is attributed to the dependencies of Schottky barrier width on drain bias and channel length.

In general, Y-Function mobility for most drain bias and channel lengths was lower than mobility extracted by
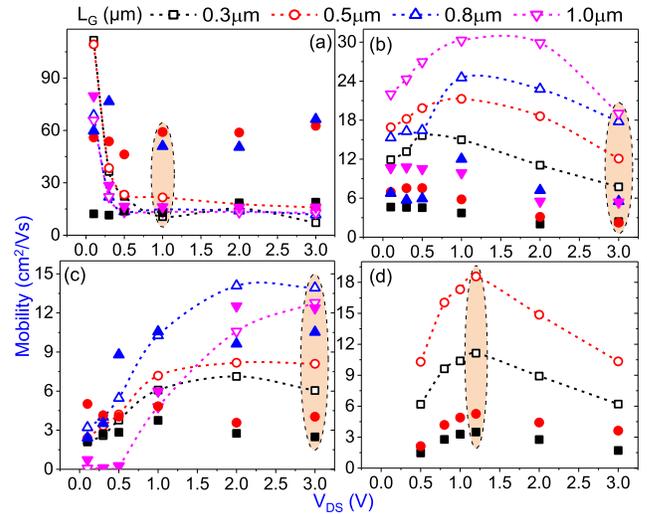
TLM/transconductance method. This is attributed to the influence of the Schottky barrier and its relative change as a function of drain bias and channel length. However, the Y-Function extracted mobility was found to converge to TLM/transconductance extracted field-effect mobility in the same window (and shorter channel length) that resulted in a closer match to contact resistance. Therefore, it can be concluded that the Y-Function method gives accurate predictions only when the influence of the Schottky barrier is negligible. It is worth highlighting that the phenomena reported in this work was confirmed across dozens of devices, which makes the finding universal.

V. CONCLUSION

Y-Function method for estimating contact resistance and channel mobility, particularly for channel materials like few-layer TMDs integrated in a back-gated FET, was found to depend on various factors such as drain bias, channel length, Schottky barrier, etc. With drain bias, the Y-Function contact resistance had a U-shape trend. The initial drop is attributed to the reduction in Schottky barrier width and subsequent rise is due to the deviation in the device's operation from the linear regime. The valley point strongly depends on the metal-TMD interface. Moreover, the contact resistance increases with increasing channel lengths, which is not observed in the TLM approach. The Y-Function extracted mobility also follows a similar trend. In general, the Y-Function method underestimates mobility and overestimates contact resistance for most drain bias and channel lengths. Y-Function method gives closer predictions only when the influence of the Schottky barrier is minimized, i.e., for an optimum drain bias (which depends on the metal-TMD interface) and the lowest channel length. The Y-Function method, therefore, particularly when used for back-gated, few-layer TMD FETs, is not universal and free of errors like the TLM method. However, closer estimates can be made by identifying the right estimation window as presented in this work.

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