Part II: Proposals to Independently Engineer Donor and Acceptor Trap Concentrations in GaN Buffer for Ultrahigh Breakdown AlGaN/GaN HEMTs

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***Abstract*— In part I of this paper, we developed physical insights into the role and impact of acceptor and donor traps—resulting from C-doping in GaN buffer—on avalanche breakdown in AlGaN/GaN HEMT devices. It was found that the donor traps are mandatory to explain the breakdown voltage improvement. In this paper, silicon doping is proposed and explored as an alternative to independently engineer donor trap concentration and profile. Keeping in mind the acceptor and donor trap relative concentration requirement for achieving higher breakdown buffer, as depicted in part I of this paper, silicon & carbon codoping of GaN buffer is proposed and explored in this paper. The proposed improvement in breakdown voltage is supported by physical insight into the avalanche phenomena and role of acceptor/donor traps. GaN buffer design parameters and their impact on breakdown voltage as well as leakage current are presented. Finally, a modified Si-doping profile in the GaN buffer is proposed to lower the C-doping concentration near GaN channel to mitigate the adverse effects of acceptor traps in GaN buffer.**

***Index Terms*— Acceptor traps, AlGaN/GaN HEMTs, breakdown voltage, buffer doping profile, carbon doping, donor traps, Si doping.**

I. Introduction

FOR AlGaN/GaN HEMTs to result in high breakdown voltage (V_{BD}) with low ON-resistance, it is important to have a highly resistive GaN buffer [1]. Standard growth conditions result in an unintentional doping (UID) of the GaN buffer [2], which leads to increased buffer leakage and reduced V_{BD} [1]. In order to achieve semi-insulating GaN buffer, compensation doping is a common technique. Carbon (C) doping in GaN buffer is a well-known method to increase buffer resistivity and lower buffer leakage, which apparently improves V_{BD} of AlGaN/GaN HEMT devices as well [3]. It is well known that the C-doping results in a resistive buffer due to introduction of deep acceptor traps [4], [5]. However, as has been observed in earlier works, a significant doping of C in GaN buffer is required to achieve any substantial improvement in V_{BD}, as shown in Fig. 1.

Clearly, as also seen in part I of this paper [8], the doping requirement for V_{BD} improvement is higher compared to what is required to merely increase buffer resistivity. A closer study of C-doping behavior in GaN buffer, presented in part I of this paper, revealed self-compensating nature of traps induced by C-doping to be the key parameter controlling the V_{BD} [8]. Furthermore, it was observed that donor traps had a major contribution in delayed avalanche action due to vertical field relaxation. Without presence of donor traps, V_{BD} does not improve significantly. In addition to this, acceptor traps were found to have a limited impact on avalanche process and were

TABLE I
C-Doping Concentration Required in GaN Buffer to Achieve High Breakdown Voltage in AlGaN/GaN HEMT Devices

Thickness of C-doped buffer	C-doping concentration (cm^{-3})	Breakdown Voltage	Ref.
1.5 μm	4 x 10^{19}	1000 V	[3]
3 μm	4 x 10^{19}	1000 V	[6]
4.6 μm	1 x 10^{19} - 1 x 10^{20}	650 V	[7]

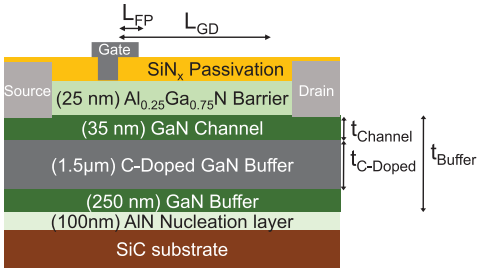

Fig. 1. C-doped AlGaN/GaN HEMT structure used in this paper for demonstrating breakdown voltage improvement with engineered trap profiles. The structure was adapted from [3].

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rather necessary to support the donor trap concentration by compensating the free charge carriers introduced by donor traps in GaN buffer. It was thus concluded that the required improvement in V_{BD} can be achieved along with optimized dc performance of the device by reducing the acceptor trap concentration and maximizing the donor trap concentration [8]. However, behavior of C as acceptor or donor trap site in GaN buffer is a function of process conditions. Through density functional theory-based calculations, it was shown in [4], that under typical GaN buffer growth conditions (n-type with Ga face), C has a lower probability to behave as donor type trap site in GaN buffer, associated with high formation energy required for C-Ga substitution. On the other hand, C has a higher probability to replace N due to lower formation energy required for C-N substitution [4]. Under these conditions, C is expected to result in a much higher acceptor trap concentration as compared to donor trap concentration. This also explains the high C-doping concentrations required to achieve improvement in V_{BD}. This in turn results in a high acceptor trap concentration in the GaN buffer, resulting in a negative impact on device performance. Acceptor traps in GaN buffer are responsible for several major performance bottlenecks, like dc-RF dispersion [7], [9], current collapse [10]–[16], ambient light exposure dependent safe operating area of the device [17], hot electron induced effects [18], performance degradation [12], [19], [20], kink effect [21], and so on. The V_{BD} improvement with C-doping of GaN buffer thus involves a tradeoff with the device performance parameters as mentioned above, dc-RF dispersion being the worst affected parameter limiting the RF performance of device [7], [9], [22]. While C-doping is well known to behave as acceptor traps in GaN buffer [5], a separate doping source for donor traps can help in reducing the overall C-doping requirement while simultaneously improving V_{BD} of the device. Having independent doping sources to achieve required acceptor and donor trap concentration in GaN buffer can enable: 1) minimizing acceptor trap concentration or C-doping to only what is required to increase buffer resistivity/reduce buffer leakage and 2) independently achieve required/optimum donor trap concentration required to improve V_{BD} while maintaining device performance. This reduced C-doping requirement will in turn limit the acceptor trap concentration in GaN buffer thereby improving the dc/RF performance of the device while achieving high V_{BD}.

With the above motivation in mind, this paper proposes a novel method to independently control the acceptor and donor trap concentrations in GaN buffer, thereby tapping the full potential of AlGaN/GaN HEMT devices without affecting device performance. Here C-doping is proposed for introducing acceptor traps whereas Si doping is proposed and demonstrated using computations to play the role of donor traps in GaN buffer. Section II presents the device structure considered in this paper along with a description of the simulation setup. Section III introduces Si-doping in GaN buffer, which is a well known n-type dopant in GaN, as a viable source for independently achieving the required donor trap concentration. The discussion is supported with associated physics to have a clear understanding of the impact of Si-doping when compared to C induced donor traps. Section IV discusses different design parameters related to C and Si-doping of GaN buffer. In Section V, a novel Si-doping profile in conjunction with C-doping induced acceptor traps is proposed to optimize device performance without compromising on the breakdown performance of the device. Section VI concludes the results presented in this paper.

II. Device Structure & Simulation Framework

The device structure used in this paper is adapted from [3] and is as shown in Fig. 1. Simulation framework is similar to the one described in our earlier work [23], and is discussed in detail in part I of this paper [8]. Impact ionization is taken into account following the Chynoweth law [24]. Quantum correction, lattice and carrier heating are neglected for breakdown calculations while polarization effect is taken into account at all heteromaterial interfaces. Donor type surface traps, channel electron density, mobility and related transport parameters are calibrated with the experimental data as per the framework discussed in our earlier work [23]. Following physical design parameters of the device are kept constant: source to gate distance (L_{SG}) = 1 μm, gate length (L_{Gate}) = 0.7 μm, L_{GD} = 5 μm, L_{FP} = 0.6 μm, $t_{channel}$ = 35 nm, $t_{C\text{-}Doped}$ = 1.5 μm. An unintentional n-type doping of 1×10^{15} cm^{-3} was considered in the GaN buffer. For extraction of V_{BD}, the device, having a threshold voltage of -1 V, was biased in the OFF-state with $V_{GS} = -5$ V. Substrate was kept open to isolate any substrate induced effects on V_{BD}.

III. Silicon Doping to Independently Engineer Donor Trap Concentration With C-Doping

Donor traps induced by C-doping effectively address two issues: 1) compensate excess hole density induced by acceptor traps and 2) enable vertical field relaxation by modulating space-charge profile. Since these donor traps are known to be shallow in nature with activation energy of 0.11 eV relative to conduction band edge [9], [22], their presence can be considered as equivalent to n-type doping in GaN buffer. Thus, a similar function can be achieved by introducing n-type doping in GaN buffer with doping agents such as Si [2]. Having a reliable source for n-type carriers can significantly bring down the C-doping requirement, as C-doping is now required only for the acceptor traps, which has a lower formation energy compared to donor traps [4]. As noted in part I of this paper, a significantly lower acceptor trap concentration can be used to achieve similar breakdown performance provided that an optimum concentration of donor traps is present [8]. Based on these observations, Si-doping of C-doped GaN buffer is proposed here to bring down the C-doping requirement while maintaining high breakdown voltage. Reduced C-doping requirement can potentially improve the channel performance as well. In order to validate V_{BD} improvement, computations are performed by considering uniformly distributed acceptor traps in the C-doped GaN buffer region while donor traps are replaced by Si-doping. Si-doping discussed here is considered only in the region where C-doping is present. Rest of the buffer region has a lower UID of 1×10^{15} cm^{-3}.

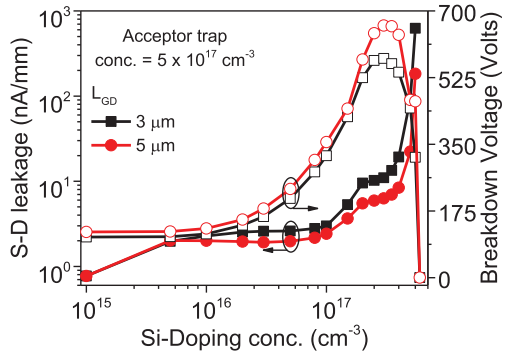

Fig. 2. Impact of Si-doping inside the C-doped GaN buffer on breakdown voltage of the device, and Source/Drain leakage current under off-state. Leakage current is extracted at $V_{DS} = V_{BD}/2$. Si-doping concentration depicted, here, is considered to be uniformly distributed in the complete C-doped GaN buffer.

A. Impact on Breakdown Voltage

Fig. 2 depicts impact of Si-doping concentration on V_{BD} of the device in presence of a fixed acceptor trap concentration. An increase in V_{BD} of the device can be observed as Si-doping concentration is increased. Furthermore, scaling of V_{BD} with L_{GD} is also observed, as Si-doping concentration is increased, which signifies electric field redistribution in the vertical direction, as discussed in part I of this paper [8]. However, as concentration of Si-doping approaches acceptor trap concentration, V_{BD} was found to fall to much lower values, which is attributed to increased leakage current, as shown in Fig. 2. These results suggest that Si codoping with C-doping-induced acceptor traps can result in V_{BD} improvement; however, maximum Si-doping concentration is limited by the acceptor trap concentration induced by C-doping. While this behavior of Si-doping is similar to that observed with donor traps induced by C-doping, following sections provide a physical insight into the impact of Si-doping on factors affecting the avalanche breakdown of GaN buffer.

B. Physical Insights: Impact of Si-C Codoping on Avalanche Breakdown

Si-doping can influence GaN buffer properties in following ways: 1) it changes the parasitic hole and electron density in the GaN buffer and 2) as an ionized dopant, it can modulate the space-charge distribution and vertical electric field in the GaN buffer. The first aspect is evaluated by observing free hole density and ionized acceptor trap density in GaN buffer as a function of Si-doping concentration. Fig. 3(a) shows that free hole density in the GaN buffer, induced by acceptor traps, is compensated by Si-doping, thereby maintaining the buffer resistivity. On the other hand, excess free electrons induced by Si-doping are trapped by the acceptor traps already present in GaN buffer due to C-doping. This can be observed from the increase in ionized acceptor trap concentration with Si-doping concentration, as shown in Fig. 3(b). However, this condition is true only until the Si-doping concentration is less than the acceptor trap concentration. This further explains the limit imposed by acceptor trap concentration on maximum allowed Si-doping concentration, as shown in Fig. 2.

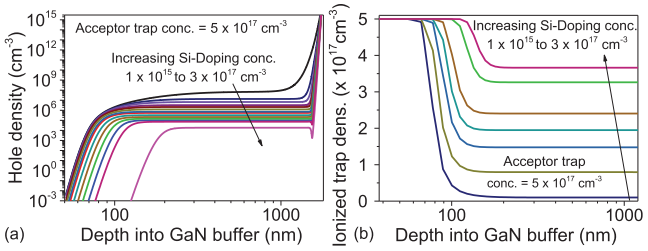

Fig. 3. Impact of Si-doping in C-doped GaN buffer on (a) parasitic hole density induced by acceptor traps and (b) ionized acceptor trap density in GaN buffer.

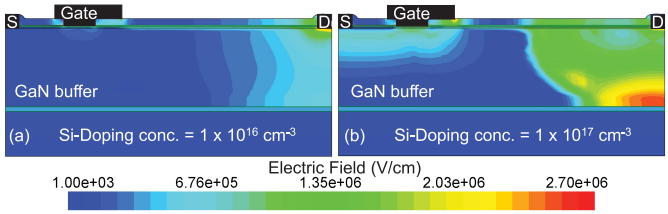

Fig. 4. Electric field contours extracted for a fixed acceptor trap concentration in the C-doped region for Si-doping concentration of (a) 1×10^{16} cm^{-3} and (b) 1×10^{17} cm^{-3}. E-field redistribution in the deep GaN buffer region can be observed with increased Si-doping. Bias conditions are taken as $V_{GS} = -5$ V and $V_{DS} = V_{BD}$.

In order to understand the second aspect, i.e., impact of Si-doping on space-charge distribution and vertical electric field, electric field contours for different Si-doping concentrations are compared in Fig. 4. These contours suggest an increased vertical electric field redistribution in deep GaN buffer region under the drain electrode, as Si doping concentration is increased. In addition to this, the vertical electric field extracted along a cut line near the drain edge, shown in Fig. 5(a), indicates an increased redistribution of electric field in the complete GaN buffer region, as Si-doping concentration is increased. As can be observed, the vertical field is now effectively redistributed between two electric field peaks, thereby improving the voltage handling capacity of the device.

This effect is similar to the one observed with donor traps in the GaN buffer, explained in part I of this paper [8]. As was observed with donor traps, the vertical field redistribution in the GaN buffer can be attributed to space-charge modulation in presence of donor traps (here Si dopants) and acceptor traps. In this case, Si dopants and acceptor traps provide positive and negative charges, respectively, in their ionized state. This modulates the space-charge profile in the buffer region, which changes the E-field distribution. In order to evaluate this, ionized acceptor trap density, Si doping concentration, and vertical electric field extracted along the GaN buffer are shown in Fig. 5(b). It can be observed from Fig. 5(c) that, on application of high drain bias voltage, the ionized acceptor trap density falls to much lower values. This is attributed to the deep energy levels associated with these traps (located at an energy level of 0.9 eV above the valence band edge), which results in deionization of these traps by: 1) detrapping of electrons and subsequent drift movement under influence of applied drain electric field and/or 2) capturing of holes injected by drain electrode under influence of high electric field near drain edge. On the other hand, Si dopants are

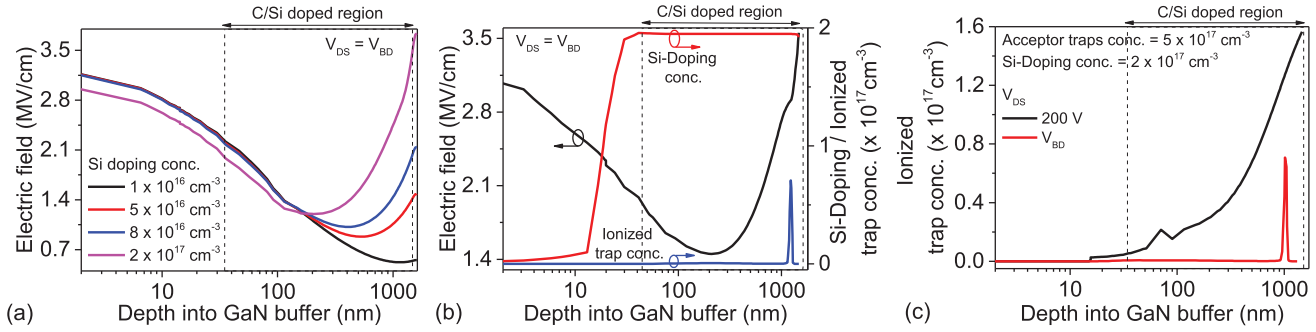

Fig. 5. (a) Impact of increasing Si-doping concentration on vertical electric field profile near the drain edge, extracted at the onset of avalanche breakdown. Avalanche hot-spot was observed near the drain edge. (b) Electric field profile along with doping concentration and ionized acceptor trap density near the drain edge. (c) Change in ionized trap concentration and profile as a function of applied drain voltage.

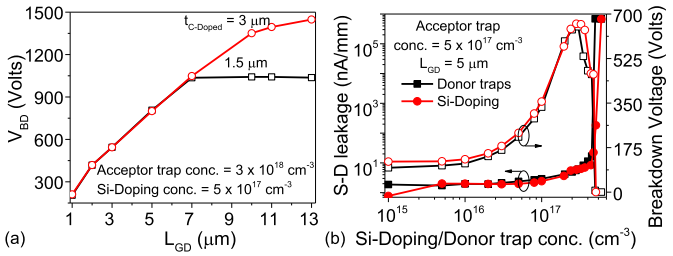

Fig. 6. (a) Improvement in V_{BD} with lateral and vertical scaling of the device in presence of C-doping induced acceptor traps and Si doping in GaN buffer. (b) Relative comparison of the impact of Si-doping concentration with that of donor trap concentration on V_{BD} and source/drain leakage current. Si-doping (or donor traps) is considered to be uniformly distributed in the complete C-doped GaN buffer.

completely ionized under influence of drain field. These factors result in a reduction in ionized acceptor traps in GaN buffer, as drain bias is increased, while the Si dopants are ionized, as shown in Fig. 5(b). These ionized traps and dopants result in a net positive charge in the deep GaN buffer, which leads to electric field redistribution according to the relation $dE/dx \approx qN_{\mathrm{SiDop}}/\epsilon_{\mathrm{GaN}}$, as depicted in Fig. 5(b). Here, N_{SiDop} is the concentration of ionized Si dopants, and ϵ_{GaN} is the electric permittivity of GaN. With electric field redistribution in the deep GaN buffer, electric field near the drain edge relaxes, which results in an improved V_{BD} of the device. Owing to similar relation ($dE/dx \propto N_{\mathrm{SiDop}}$), redistribution of vertical electric field in the deep GaN buffer increases, as Si-doping concentration is increased, as shown in Fig. 5(a), which results in further improvement in V_{BD} of the device. Furthermore, as shown in Fig. 6(a), V_{BD} of the device shows improvement with lateral scaling (L_{GD}) as well as vertical scaling ($t_{\mathrm{C\text{-}Channel}}$) of the device in the presence of Si-doping along with C-doping-induced acceptor traps in the GaN buffer.

C. Comparison With Donor Traps in GaN Buffer

This section compares V_{BD} improvement and associated device physics for the following two cases: 1) device with C-doping induced acceptor traps along with compensating donor traps and 2) device with C-doping induced acceptor traps and Si-doping in the same region for donor traps. Fig. 6(b) depicts similar V_{BD} in both the cases, thereby quantifying the argument that Si-doping in GaN buffer can be effectively used to independently engineer the donor trap concentration in C-doped GaN buffer. Furthermore, the leakage current characteristics, as shown in Fig. 6(b), indicate an approximately equal leakage current for both the cases.

IV. Si-C Codoping: Buffer Design Guidelines

A. Acceptor Trap Concentration and Si Doping

One of the primary device design objective, for achieving high V_{BD} without affecting dc/RF performance of the device, is to minimize acceptor trap concentration while maintaining high V_{BD}. This section compares V_{BD} of the device around two design variables, i.e., C-doping (acceptor traps) and Si-doping (donor trap) concentrations. For this study, lateral dimensions of the device were increased to $L_{GD} = 10$ μm and $L_{FP} = 3$ μm to avoid lateral field driven avalanche phenomena. Furthermore, the C-doped buffer thickness was increased to 3 μm, in order to have a better estimate of V_{BD} improvement due to Si-doping. Fig. 7(a) and (b) compares V_{BD} and S/D leakage current of the device, respectively, for different acceptor trap and Si-doping concentrations. Fig. 7 shows that irrespective of acceptor trap concentration, improvement in V_{BD} largely depends on relative concentration of acceptor traps and Si doping. This makes it possible to retain V_{BD} of the device, even while reducing the C-doping concentration by maintaining the required Si doping concentration. However, as noted earlier, maximum Si-doping concentration is limited by acceptor trap concentration and leakage through the device, as shown in Fig. 7(b). Furthermore, Fig. 7(b) shows an increased leakage current for two cases: 1) when Si-doping concentration is comparable to or greater than acceptor trap concentration and 2) when acceptor trap concentration is high when compared to Si-doping concentration. In the former case, leakage current is due to excess electrons induced by relatively higher Si-doping concentrations. Increased leakage in the latter case is attributed to holes induced by higher concentration of acceptor traps. These holes in combination with hole injection from drain electrode under presence of higher electric field near drain edge result in an increase in the leakage current.

This is validated in Fig. 8, which depicts that in the former case, the total current density [see Fig. 8(a)] is dominated

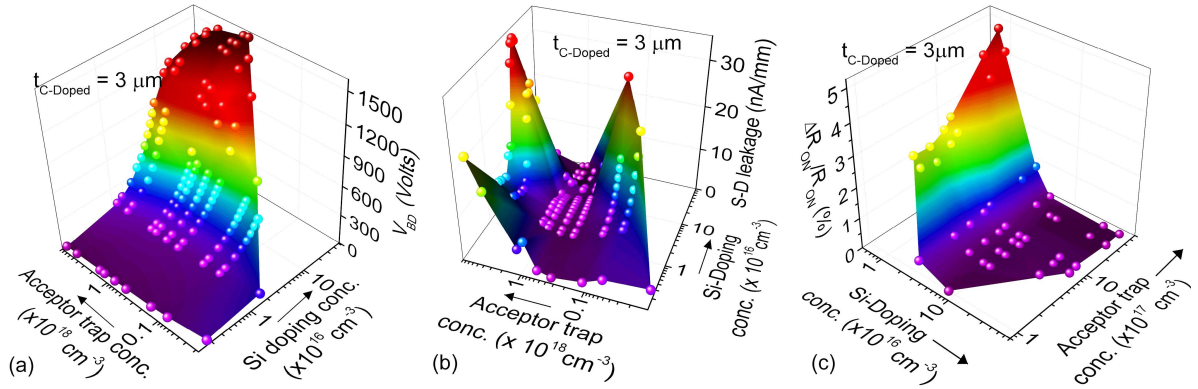

Fig. 7. Impact of Si-doping and C-doping induced acceptor trap concentration on (a) breakdown voltage, (b) leakage current in the device, and (c) dynamic R_{ON}. Leakage current is extracted at $V_{DS} = V_{BD}/2$. Si-doping concentration depicted, here, is considered to be uniformly distributed in the complete C-doped GaN buffer. A constant GaN channel thickness, $t_{Channel}$, of 35 nm is considered. Method of extracting dynamic R_{ON} of the device and timing specifications of gate and drain pulses were adopted from experimental work in [25]. The quiescent bias conditions were taken as $V_{GS} = -5$ V and $V_{DS} = 45$ V.

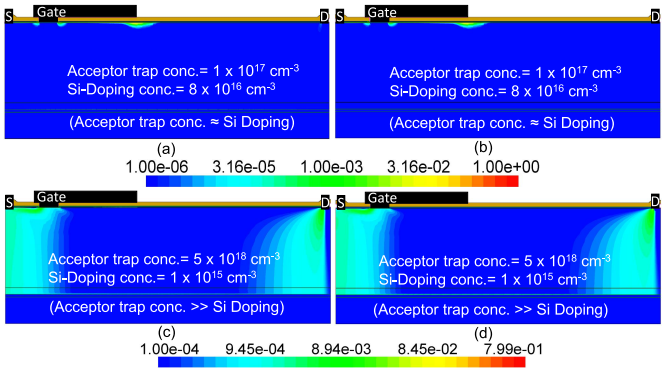

Fig. 8. (a) Total current density and (b) electron current density when acceptor trap concentration was similar to Si-doping concentration (or donor trap concentration). (c) Total current density and (b) hole current density when acceptor trap concentration was significantly higher than Si-doping concentration (or donor trap concentration).

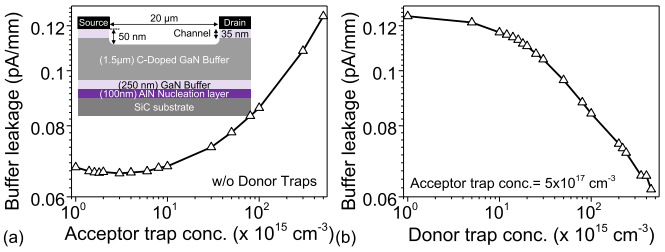

Fig. 9. (a) Buffer leakage current as a function of acceptor traps in absence of donor traps. (b) Buffer leakage current as a function of donor trap concentration for a fixed acceptor trap concentration. Inset shows the structure used to simulate buffer leakage. Leakage current was extracted at a voltage 50% of V_{BD}.

by electron current [see Fig. 8(b)] in the channel region, whereas in the later case, total current density [see Fig. 8(c)] is dominated by hole current in the buffer region [see Fig. 8(d)]. It is worth highlighting that the buffer leakage, as shown in Fig. 9, is in the orders of magnitude smaller than S/D leakage. This result highlights the role of C-doping as back barrier as well, which improves the gate control over channel by confining the 2-D electron gas (2DEG) closer to the AlGaN barrier, thereby lowering the S/D leakage current. Keeping these results in mind, it would be worth concluding that rather than using buffer leakage, S/D leakage together with V_{BD} is an appropriate measure to optimize C-doping and stack design. Furthermore, Fig. 7(c) depicts the dynamic performance of the device by comparing percentage change in ON-resistance of the device, $\Delta R_{ON}/R_{ON} = (R_{Dynamic} - R_{dc})/R_{dc} \times 100\%$, as a function of C-doping induced traps and Si-doping concentration in the GaN buffer. Here, $R_{Dynamic}$ is the dynamic-ON-resistance of the device. There is a significant increase in dynamic ON-resistance of the device, as acceptor trap concentration is increased in absence of Si-doping. However, as the Si-doping concentration is increased, the dynamic ON-resistance of the device comes closer to the dc ON-resistance. This indicates that an optimized Si-doping concentration in combination with C-doping of the GaN buffer can improve the dynamic performance of the device, besides improving the V_{BD} and maintaining a lower leakage current. From this analysis, an optimum acceptor trap concentration of 5×10^{17} cm^{-3} and Si-doping concentration of 2×10^{17} cm^{-3} is used for subsequent analysis.

B. Channel Thickness

From device performance point of view, a thicker GaN channel is desired to minimize impact on channel electron density and mobility. Channel electron density will be affected by acceptor traps induced by C-doping. On the other hand, Si-doping will induce charged ions and will affect the electron mobility. However, increasing the channel thickness will affect breakdown performance of the device. In order to evaluate impact of channel thickness on device performance, $t_{Channel}$ was varied while keeping the total buffer thickness unchanged. Thus, with an increase/decrease in $t_{Channel}$, $t_{C\text{-}Doped}$ was varied to maintain a constant buffer thickness. Fig. 10(a) compares breakdown performance of the device for different values of $t_{Channel}$. It interestingly shows a sublinear reduction in V_{BD} with increasing $t_{Channel}$ up to 1 μm; however, a sharp reduction in V_{BD} is seen beyond $t_{Channel} = 1$ μm. Furthermore, V_{BD} was found to remain mostly unchanged up to the channel thickness

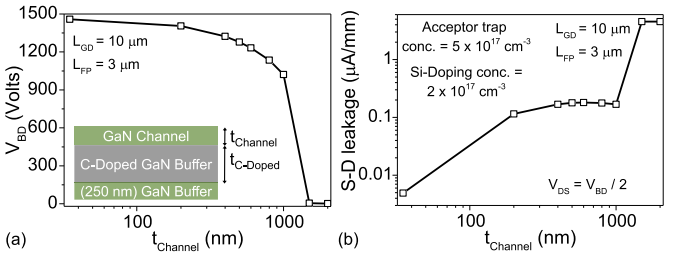

Fig. 10. Impact of GaN channel thickness ($t_{Channel}$) on (a) breakdown voltage and (b) source–drain leakage current extracted at $V_{DS} = V_{BD}/2$. Total thickness of the GaN buffer was kept constant at 3 μm. Thus, with an increase in $t_{Channel}$, $t_{C\text{-}Doped}$ was reduced to maintain a constant total buffer thickness. Uniform Si-doping and acceptor trap concentration were considered in the C-doped GaN buffer region.

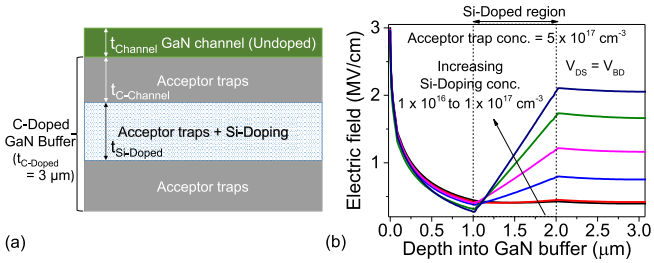

Fig. 11. (a) Proposed C-doped buffer stack below undoped GaN channel with engineered Si & C doping profile. C-doped buffer region consists of three regions, i.e., Si-C codoped region, which is sandwiched between regions only with C-doping. (b) Impact of increasing Si-doping concentration on vertical electric field redistribution in the case of the modified doping profile.

of ~250 nm. Moreover, Fig. 10(b) indicates a sharp increase in leakage current for channel thicker than 1 μm. An optimum channel thickness can thus be selected for achieving the desired performance. Due to limited availability of data on impact of Si-doping on channel mobility, it is difficult to comment on ON-resistance of the device; however, a thicker channel is expected to reduce impact of Si-doping on channel mobility, thereby reducing ON-resistance.

V. Si-C Codoping: Trap Profile Engineering

As presented in the previous section, a thinner GaN channel is required to maintain high V_{BD} of the device, whereas a thicker channel would shift the Si doped region away from 2DEG minimizing its adverse impact on 2DEG mobility. On the other hand, Si-doping is responsible for electric field redistribution in deep GaN buffer region, which is independent of C-doping and enables an independent control over trap profiles. To address both the topics, a modified Si-doping profile is proposed in Fig. 11(a). Here, C-doped GaN region with acceptor traps is considered to be of a constant thickness of 3 μm, while C–Si codoped region is considered to be buried between C-doped regions within this buffer with thickness $t_{Si\text{-}Doped}$, which is located at a depth of $t_{C\text{-}Channel}$ from the top of C-doped GaN buffer. The GaN channel thickness $t_{Channel}$, where neither C-doping nor Si-doping is considered, is kept fixed at 35 nm. As acceptor traps are responsible for restricting leakage through the buffer and Si-doping (donor traps) is responsible for vertical field redistribution in deep GaN buffer, this type of profile is expected to maintain a high V_{BD}, where Si-doped region can be moved further away from the GaN channel to minimize its impact on channel mobility.

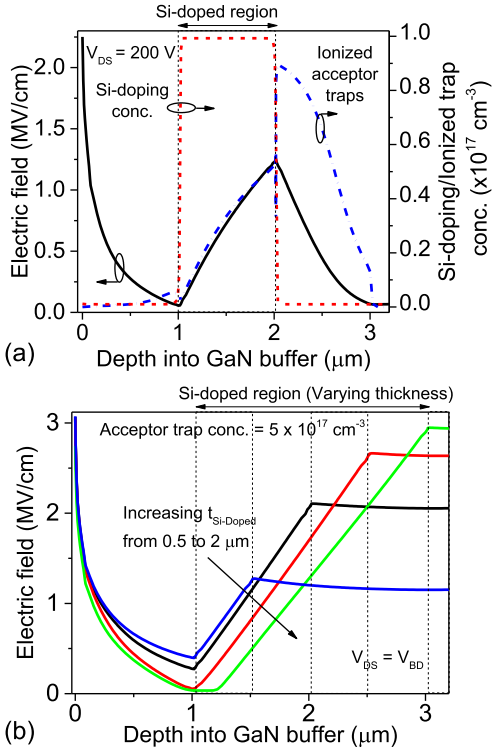

Fig. 12. (a) Vertical electric field under the drain edge plotted together with Si-doping and ionized acceptor trap profile, which collectively define the space-charge profile, extracted for the buffer stack with modified Si-doping profile. (b) Impact of Si-doped region's thickness on vertical electric field profile extracted at the onset of avalanche phenomena. A constant Si-doping concentration of 1×10^{17} cm^{-3} along with an acceptor trap concentration of 5×10^{17} cm^{-3} is considered.

A. Impact on Vertical Electric Field

Fig. 11(b) depicts the impact of modified doping profile on vertical electric field distribution in the GaN buffer. It indicates an increased field redistribution in the deep GaN buffer region, where both acceptor traps and Si-doping were considered, while no such redistribution was observed in the buffer region, where Si-doping was not considered. This kind of field profile can be explained using the ionized acceptor trap concentration and Si-doping profile in the buffer region, which collectively define the space-charge profile. One such profile along with vertical electric field in the GaN buffer extracted at a drain bias voltage of 200 V is shown in Fig. 12(a). In the region where both Si-doping and ionized acceptor traps are present, a significant redistribution of electric field can be observed. It further reveals that within this region, Si-doping dominates the ionized acceptor trap concentration. As Si-doping offers positive charge and ionized acceptor traps contribute to negative charge, this type of profile gives rise to net positive charge in the region with Si-doping. As a result, electric field redistributes in this region, as shown in Fig. 12(a). As this positive charge is limited in the region where Si-doping is considered, electric field redistribution is also restricted to the same region. This can further be observed from Fig. 12(b), where an increase in thickness of Si-doped region ($t_{Si\text{-}Doped}$) results in an increased redistribution of electric field in the deep GaN buffer.

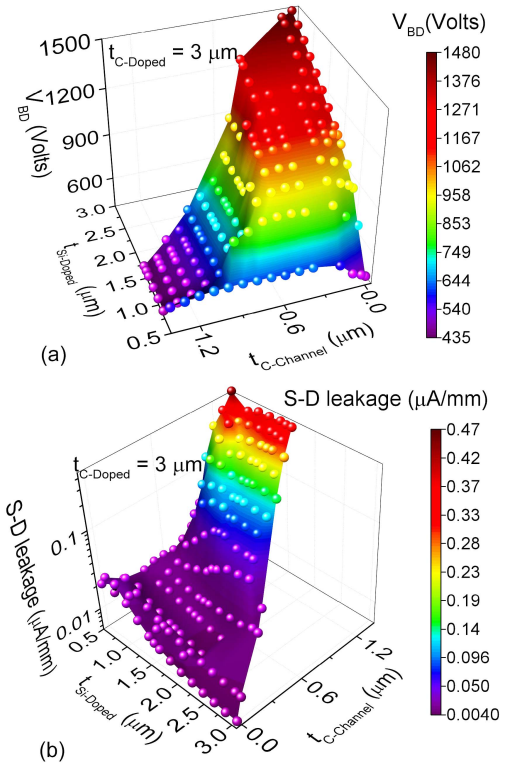

Fig. 13. Impact of channel thickness ($t_{C\text{-}Channel}$) and Si doped region's thickness ($t_{Si\text{-}Doped}$) on (a) breakdown voltage and (b) source/drain leakage current in the device. Acceptor trap concentration of 5×10^{17} cm^{-3} was considered with a Si doping concentration of 2×10^{17} cm^{-3}.

B. Design of Si-Doped Region

The above-mentioned discussion indicates the presence of two primary design parameters: 1) $t_{C\text{-}Channel}$ and 2) $t_{Si\text{-}Doped}$, which can affect V_{BD} as well as leakage current. Fig. 13(a) depicts V_{BD} of the device under influence of these design variables. V_{BD} versus the two design variables show an improvement with increase in $t_{Si\text{-}Doped}$, which is attributed to extended space-charge region deep into the GaN buffer, as presented earlier. It is interesting to note that, independent of the thickness of Si-doped region, V_{BD} does not fall significantly ($\Delta V_{BD} <$ 100 V) when channel region thickness ($t_{C\text{-}Channel}$) was increased up to ~400 nm. Moreover, the source/drain leakage data shown in Fig. 13(b) depict a controlled leakage current when $t_{C\text{-}Channel}$ was increased up to ~400 nm. However, with further increase in channel thickness, leakage current was found to increase exponentially, which adversely affects V_{BD}. This can be attributed to presence of a high concentration of uncompensated acceptor traps in C-doped region without Si-doping, which leads to an increase in leakage current.

C. Comparison With Standard/Uniformly Doped Buffer

From 2DEG performance point of view, it is always desirable to keep the doped region away from the 2DEG, as much as possible. Fig. 14(a) and (b) compares the impact of channel thickness on V_{BD} and leakage current, respectively, under following two stack doping cases: 1) having a uniform acceptor trap as well as Si-doping (or donor trap) concentration in the complete C-doped GaN buffer where $t_{Channel}$ is a design variable and 2) modified doping profile with a fixed

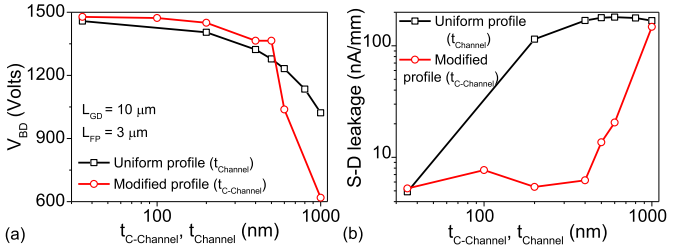

Fig. 14. Comparison of the impact of Si-doping profile on (a) breakdown voltage and (b) leakage current through the device. Acceptor trap concentration and Si-doping concentration are kept as 5×10^{17} cm^{-3} and 2×10^{17} cm^{-3}, respectively.

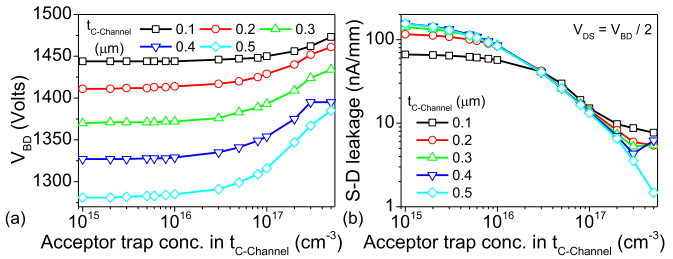

Fig. 15. Impact of acceptor trap concentration in the channel region above the Si-doped region in proposed engineered stack on (a) breakdown voltage of the device and (b) source–drain leakage current extracted at $V_{DS} = V_{BD}/2$. Si doping concentration of 2×10^{17} cm^{-3} is used. Total buffer thickness is kept constant at 3 μm with a $t_{Channel}$ of 35 nm. Lateral dimensions are kept constant as $L_{GD} = 10$ μm and $L_{FP} = 3$ μm.

$t_{Channel}$ of 35 nm where $t_{C\text{-}Channel}$ is the design variable. In both the cases, the total buffer thickness is kept unchanged. Thus, with an increase in $t_{Channel}$, $t_{C\text{-}Doped}$ is reduced to maintain a constant buffer thickness (see Fig. 1). Similarly, with an increase in $t_{C\text{-}Channel}$, $t_{C\text{-}Doped}$ is kept unchanged, whereas $t_{Si\text{-}Doped}$ is reduced to satisfy the relation $t_{C\text{-}Channel} + t_{Si\text{-}Doped} = t_{C\text{-}Doped}$. Fig. 14 suggests a superior breakdown performance and unchanged source/drain leakage in case of modified Si-doping profile for total channel thickness as high as ~500 nm. Leakage current in the case of standard profile increased significantly with a marginal increase in channel thickness. This validates superiority of proposed modified profile over standard profile.

D. Can We Lower the C-Doping With Engineered Profile?

As shown in Fig. 11(a), the modified Si-doping profile leaves a channel region above Si-doped region, where only acceptor traps are assumed (low C-doping and hence negligible donor traps). It was noted in the previous section that the thickness of this channel region can be increased up to ≈500 nm with a marginal reduction (~100 V) in V_{BD}. As majority of vertical field relaxation takes place in the Si-doped region and the acceptor trap concentration in channel region is primarily responsible for controlling the resistivity of GaN buffer, the acceptor trap concentration or C-doping in this region can be further reduced without affecting V_{BD}, however at a marginal compromise of source–drain leakage current. This is depicted in Fig. 15. Here, V_{BD} shows limited reduction with acceptor trap concentration, whereas leakage current increases. The reduction in V_{BD} with increasing channel thickness is

attributed to the reduction in thickness of Si-doped region. On the other hand, the marginal increase in leakage current with reduced acceptor trap or C-doping concentration is due to reduced channel resistivity. Fig. 15 also gives an appropriate design window and doping range for the proposed design.

VI. Conclusion

Doping of GaN buffer with moderate C & Si was found to improve V_{BD} of AlGaN/GaN HEMT devices in the same way when buffer consisted of high acceptor trap concentration and moderate donor trap concentration. While C is primarily the source of acceptor traps in GaN buffer, based on nature of Si-doping, it was proposed to provide additional donor traps in GaN buffer to independently engineer the donor trap profile. This codoping of GaN buffer by C & Si, thus, provides an independent control of the acceptor and donor trap concentration, which increases flexibility in buffer design to achieve maximum possible V_{BD} with minimum possible acceptor trap concentration. This reduced acceptor trap concentration in GaN buffer is expected to improve the dc/RF performance of the device. Finally, a modified Si-doping profile was proposed, which resulted in an improved V_{BD} while simultaneously lowering the acceptor trap concentration (C-doping).

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