Challenges & Physical Insights Into the Design of Fin-Based SCRs and a Novel Fin-SCR for Efficient On-Chip ESD Protection

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***Abstract*— This paper presents the detailed physical insights into the silicon-controlled rectifier (SCR) phenomena in planar equivalent Fin SCR devices. The complexity and roadblocks for SCR triggering in FinFET technology are explored. Implication of contact silicidation on Fin SCR turn-ON is discussed in detail. Device design approaches are discussed for efficient Fin-enabled SCRs. In this direction, a novel contact engineering scheme in Fin technology is disclosed for improved SCR action. Moreover, a novel Fin SCR is presented, which offers area-efficient electrostatic discharge current carrying capability.**

***Index Terms*— Electrostatic discharge (ESD), FinFET, on chip, silicon-controlled rectifier (SCR).**

I. Introduction

IT HAS been over seven years since FinFET-based commercial products were first announced by semiconductor industry. The tremendous pace of CMOS scaling and projected short-channel performance requirements pushed FinFETs to get into the mainstream, which are structurally designed to have an efficient channel control to reduce the OFF-state leakage [1] with least foot print and maximum ON-current per unit area. While FinFETs enjoy lower silicon footprint, these devices, however, become increasingly vulnerable toward overvoltage, self-heating, and electrostatic discharge (ESD) stress due to poorer heat dissipation when compared to its planar counterpart. Having such a technology at disposal, designing wide variety of ESD protection devices has become a major concern [2]–[5]. Reduced ESD design window for FinFET and beyond FinFET technology have posed further difficulty in developing ESD protection elements in FinFET technology [6]–[12], causing Fin-based ICs to be increasingly susceptible to ESD events [13]–[16]. This is one of the reasons why FinFET technology is mostly filling the high-performance computing and digital baseband-like product needs, to begin with. Developing a system-on-chip is still a long shot, attributed to missing variety of ESD protection devices, beside high-voltage capability.

Silicon-controlled rectifiers (SCRs) have widely been used as an efficient ESD protection device for low-voltage applications, owing to their low parasitic loading effects, relatively smaller device footprint area, lower holding voltage, and faster turn-ON [18]–[27]. With the principle of regenerative positive feedback under ESD, such as high current injection event, SCR stands as a desirable ESD protection element when compared to ggnMOS or diodes. While often the fundamental concepts for device designs are borrowed from its previous nodes, adapting the planar-like conventional SCR design approach for FinFET technology presents numerous design challenges [28], [29]. It was reported that SCR device designs from planar counterparts could not be borrowed successfully for the Fin-based SCR devices due to the lack of reproducible SCR-like action [29].

In this paper, fundamental roadblock and physical phenomena associated with Fin-based SCR designs have been studied using 3-D device TCAD. Furthermore, Section II presents the physical insights into the missing SCR action in FinFET technology. With the corresponding findings, Section III discusses the design challenges and engineering approaches toward efficient SCR mechanism. Having explored the physical insights of fin-based bottlenecks and techniques to redesign conventional Fin SCR (CFSCR), a novel dual-Fin SCR (DFSCR) is introduced in Section IV, as an efficient ESD protection element, which provides an area efficient solution with a well-distributed current conduction mechanism. Finally, Section V concludes the new findings and proposed design rules for an efficient SCR for FinFET technology.

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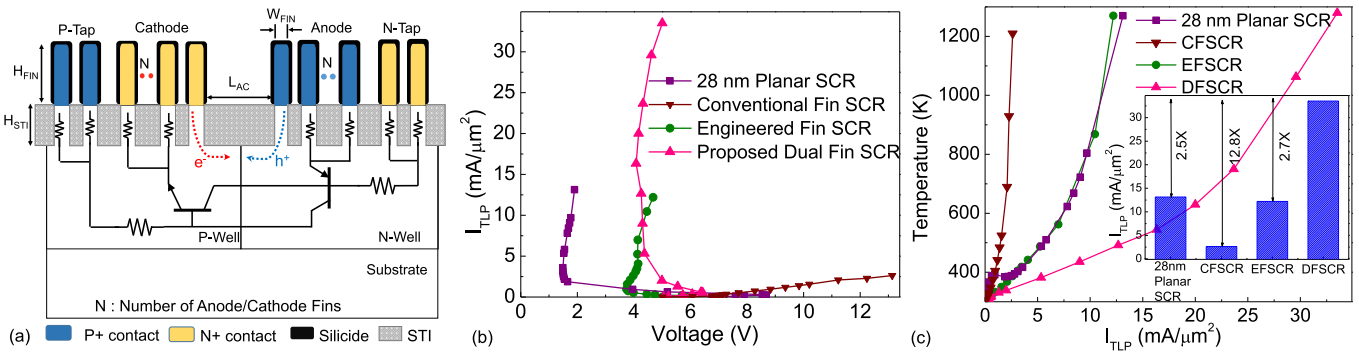

Fig. 1. (a) Planar equivalent of CFSCR. (b) TLP I–V characteristics of CFSCR, EFSCR, and proposed DFSCR. (c) Self-Heating: Lattice temperature versus I_{TLP} of CFSCR, EFSCR, and proposed DFSCR, extracted using 3-D TCAD simulations. Inset of (c) compares the ESD robustness (It2) of the CFSCR with the proposed DFSCR and EFSCR, respectively [17].

II. FinFET SCRs: A Brief Outlook

On account of a low holding voltage (V_{Hold}), high failure current (It2) and an excellent ON-resistance (R_{ON}), SCR devices serve as an efficient ESD protection element. However, the translation of this planar-based SCR ESD protection concept to FinFET technology presents many design-specific challenges, which alters the ESD relevant metrics of the SCR, such as snapback, low V_{Hold}, desirable It2, and R_{ON}. Fig. 1(a) illustrates the schematic of the planar equivalent CFSCR with the anode, cathode, and n/p triggering taps/fins. The n+ or p+ fins are fully silicided at the fin surface and are used to contact the n-/p-wells (base–collector taps) with the respective emitters. Throughout this paper, the number of fins used in n/p tap region is designed, such that the number of N/P tap fins to anode/cathode fins (N) ratio is 0.6. This ratio is considered to mimic the approximate length ratio of n/p tap to anode/cathode length of that of planar SCR, to have a conservative comparison. This design is also compared with a 28-nm technology equivalent planar SCR device, an engineered Fin SCR (EFSCR) device, and a newly proposed DFSCR device. The idea behind EFSCR and DFSCR architectures are revealed in later sections. It is worth highlighting that Transmission Line Pulse (TLP) I–V characteristics of various SCR devices explored in this paper have been extracted using 3-D device TCAD simulations [30]. The TCAD simulation deck for SCR is well-calibrated with experimental FinFET results [31] using appropriate fin aspect ratio and TCAD models, as explained in our earlier works [32], [33]. To account for self-heating effects under ESD stress condition, thermal boundary conditions are taken into consideration, as reported in [34], beside incorporating thermal resistance equivalent to back-end metal interconnect and interlayer dielectric. State-of-the-art TLP I–V extraction methodology was used with 100-ns pulsewidth with increasing amplitude after each pulse with a rise time of 10 ns. An averaging window of 60–80 ns was adopted to extract the individual I–V points in the TLP I–V curve. The failure criteria (It2) for all the devices were considered with a conservative estimate of temperature exceeding 1200 K. This is in accordance with an earlier failure analysis work on FinFETs [3]. For all investigations, H_{FIN}, H_{STI}, and W_{FIN} were considered to be 42, 70, and 8 nm, respectively.

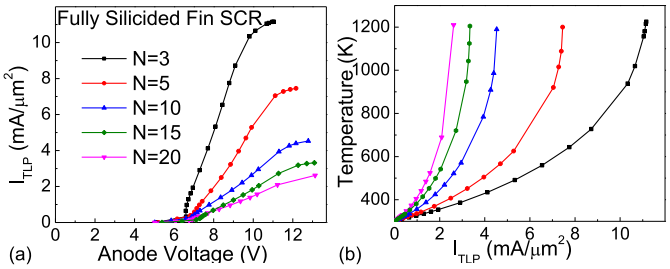

Fig. 2. (a) TLP I–V characteristics and (b) lattice temperature versus I_{TLP} characteristics of fully silicided CFSCR as a function of number of anode/cathode Fins (N).

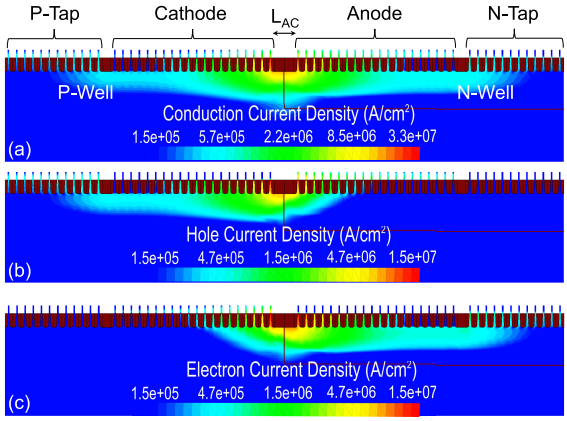

Fig. 3. (a) Total current density, (b) hole current density, and (c) electron current density across a fully silicided CFSCR, extracted at 50% of It2 [17].

The anode/cathode/tap doping was chosen as 1×10^{21} cm^{-3}; however, the p-/n-well doping was selected to be 5×10^{18} cm^{-3}. To encapsulate the real-time heat dissipation, an equivalent thermal resistance of 1-μm copper metal was defined over the anode/cathode/tap terminals. All the characteristics were extracted considering negligible contact resistance due to the degenerate doping of the anode/cathode/tap regions. Adding external contact resistance at the terminals affects the R_{ON} of the device without inducing significant effect on the intrinsic device parasitics.

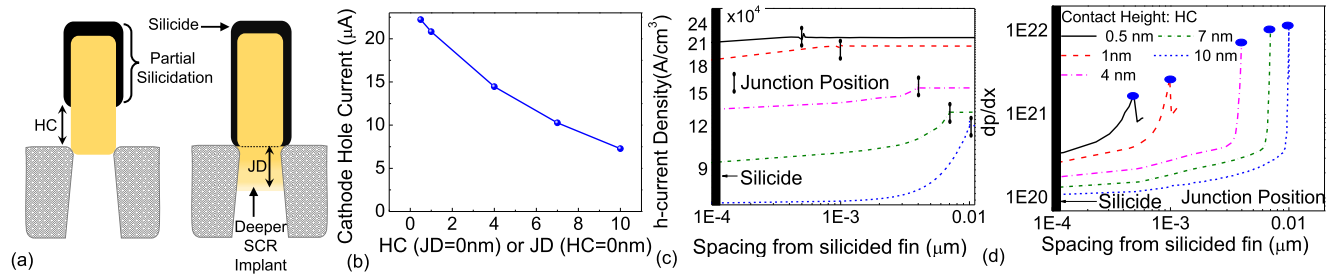

Fig. 4. (a) Fin schematic depicting contact and junction engineering schemes. CFSCR has HC = JD = 0 nm [see Fig. 1(a)]. (b) Cathode (or emitter) hole current versus HC or JD. (c) Hole current density and (d) hole density gradient (dp/dx) as a function of spacing from the silicided fin.

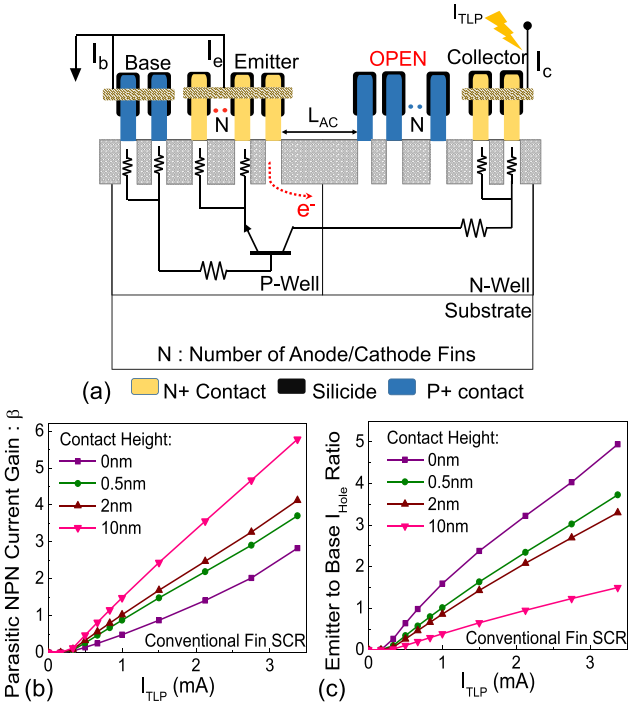

Fig. 5. (a) Cross-sectional view depicting the parasitic n-p-n device of the planar equivalent Fin SCR. (b) Current gain (β) as a function of injected collector current. (c) Emitter-to-base hole current ratio as a function of pulsed collector current.

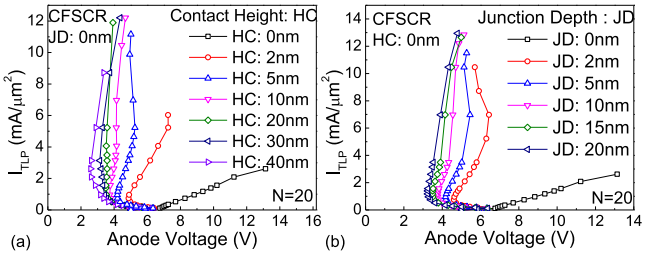

Fig. 6. TLP I–V characteristics of CFSCR with varying (a) HC (JD = 0) and (b) JD (HC = 0). Here, the number of anode/cathode fins, $N = 20$.

Fig. 1(b) depicts the simulated TLP I–V characteristics of various SCR designs, briefly mentioned earlier. It depicts absence of regenerative snapback in the CFSCR, which reveals a missing SCR action leading to higher holding voltage and a very low It2. In order to demonstrate a fair comparison

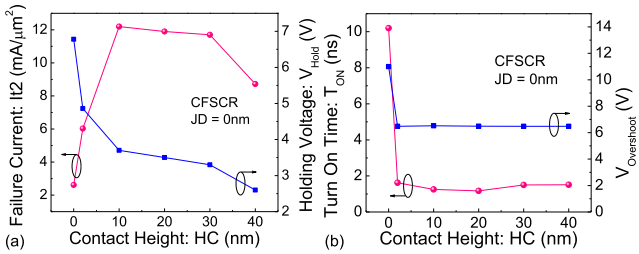

Fig. 7. (a) Failure current (It2) and holding voltage (V_{Hold}) and (b) turn-ON time (T_{ON}) and voltage overshoot ($V_{Overshoot}$) as a function of spacing between contact silicidation and base–emitter junction (HC) for JD = 0 nm. These trends were extracted at an injected stress current equivalent to 90% of the respective It2.

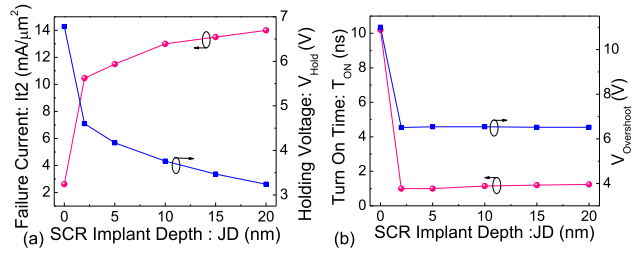

Fig. 8. (a) Failure current (It2) and holding voltage (V_{Hold}) and (b) turn-ON time (T_{ON}) and voltage overshoot ($V_{Overshoot}$) as a function of diffusion depth below active Fin (JD) for HC = 0 nm. These trends were extracted at injected stress current equivalent to 90% of the respective It2.

between 2-D (planar) and 3-D nature of the various SCR designs, the stress currents are normalized per unit layout area. The following sections present the underlying phenomena leading to the missing SCR action in conventional-/planar-based Fin topology and ways to mitigate Fin-based SCR design challenges. The corresponding findings are used to reengineer the CFSCR design and propose a novel DFSCR design [see Fig. 1(b)], providing a 13× improvement in layout efficiency in terms of failure current per unit area, beside significant improvement in holding voltage and ON-resistance of these SCR devices.

III. Fin SCRs: Design Challenges and Engineering

As discussed earlier, the CFSCR does not exhibit an SCR action (or first snapback), as depicted in Fig. 1(b), which is further elaborated in Fig. 2, as a function of number of

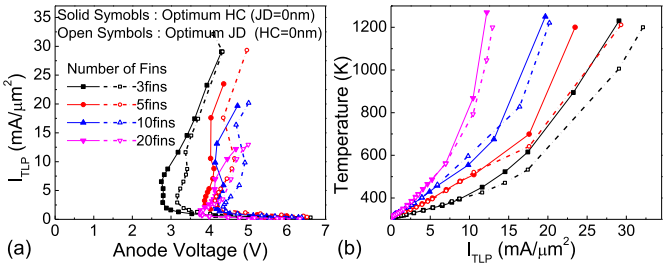

Fig. 9. (a) TLP *I–V* characteristics and (b) lattice temperature versus I_{TLP} characteristics of partially silicided Fin SCR device for both optimum HC and optimum JD, as a function of number of anode/cathode fins (N).

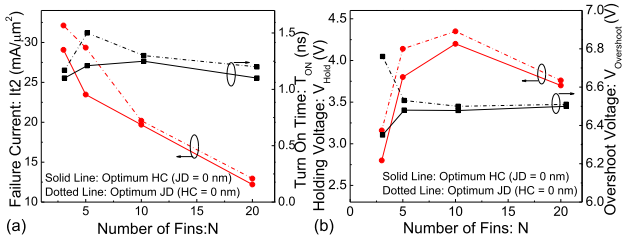

Fig. 10. (a) Failure current (It2) and turn-ON time (T_{ON}) and (b) holding voltage (V_{Hold}) and voltage overshoot ($V_{Overshoot}$) as a function of number of fins (N) for partially silicided Fin SCR device.

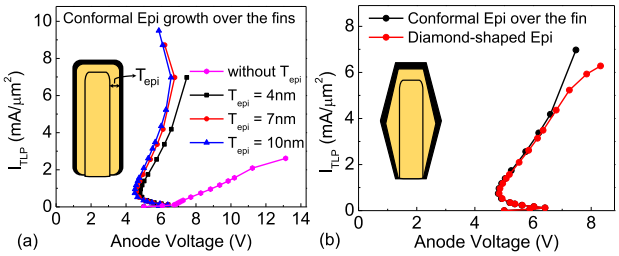

Fig. 11. (a) TLP *I–V* characteristics of CFSCR with the incorporation of a conformal epitaxial silicon layer over the fins (shown in inset) as a function of epi layer thickness (T_{epi}). (b) TLP *I–V* characteristics of CFSCR with conformal and diamond-shaped epi-growth over the fins (shown in inset).

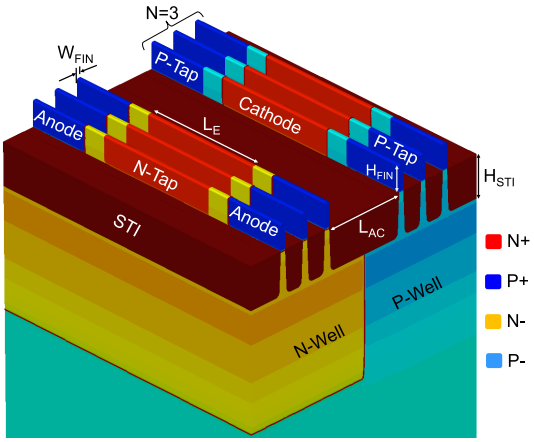

Fig. 12. 3-D architectural view of the proposed DFSCR design. The active Fin regions consist of anode/cathode and n-/p-taps, which forms a junction or contact with the respective n-/p-wells [17].

anode/cathode fins (N). Fig. 2 demonstrates the TLP *I–V* characteristics of CFSCR with increasing N, and it can be seen that, as N increases, the It2 per unit area lowers, and it does not affect the SCR action. The possible explanation for this is the weak parasitic bipolar, which can be attributed to an increased emitter resistance due to the Fin shape or increased carrier recombination in the base region due to relatively higher doping in FinFET's n-/p-wells. However, detailed TCAD analysis revealed that none of these were responsible for the missing SCR action or weaker bipolar action in CFSCRs. Fig. 3(a) shows the total conduction current density for CFSCR (considering $N = 20$), where the major current carrying regions are anode and cathode terminals, which is consistent with the traditional understanding of current transport across SCR device [20]. Fig. 3(b) and (c) depicts the respective minority carrier current conduction (electron and hole) across CFSCR. It has been found that unlike in planar SCRs, a significant portion of minority carrier current flows through the respective cathode/anode contacts, which are the emitter contacts of the Fin SCR, i.e., a significant hole current through the cathode contact and an electron current through the anode contact. This minority hole (electron) conduction through the parasitic n-p-n (p-n-p) emitter contact is expected to dominate through p (n)-Tap to trigger the SCR. The weaker bipolar action in CFSCR can then be explained due to the significant loss of minority carriers through the emitter contacts. The high minority carrier conduction through emitter contacts is due to fully silicided nature of Fins, which is elaborated in Fig. 4. Fig. 4(a) shows single-Fin schematic, depicting parameters contact height (HC) or junction depth (JD) to study the impact of spacing between silicided portion of the Fin and base–emitter junction. The HC is defined as the height from the base of the fin, above which the fin is fully silicided. This refers to contact silicidation from the base of the fin up to a desired height. The JD can be defined as the diffusion depth of the emitters, beneath the active region of the fin. In case of conventional (fully silicided) Fin SCR, HC = 0 and JD = 0, Fig. 4(b) depicts the gradual reduction in minority carrier conduction through the emitter contact, as HC was increased from 0 to 10 nm (keeping JD = 0 nm) or when JD was increased from 0 to 10 nm (keeping HC = 0 nm). This is plotted as a decrease in the minority hole current through the emitter cathode contact for the n-p-n parasitic bipolar. This is attributed to the minority carrier diffusion current [see Fig. 4(c)], which is a strong function of the minority carrier gradient between junction and the contact as

$$J_P = q.D_p \frac{dp}{dx}. \tag{1}$$

In theory, for HC = JD = 0, $dx \to 0$ and, hence, $dp/dx \to \infty$. Extrapolating this to the situation when contact was placed next to the vertical junction in case of fully silicided Fin, it resulted in significantly higher carrier gradient [see Fig. 4(d)] and minority carrier conduction through emitter (anode/cathode) contacts. This can also be observed from Fig. 4(b), which depicted highest minority hole current through the cathode (or emitter) for HC = 0 and JD = 0. This can be relaxed by keeping the silicided region away from the junction, either by increasing HC or by increasing JD, which is found

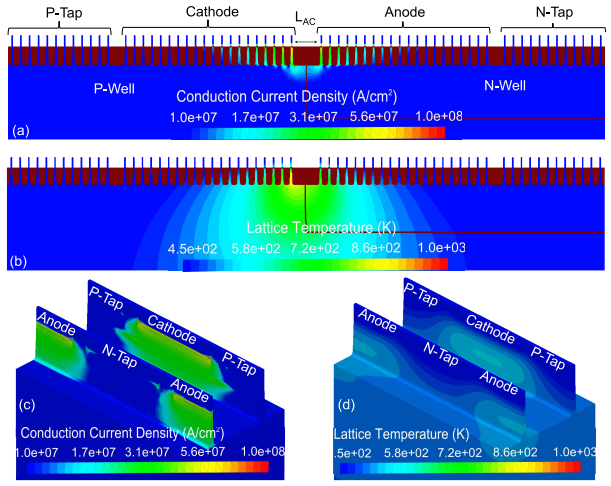

Fig. 13. Conduction current density and lattice temperature profiles of (a) and (b) CFSCR and (c) and (d) DFSCR, respectively, extracted for $I_{TLP} = 2.3$ mA/μm^2.

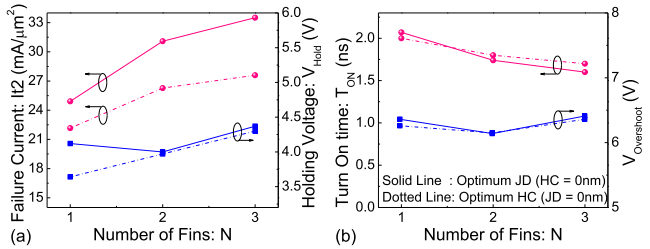

Fig. 14. (a) Failure current (It2) and holding voltage (V_{Hold}) and (b) turn-ON time (T_{ON}) and voltage overshoot ($V_{Overshoot}$) as a function of number of Fins (N) over the n-/p-wells in DFSCR. These trends were extracted using 3-D TCAD simulation at injected stress current equivalent to 90% of the respective It2.

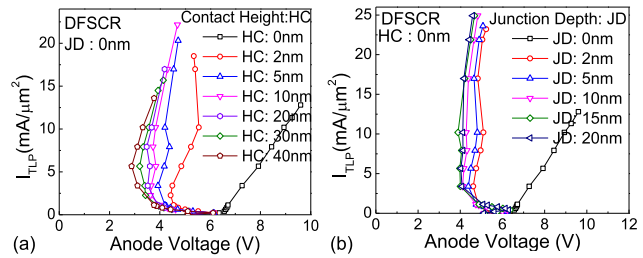

Fig. 15. TLP I–V characteristics of DFSCR with varying (a) HC (JD = 0) and (b) JD (HC = 0). Here, the number of anode/cathode fins, $N = 1$.

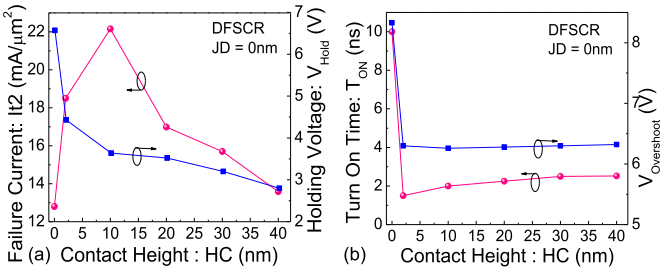

Fig. 16. (a) Failure current (It2) and holding voltage (V_{Hold}) and (b) turn-ON time (T_{ON}) and voltage overshoot ($V_{Overshoot}$) as a function of HC in DFSCR.

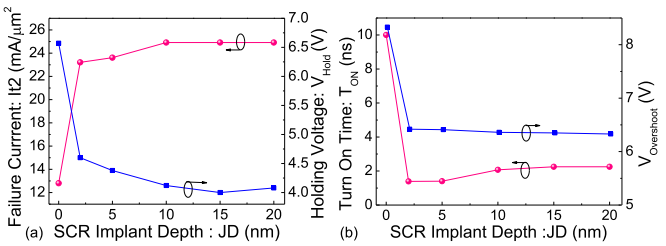

Fig. 17. (a) Failure current (It2) and holding voltage (V_{Hold}) and (b) turn-ON time (T_{ON}) and voltage overshoot ($V_{Overshoot}$) as a function of JD in DFSCR.

to improve the parasitic bipolar action. Similar improvement in bipolar efficiency for planar nMOS devices was earlier experimentally validated with thin S/D salicides [16]. Fig. 5(a) depicts a scheme using which, the efficiency of the parasitic n-p-n bipolar was studied, where the anode contact was left open, the p-tap and cathode were grounded and the n-tap was stressed. It can be observed that as the spacing between silicided portion of the Fin and base-emitter junction was increased, the bipolar gain (β) was found to increase [see Fig. 5(b)], which is attributed to the reduced emitter-to-base hole current ratio [see Fig. 5(c)]. This results in an efficient SCR action, which manifests as a deep snapback in the TLP I–V characteristics, further illustrated in Fig. 6, where an SCR action is clearly visible for HC $>$ 2 nm or JD $>$ 2 nm. Similar improvement in the parasitic bipolar efficiency with the increase in HC was observed for dc simulations, as well. An important point to highlight here is that the SCR action (or efficient bipolar action) for FinFET technology can be improved by separating the contact (or silicide) from the junction by either lifting the silicide up from the base of the fin (increasing HC) or by diffusing the emitter deeper (increasing JD).

Figs. 7 and 8 further depict the impact of contact separation from the junction by increasing HC and JD, respectively, on the ESD figure-of-merit parameters of SCR device, such as It2, V_{Hold}, turn-ON time (T_{ON}), and overshoot voltage ($V_{Overshoot}$). The trends were extracted for injected stress current equivalent to 90% of the respective It2. As HC or JD was increased, SCR's failure current and turn-ON time were found to improve by an order of magnitude. Similarly, holding voltage and voltage overshoot was found to scale by a factor of 3 and 2, respectively, [V_{Hold} drops from 7 to 3 V, and $V_{Overshoot}$ drops from 11 to 6.5 V in Fig. 8]. It should be noted that normalized It2 per layout area drops and then saturates after an optimum value of HC or JD = 10 nm. This is attributed to the increased thermal resistance between S/D Fins and contact with increase in HC and/or JD, which enhances the lattice heating and resulting device failure. Given that most of the thermal energy from FinFET channel is taken away by the Back End of Line metallization via S/D contacts [35], any change in contact scheme is prone to affect the self-heating behavior of the FinFET devices. With increasing HC or JC, the silicided region is moved away from hot spot, which adds to the thermal resistance mentioned. Therefore, from Figs. 7 and 8, it can be stated that the CFSCR can be engineered

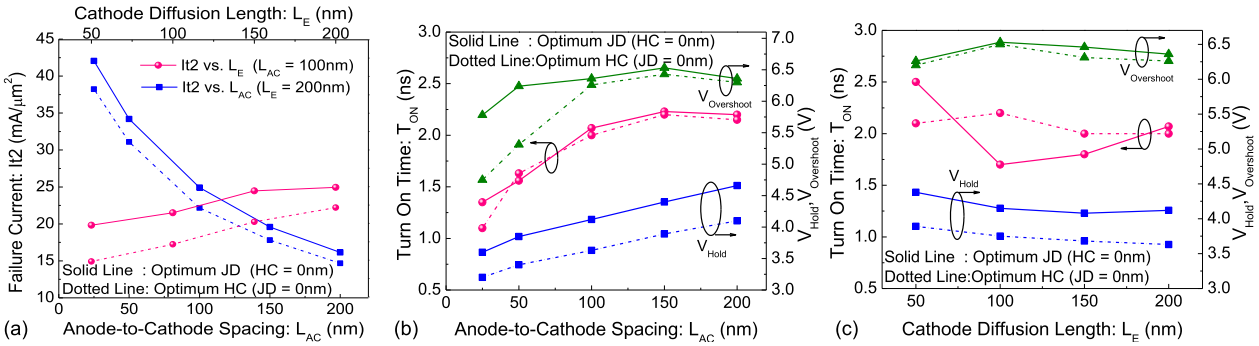

Fig. 18. (a) Failure current (It2), holding voltage (V_{Hold}), turn-ON time (T_{ON}) and voltage overshoot ($V_{Overshoot}$) as a function of (b) anode-to-cathode spacing (L_{ac}) and (c) anode/cathode diffusion length (L_E), as shown in Fig. 12, depicting improved design scalability for DFSCR. The respective trends were extracted using 3-D TCAD simulation at an injected stress current equivalent to 90% of the respective It2.

with HC = 10 nm (keeping JD = 0 nm) or JD = 10 nm (keeping HC = 0 nm) to offer optimum performance as an SCR ESD protection device, which is termed as EFSCR device in this paper. This value for the optimum HC and JD shall be used in the subsequent investigations too.

Fig. 9 demonstrates the TLP characteristics for the EFSCR with HC = 10 nm (JD = 0 nm) and with JD = 10 nm (HC = 0 nm), as a function of number of anode/cathode fins (N). With the contact and junction engineering scheme, an efficient SCR action is evident from deep snapback in the TLP I–V graph. It is also worth highlighting that the EFSCR exhibits reduced failure current per layout area with the increase in the number of anode/cathode fins. This is because It2 per unit device width does not increase linearly with increasing number of anode/cathode Fins, which is due to nonuniform current contributions from anode/cathode Fins. Fins that are close to well junction contribute to higher SCR current, which falls as one moves away from well junction. Attributed to this reduced current contribution while moving away from junction, It2 per unit area falls beyond an optimum value of 3 Fins. This trend is found to be similar to the CFSCR devices, as depicted in Fig. 2. Fig. 10 further illustrates the effect of the number of anode/cathode fins on the ESD relevant metrics for the partially silicided Fin-SCR. It can be observed that the turn-ON time and the overshoot characteristics do not get affected with the increase in the number of anode/cathode fins. However, the holding voltage (V_{Hold}) reaches a peak at $N = 10$ and is seen to roll off at higher values of N. With the increase in the number of fins, the current density drops, and hence, it requires an increased number of minority carriers to sustain the bipolar action, which leads to an increase in V_{Hold}. Furthermore, as the number of fins is increased, the emitter junction area increases, which improves the emitter injection efficiency and allows the bipolar action to be maintained even at slightly lower holding voltages. Hence, the number of anode/cathode Fins in FinFET SCRs can be used as a design knob to tune the holding voltage, as per the design requirement.

To summarize, so far we have shown that for efficient SCR action in FinFET-based ESD protection devices, the efficiency of the parasitic bipolar needs to be improved, which is achieved by separating the contact silicide and the drain-well junction. This was found to mitigate the minority carrier

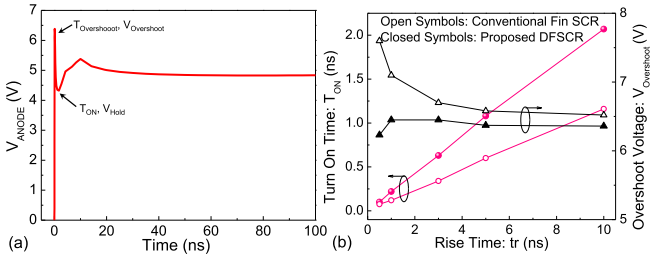

Fig. 19. (a) Anode voltage versus stress time for DFSCR, depicting the extraction of T_{ON}. (b) Transient figure-of-merit comparison (T_{ON} and $V_{Overshoot}$) of EFSCR and DFSCR as a function of pulse rise time, extracted for optimum JD. These trends were extracted using 3-D TCAD simulation at an injected stress current equivalent to 90% of the respective It2.

loss through the emitter contacts, which can be achieved by either increasing HC (i.e., moving silicide region vertically) or increasing JD (pushing the anode/cathode regions deeper into the n-/p-wells). Fig. 11 proposes and depicts another approach to disjoint the p-n junction from the silicide by incorporating an epitaxial layer over the fins before the metal silicidation process. With the epitaxial growth over the fins, the contact silicidation at the base of the fin may not be present. This phenomena act as a raised contact metallization case. The epitaxial layer can be a conformal growth all over the fins, leading to a rectangular epitaxy profile or a diamond-like epitaxy over the fins. Fig. 11(a) depicts the TLP I–V characteristics of the CFSCR with increasing thickness of a conformal epitaxial layer of silicon (with thickness T_{epi}) all over the active-fin region. As depicted, the SCR action is improved with increasing epi thickness, attributed to the physics explained earlier while increasing JD or HC. Fig. 11(b) presents the TLP I–V comparison of CFSCR with conformal and diamond-shaped epitaxy over the fins. It is worth highlighting that no significant change is observed in the TLP characteristics, which demonstrates the independence of the behavior of the parasitic bipolar with the shape of the epitaxial growth over the fins.

IV. Novel Dual Fin SCR

The previous section demonstrated the physical insights and ways to overcome the challenges associated in designing efficient FinFET SCR ESD protection devices. This section presents a novel DFSCR design to further improve the layout

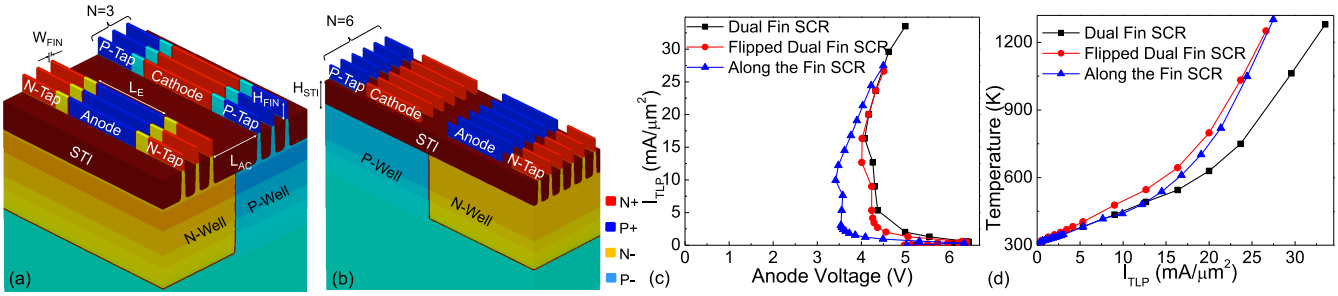

Fig. 20. 3-D architectural view of (a) Flipped DFSCR with adjacent anode/cathode regions, (b) along the Fin-SCR, where the anode/cathode and tap regions are placed on the same group of fins, and (c) and (d) TLP I–V and lattice temperature versus I_{TLP} characteristics of DFSCR, Flipped version of DFSCR (or nondiagonal DFSCR), and along the Fin SCR, respectively.

efficiency of these protection elements. Fig. 12 depicts the proposed DFSCR design, which consists of two groups of fins separately placed in n- and p-wells. Here, each group may have one or more number of Fins (N). n-/p-taps are placed on both the sides of anode/cathode. Note that the anode and cathode diffusions are intentionally placed diagonal to each other. This permits uniform current spreading and, therefore, lowers the current density for a given absolute anode-to-cathode current, which further helps in relaxing the heat dissipation across the device and improves failure current per unit area [Fig. 1(b) and (c)] [17]. This is also depicted in Fig. 13, which shows relaxed lattice temperature for DFSCR, as compared to the CFSCR architecture. The proposed DFSCR device can easily be used in cell-based geometry to minimize its overall footprint.

Fig. 14 plots the ESD relevant parameters for SCR device for DFSCR as a function of number of anode/cathode fins (N). It shows that increasing number of Fins in a given group improves the overall area efficiency of the device without sacrificing the turn-ON or holding voltage characteristics. Comparing with the optimum EFSCR [see Figs. 7 and 8], the proposed DFSCR device offers 3× higher It2 per unit area. The same concept for separating the contact from the junction by increasing HC or JD can be implied in DFSCR. Fig. 15 summarizes the TLP I–V results for DFSCR with increasing HC and JD. As discussed in the previous section, with the increase in the contact and junction separation, the bipolar efficiency improves, leading to a snapback in the I–V characteristics. This is attributed to the reduction in the minority carrier current through the emitter regions. Figs. 16 and 17 depict the variation of the ESD figure-of-merit parameters with HC and JD, respectively. Similar to EFSCR, the proposed DFSCR also exhibits improved SCR action when HC and JD were increased above 2 nm, which validates the design challenges and proposed solutions in the previous section. However, unlike EFSCR, DFSCR with optimum JD exhibits higher failure threshold than the same with optimum HC, which validates the presence of efficient current spreading in the proposed device compared to planar equivalent design.

Fig. 18 illustrates the design scalability of the proposed DFSCR. Fig. 18(a) shows 20% improvement in failure current per unit area when cathode diffusion length (L_E) was increased by 4×. This can be achieved without sacrificing transient performance, as depicted in Fig. 18(c). By scaling the anode-to-cathode spacing (L_{ac}) by 4×, It2 per unit area was found to improve by 3× with 25% reduction in holding voltage, 25% reduction in voltage overshoot, and 2× faster turn-ON. This was found to achieve without sacrificing the OFF-state leakage. Similar design feasibility was missing in the conventional designs. The transient performance metrics of the EFSCR and DFSCR are compared as a function of pulse rise time, for optimum JD, as depicted in Fig. 19. Here, the turn-ON time (T_{ON}) is extracted as the time when the voltage achieves a minimum holding state [see Fig. 19(a)]. DFSCR offers lower voltage overshoot at shorter rise times (tr < 2 ns, emulating the vf-TLP conditions), without compromising with the turn-ON time, when compared to EFSCR. This is attributed to the smaller design foot print area (lower capacitance) and improved current-spreading characteristics in the proposed DFSCR. Similar trends were also observed for optimum HC design too. This affirms an area efficient ESD robustness of DFSCR when compared to EFSCR.

So far, the planar SCR is compared with the Fin-based SCR (EFSCR and DFSCR), where DFSCR depicts relaxed lattice temperatures and higher ESD robustness. An obvious question regarding this is whether the It2 improvement is due to the diagonal placement of anode/cathode in DFSCR or some other phenomenon. To quantify this, the TLP results with diagonally placed anode/cathode contacts (see Fig. 12) are compared with a Flipped version of DFSCR with anode/cathode regions facing toward each other [see Fig. 20(a)] and an "Along the Fin-SCR," where the anode/cathode and the tap regions are all placed along the same group of fins [see Fig. 20(b)]. The TLP I–V and lattice temperature comparison of these variants plotted in Fig. 20(c) and (d) clearly depict that while a diagonal placement offers similar I–V characteristics as other variants, the It2 for the case of diagonal DFSCR is 20% higher than the other design architectures, attributed to relaxed self-heating, depicted in Fig. 20(d). This difference is ascribed to the way the majority current carrying regions are placed in the device. In the Flipped DFSCR, the anode/cathode diffusions are placed adjacent to each other; however, in the diagonal configuration, the current effectively spreads across the entire active device, thereby relaxing the lattice heating, which eventually leads to increased ESD robustness of DFSCR.

V. Conclusion

In this paper, we revealed physical insights into the missing SCR action in planar equivalent CFSCR devices. The fundamental reason for the weak parasitic bipolar and missing SCR

action was found to be the excess minority carrier conduction through the anode/cathode contacts in CFSCR device. This was attributed to the fully silicided nature of the Fins, which gives rise to minority carrier diffusion current through parasitic bipolar's emitter–base junction. This was avoided by: 1) pushing the silicided region away from the junction by introducing partial silicidation (HC) or 2) pushing the junction away from the silicided portion by introducing an SCR implant (JD). The same can also be achieved by incorporating an epitaxial layer of silicon grown over the emitter contacts. This resumed the SCR action with significantly improved performance. Finally, the novel DFSCR design is proposed, which allows uniform current spreading, better design scalability, and relaxed heat dissipation across the device. Attributed to this, the proposed design offers 3× higher failure current per unit area and 35% lower voltage overshoot without compromising with turn-ON time when compared to EFSCR device. This efficient diagonal anode/cathode placement in DFSCR accounts for 20% increase in It2 when compared to other nondiagonal Flipped DFSCR and along the Fin-SCR variants.

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