Part II: RF, ESD, HCI, SOA, and Self Heating Concerns in LDMOS Devices Versus Quasi-Saturation

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***Abstract*— Various LDMOS device design parameters to mitigate quasi-saturation (QS) have been identified. Based on this, a set of independent and mixed device designs to mitigate QS, while maximizing the device performance, are presented. The impact of QS on the analog/RF/switching performance of these independent and mixed designs is investigated thoroughly, while analogizing performance with QS for the first time. Furthermore, hot carrier induced (HCI) degradation in various independent and mixed LDMOS designs is studied using spherical harmonic expansion of Boltzmann transport equation. In addition to this self-heating behavior, safe operating area (SOA) boundaries and electrostatic discharge (ESD) behavior of independent and mixed LDMOS designs with and without QS are studied. For the first time, HCI degradation, self-heating behavior, SOA boundary, and ESD failure in LDMOS devices are correlated with the extent of QS in LDMOS devices, based on which device design guidelines to tackle all performance versus reliability challenges are derived.**

***Index Terms*— DeMOS, electrostatic discharge (ESD), hot carrier induced (HCI), LDMOS, quasi-saturation (QS), reliability, spherical harmonic expansion (SHE), safe operating area (SOA).**

I. Introduction

NEVER ceasing demand for scaling automotive and CMOS technologies to improve the performance and cost has imposed limitations on the breakdown voltage of integrated power/high-voltage devices. However, the peripheral operating voltages have not scaled down at a similar pace. Similarly, the power and frequency requirements of integrated power management modules and RF power amplifiers have increasingly become a challenge. As discussed in Part-I of this paper [1], quasi-saturation (QS) is a fundamental challenge with such devices, which becomes severe as the breakdown voltage rating increases [2]–[8]. Earlier studies on design optimization of LDMOS devices for RF power amplifier applications, e.g., Muller *et al.* [9], have presented layout optimization of the source side p-body contact and gate silicidation to reduce the parasitic capacitance in order to boost the transit frequency. However, effects attributed to QS, like g_m and R_o roll-off, which seriously affect the transit frequency (f_t), were not considered in earlier works. In addition to this, self-heating in integrated LDMOS devices, under high-power operations, is another major challenge, which can only be mitigated by appropriate thermal codesign, but not avoided [10]. In particular, self-heating in correlation with QS, which leads to high field and current crowding across the device, was never investigated before.

Hot carrier induced (HCI) degradation and gate oxide reliability add another dimension to the design challenges for these integrated power/high-voltage devices [11], which further restricts the operating voltage. Some of the earlier works presented higher sensitivity of LDMOS devices toward ON- and OFF-state hot carrier stress [12]–[16], which degrades analog/RF FOM parameters in ON state or leads to dielectric breakdown in OFF state. Drift region engineering, overlap and extension region design, layout, and drain ring optimization was later suggested for mitigating HCI degradation and failure [17]–[19]. However, no work until date has correlated QS with HCI degradation. In addition to HCI, integrated LDMOS devices are highly fragile and prone to safe operating area (SOA) concerns and electrostatic discharge (ESD) failures [20]–[22]. SOA depends on the duration of stress, voltage across the device, and injected current [23], which lead to the classification of thermal and electrical SOA. Podgaynaya *et al.* [24] mentioned that circular geometry would reduce the current density and eventually can widen the SOA. More often, a buried layer, or in general base resistance engineering, is highly appreciated to subsidize the parasitic bipolar triggering, which in turn is often believed to improve SOA [12]. Though a number of articles have addresses SOA and ESD issues, these have never been studied in context of QS.

These voltage driven inconsistencies at the I/O interfaces, high-power requirements, and tighter performance-reliability design window bring forth the requirement of device-circuit codesigned devices for integrated I/O, dc–dc, and RF PA applications [16], [25]–[30]. Realizing a well-designed transistor, which can meet the performance (I/O switching and RF) specifications and is robust enough to sustain high voltage (HCI)—high current (ESD) stress, while keeping in

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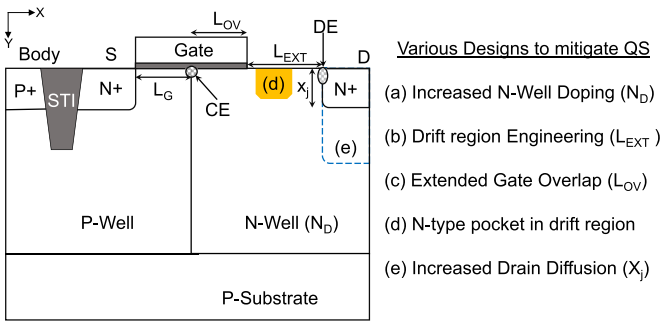

Fig. 1. Schematic of LDMOS device ($L_G = 200$ nm) depicting various designs and respective parameters to mitigate QS behavior. (a) Higher n-well doping compared with the optimum device. (b) Additional extention of the drift region when compared to optimum design. (c) Engineered overlap region to mitigate QS. Here, optimum design is the standard design, which was designed for best breakdown voltage versus ON-resistance tradeoff. (d) Additional n-type pocket/Island introduced to the optimum design. (e) Deeper drain diffusion introduced to the optimum design ($x_j = 100$–300 nm).

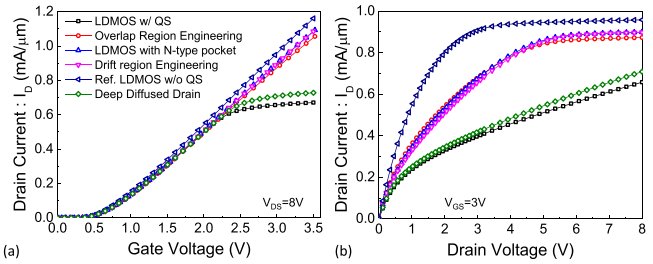

Fig. 2. (a) I_{DS} versus V_{GS} and (b) I_{DS} versus V_{DS} characteristics of LDMOS with QS as well as modified LDMOS designs with mitigated QS effect.

mind QS and self-heating like fundamental issues, is a challenge. However, not much work have been reported until date considering all the aspects together. Device engineering to address one concern often trades off through the other aspects. For instance, overlap and drain extension engineering might help in reducing HCI degradation but are very sensitive to QS and device linearity, which affects the RF performance. The buried layer may suppress the parasitic bipolar action; however, cannot avoid filament formation under high current injection conditions. At this stage, it would not be an exaggeration to say that a device design study up to the extent presented in this paper, while correlating various design and reliability challenges with QS is largely missing in the scientific literature.

While looking extensively into the physics of QS by using Synopsys Device TCAD suit [31], the design and reliability studies presented in this paper are classified as follows. Fig. 1 lists out different device design parameters, carried from Part-I of this paper, to mitigate QS. Through these parameters, a set of independent and mixed device designs are qualified/identified to eliminate QS while maximizing switching, RF, and analog performance, which is presented in Sections II and III. In principle switching, RF and analog figures of merit (FoMs) are correlated with QS. Section IV presents simulated hot carrier behavior of these designs and highlights importance of QS mitigation to reduce HCI degradation. Similarly, Section V compares self-heating behavior and addressed SOA and ESD reliability concern of independent and mixed designs while analogizing it with QS mitigation. Finally, Section VI concludes this paper.

II. Switching FoM Versus Quasi-Saturation: Design Guidelines

Physics of QS is systematically investigated and unified in the Part I of this paper, while highlighting high field mobility degradation postspace charge modulation and electric field screening [32] to counter mobility degradation as the root cause. Fig. 1 summarizes various LDMOS designs while depicting various design parameters to mitigate QS. Each of these parameters, as presented in Part I, has a potential to mitigate QS independently as well as in combination with each other.

Fig. 2 compares I–V characteristics of LDMOS with QS device with modified designs, which show mitigated QS effect. Among the modified designs, gate overlap (L_{OV}), well doping profile, and insertion of n-type pocket appear to be the key parameters, whereas drain junction depth (X_j) offers a marginal improvement as far as mitigation of QS is concerned. However, it is depicted later that a mixed design with deeper drain junction improves a number of FoM parameters. The design with n-type pocket offers mitigated QS and improved device characteristics without any noticeable change in breakdown voltage; however, it may require an extra mask. It is worth highlighting that individual techniques have their own merits and demerits in terms of meeting device's FoMs for switching/RF performance, ESD reliability, hot carrier degradation, self-heating, and SOA concerns. In a nutshell device's breakdown voltage, parasitic capacitances would get marginally sacrificed for improving performance and reliability characteristics when device design parameters are handled individually. However, given that individual design parameters are now disclosed, an intelligent combination of these parameters can be chosen (mixed designs) to mitigate QS without sacrificing FoM, while keeping physics of QS in mind.

Fig. 3(a)–(d) shows the impact of a few design variables on device's FoM parameters, which in combination with other design variables (as shown in Fig. 1) has been simulated comprehensively to develop mixed designs. Fig. 3(a)–(d) implicates change in FoM, i.e., performance parameters, using a pool of permutations of drift region profile, L_{EXT} and L_{OV}. These projections depict that the effect of L_{OV} over V_{BD}, R_{ON}, and g_m is negligible beyond a point; however, offers a subtle I_{ON} improvement at lower drift region doping, which is attributed to shift in the onset of QS as L_{OV} was increased. On the other hand, increasing L_{OV} potentially adds to parasitic/miller capacitances; therefore, L_{OV} becomes an important parameter causing a tradeoff between circuit performance and QS. However, as the carriers are confined to the surface at higher drift region doping, the trends saturate. Similarly, drift region profile (denotes as peak n-well doping) is a very crucial parameter in overall device design as the space charge modulation largely depends on the background doping.

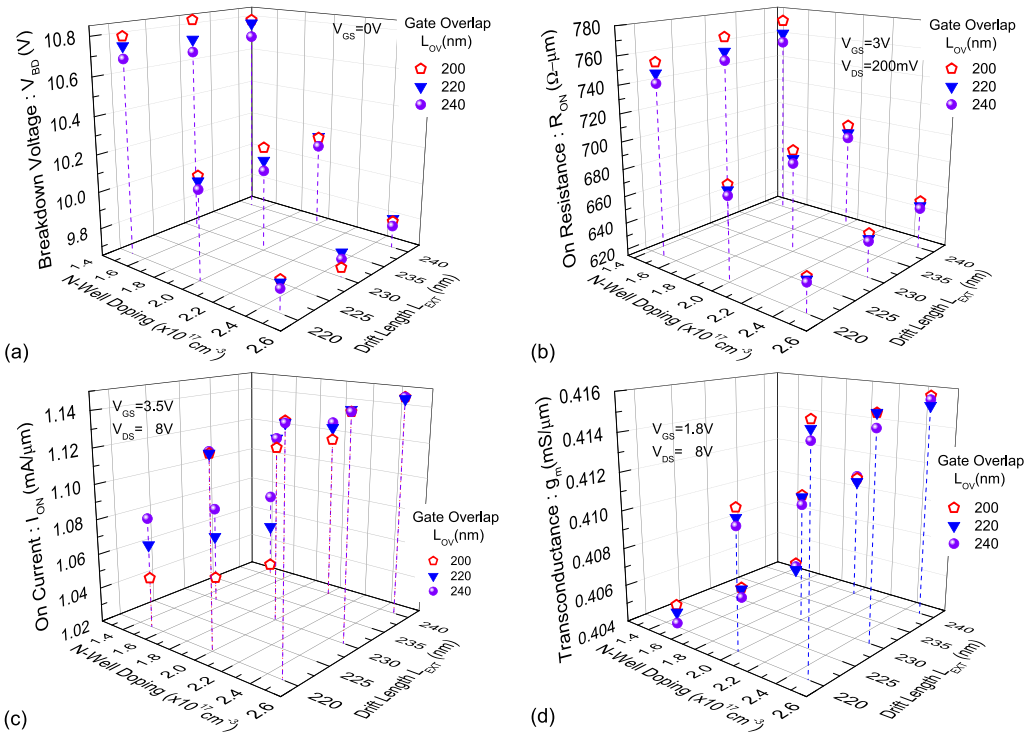

Fig. 3. Device's switching performance parameters of QS mitigated devices as a function of L_{OV}, n-well doping, and L_{EXT}. (a) Breakdown voltage (V_{BD}). (b) ON resistance (R_{ON}). (c) ON current (I_{ON}). (d) Transconductance (g_m).

Drift region profile, in terms of peak n-well doping, shows a clear R_{ON} versus V_{BD} tradeoff in a given range (used in Fig. 3), below which the device's onset of QS falls. It is worth highlighting that the drift region profile along the n-well depth also plays a significant role in QS and in general device design, which was addressed earlier in senior authors works [28], [29]. However, it seriously depends on other design variables, which adds another dimension of complexity. To keep clarity and independence between various design variables, permutations of drift region profile along the n-well depth is not considered in this paper. Finally, Fig. 3(c) shows that L_{OV} mitigates QS and improves R_{ON} for lower background doping. Moreover, L_{EXT} does not show a significant impact on V_{BD} above a point, however, increases R_{ON} linearly; reducing L_{EXT}, however, improves I_{ON} and g_m due to delayed QS and hence shows a tradeoff between QS and breakdown.

As mentioned earlier, the optimum design from Fig. 3 is permuted comprehensively in combination with other design variables (shown in Fig. 1) to develop mixed designs. Fig. 4 shows R_{ON} and V_{BD} tradeoff of design from these new set of experiments and depicts two sets inside the shaded regions: 1) independent designs, i.e., *Set A*, here the chosen parameter of a design is varied by keeping others unaltered, such as for overlap region engineering, the L_{OV} is increased while the other parameters are kept as the same as those in LDMOS with QS and 2) mixed designs, i.e., *Set B*. Detaching from the optimal designs of *Set A*, a set of mixed designs provides lower R_{ON} in addition to an increased V_{BD}. A comparison from Fig. 4 reveals an average breakdown voltage of mixed designs (*Set B*) to be ~13% higher than the average

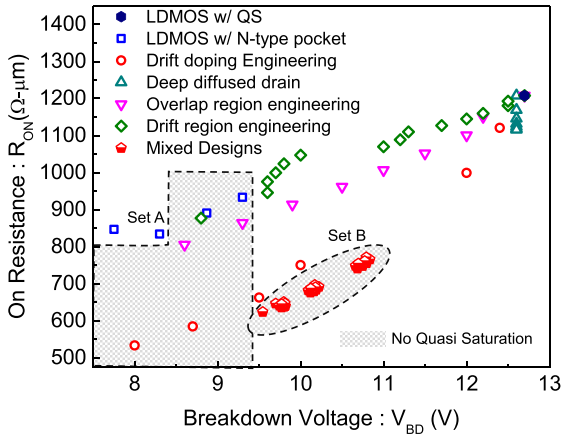

Fig. 4. R_{ON} versus V_{BD} tradeoff of two sets of devices. *SetA* represents independent designs using design parameters shown in Fig. 1 and *SetB* represents mixed designs using combinations of independent design parameters. Shaded region depicts devices without QS. Designs offering no QS with least R_{ON} for a common V_{BD} were selected for rest of the investigations.

V_{BD} of the designs in *Set A*, without a significant change in the R_{ON}. It is worth highlighting that designs outside of the shaded regions (Fig. 4) either guide the device back into QS or lead to an over designing with significant V_{BD} reduction.

III. Quasi-Saturation Versus Analog/RF Performance

Frequency response of LDMOS devices, together with V_{BD} and R_{ON} tradeoff, is a very important FoM parameter.

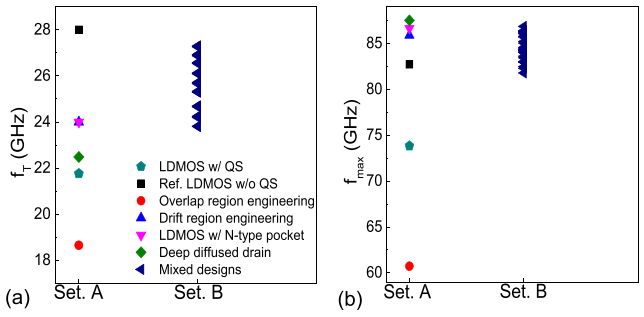

Fig. 5. Frequency performance of devices from *SetA* and *B* compared with LDMOS with QS and reference LDMOS without QS designs. (a) Unity gain frequency (f_T). (b) Maximum oscillation frequency (f_{MAX}).

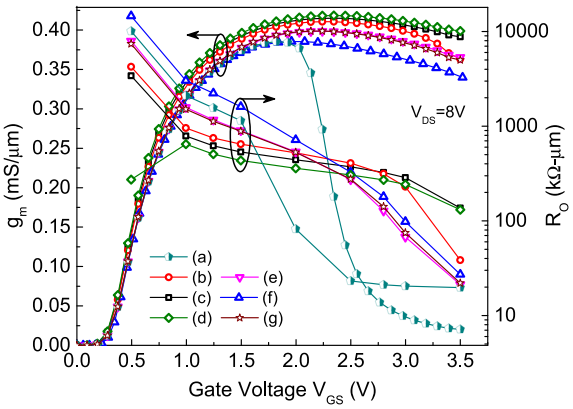

Fig. 6. Transconductance (g_m) and output resistance (R_O) versus gate voltage characteristics of devices from *SetA* and *SetB*. (a) LDMOS with QS. (b) Mixed design (1): $N_{Drift} = 2.5e^{17}$ cm^{-3}, $L_{OV} = 200$ nm, and $L_{EXT} = 220$ nm. (c) Mixed design (2): $N_{Drift} = 2e^{17}$ cm^{-3}, $L_{OV} = 220$ nm, and $L_{EXT} = 230$ nm. (d) Ref. LDMOS without QS. (e) Drift region engineering. (f) Overlap region engineering. (g) LDMOS with n-type pocket.

To find the optimum device among the mixed designs, i.e., *Set B*, cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) were extracted of *Set A* and *Set B* devices, as shown in Fig. 5. Fig. 5 suggests that f_t and f_{MAX} of mixed designs (*Set B*) stand considerably better than individual designs (*Set A*). Moreover, it depicts incorporation of n-type pocket to be a favorable options maximizing frequency response of the device. Moreover, deeper drain junction (X_j) stands favorable for maximizing frequency response. Having considered these benefits of the mixed designs, as shown in Figs. 4 and 5 and discussed above, two designs from *Set B* along with independent designs of *Set A* are considered in further sections for correlating QS with device's analog/RF performance, ESD reliability, hot carrier degradation, self-heating, and SOA concerns.

Fig. 6 compares the transconductance (g_m) and output resistance (R_O) versus gate voltage characteristics of devices from *Set A* and *B* with LDMOS with a QS device. It shows that the presence of QS forces g_m to roll-off and R_O to fall by orders of magnitudes at the higher gate voltages. The extent of g_m roll-off or fall in R_O depends on the strength of QS. For example, LDMOS with QS device has the maximum g_m roll-off and reduction in R_O, whereas the mixed

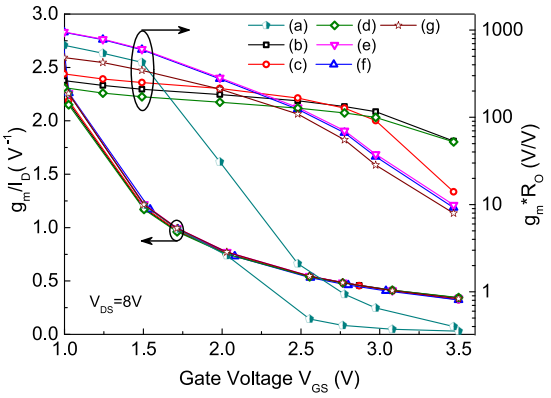

Fig. 7. g_m/I_D and intrinsic transistor gain (g_m*R_o) versus gate voltage characteristics of devices without and with QS. (a) LDMOS with QS. (b) Mixed design (1). (c) Mixed design (2). (d) Ref. LDMOS without QS. (e) Drift region engineering. (f) Overlap region engineering. (g) LDMOS with n-type pocket.

design offers g_m and R_O trends very close to the reference design without QS (device with higher drift region doping). At $V_{GS} = 3$ V, mixed designs offer the orders of magnitude higher g_m and R_O, when compared to LDMOS with the QS device. The other optimum designs fall somewhere between LDMOS with QS and reference design without QS.

Fig. 7 compares analog performance parameters like g_m/I_D and intrinsic transistor gain (g_m*R_o) versus gate voltage characteristics of devices without QS with reference design and device with QS. It shows that the g_m/I_D and intrinsic gain does not differ significantly for different devices at lower gate bias; however, as soon as device enters into QS, it falls depending on the strength of QS. At higher gate voltages, g_m*R_o of mixed designs differs by $\sim$ two orders when compared to LDMOS with QS design and by four times when compared with independent designs without QS. At this stage, it is worth highlighting that the mixed designs offer performance equivalent to reference design with high background doping and breakdown characteristics close to LDMOS with the QS device.

Investigating influence of device design on intrinsic and parasitic capacitances is equally critical, as it directly defines the frequency response of the device (f_t and f_{max}). Hence, device design while mitigating QS should be carried out in a way that parasitic capacitances are reduced to an optimum value. Fig. 8(a) shows C_{DD} with respect to the drain voltage, which affects the switching speed/delay ($\tau = C_{DD}.V_{DS}/I_{DS}$) of the circuit. Fig. 8(a) shows that the drain capacitance of the independent designs without change in drift region doping profile does not differ from LDMOS with QS device; however, the mixed designs, which also account for drift region doping profile, have higher drain capacitance, which may adversely affect the switching performance of the device. Hence, while mitigating QS, drift region engineering must account for potential increase in drain capacitance increase. Fig. 8(b) and (c) shows C_{GD} and C_{GG}, respectively, with respect to the gate voltage, which affects the unity gain frequency ($f_T = (g_m/2\pi(C_{GS} + C_{gd}))$) and maximum oscillation frequency ($f_{MAX} = (1/2)(f_T/(2\pi.f_T.C_{gd}.R_g + (R_g/r_o))^{1/2})$)

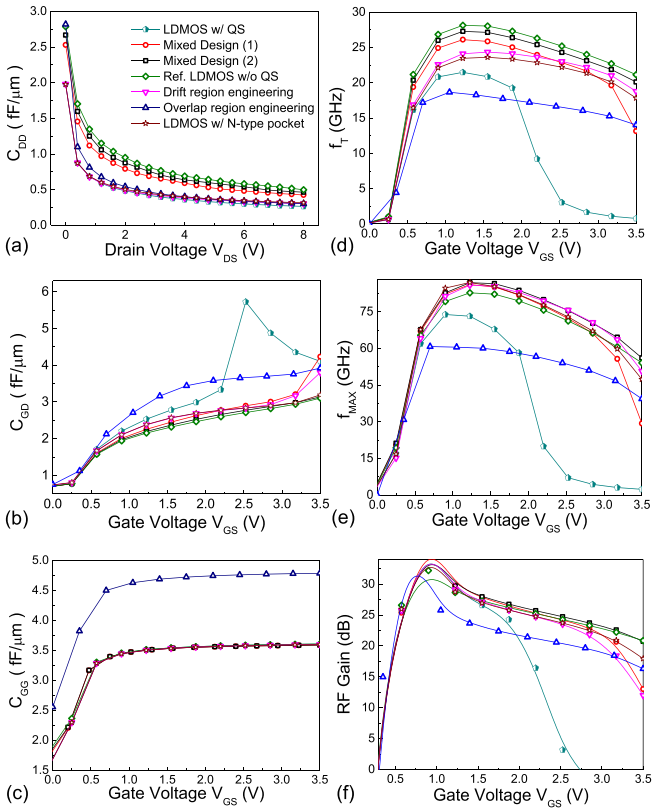

Fig. 8. Comparison of frequency and capacitance parameters of different optimized devices with Std.LDMOS. (a) Parasitic drain capacitance C_{DD} versus V_{DS}. (b) Miller capacitance C_{GD} versus V_{DS}. (c) Gate capacitance C_{GG} versus V_{GS}. (d) f_T versus V_{GS}. (e) f_{MAX} versus V_{GS}. (f) Power gain (MUG) versus V_{GS}.

of the device. Fig. 8(b) shows the nonlinear nature of miller capacitance in the quasi-saturated (convention) LDMOS device. In general, the figure depicts the presence of nonlinearity as soon as QS is triggered. This attributes to the absence of nonlinearity in mixed designs. Fig. 8(c) shows no change in the gate capacitance among all designs, except the design with higher gate-to-drift region overlap length. Therefore, the attempt while mitigating QS should be to minimize L_{OV}.

Fig. 8(d)–(f) shows frequency and RF gain versus gate voltage characteristics, which clearly shows the influence of QS or design variables. Fig. 8(d) shows a clear shift in unity gain frequency as the strength of QS increases. For example, mixed designs offer f_T close to reference design for all range of gate voltages, whereas the independent designs offer lower f_T and rolls-off at higher gate voltages. The LDMOS with QS, which suffers seriously with QS, shows lower f_T, which rolls-off at much lower gate voltages. The influence of L_{OV} on frequency response is also clearly evident from the figure. Fig. 8(e) and (f) shows that the f_{MAX} and RF gain, respectively, do not depend on the extent of QS directly; however, depend on f_T, parasitic capacitances and g_m roll-off. Clearly, the well-designed devices (mixed designs) without QS show significantly better frequency and gain performance, when compared to LDMOS with QS device, which suffers from QS.

IV. Quasi-Saturation Versus Hot Carrier Degradation

In the earlier Sections II and III, various key design parameters for mitigating QS are explored. It comes out that, engaging multiple dimensional design variables gives an optimized device (Mixed B1/Mixed B2), which qualifies for QS mitigation. In this section, HCI degradation/reliability aspects are augmented to various key design parameters, including mixed designs discussed so far. HCI degradation mechanism for DeNMOS has been investigated earlier by Varghese *et al.* [14]. In this paper, for the first time, HCI reliability for both ON and OFF states is studied for DeMOS devices using spherical harmonic expansion (SHE) of Boltzmann transport equation [33]. This has helped in HCI aware device design keeping QS issues in mind.

Hot carrier density at the gate-to-drain edge and HCI degradation in ON state is often maximum at $V_{GS} \sim V_{DS}/2$. This proportion was earlier experimentally and theoretically validated by various groups [11], [15], [34], which was then considered to be started practice for symmetric planar MOSFETs. However, in the case of LDMOS device, as V_{DS} is significantly higher than V_{GS} and because of extended/asymmetric drain, the same proportion is not valid. For this reason, while investigating ON-state HCI degradation behavior, V_{GS} for different designs was chosen as such that it gives rise to maximum substrate current and V_{DS} was kept close to the breakdown voltage to accelerate hot carrier generation. Fig. 9 shows the electron and hole energies in the channel and interface trap generation at the Si–SiO_2 interface, extracted for various designs, under ON and OFF states. Fig. 9(d)–(f) shows that, except devices with n-type pocket and drift region engineering, other designs have similar or better hot electron energy when compared to conventional and other QS mitigated designs. Moreover, no major change in hot hole energy profile was noticed. As a result except device with overlap engineering, other designs, including mixed designs, show similar or higher degradation under OFF state. As the devices were mostly engineered for ON state (QS) operation, the HCI degradation dynamics is completely different. Fig. 9(a)–(c) shows that mixed design 2 and device with overlap engineering offers lower electron and hole energies when compared to conventional design and other QS mitigated designs. As a result, in ON state, devices with mixed design lead to lower interface trap generation when compared to overlap engineering and n-type pocket designs.

V. Self Heating, Safe Operating Area, and ESD Concerns

Other than RF, switching and mixed signal performance, and HCI reliability issues, self-heating, SOA, and ESD are other bigger concerns for LDMOS device design. This section for the first time investigates the impact of various key design parameters on thermal, SOA, and ESD ruggedness of LDMOS devices while correlating it with QS.

A. Self-Heating

Lattice heating is attributed to electron–phonon interaction and energy exchange from hot electrons to the crystal lattice

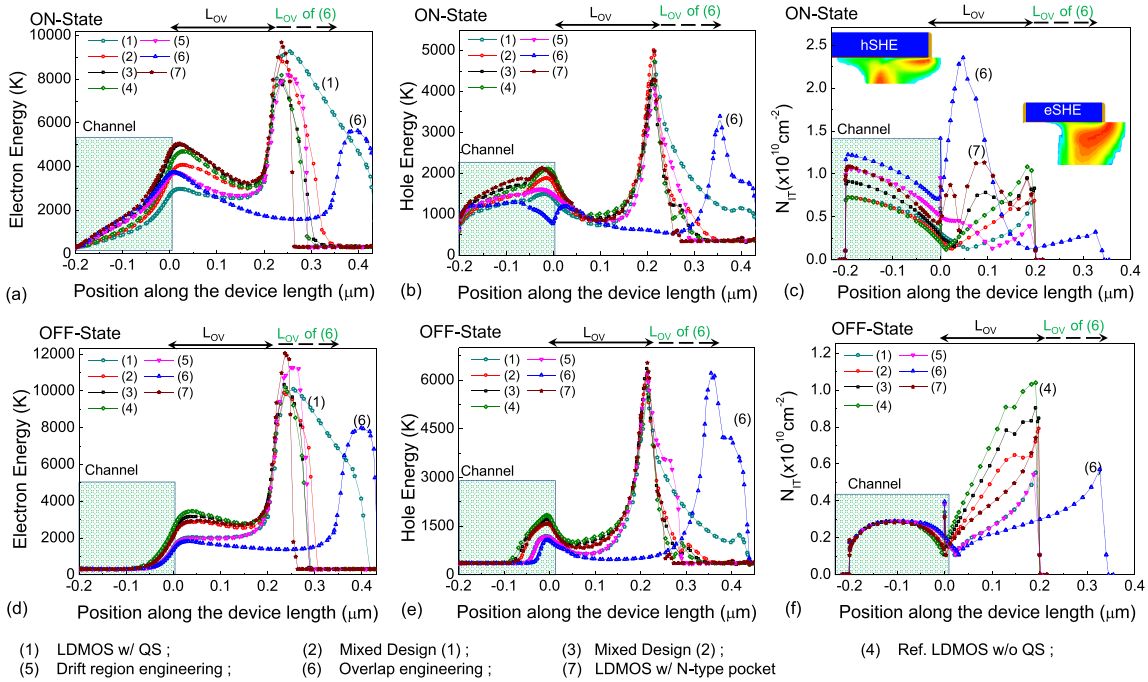

Fig. 9. (a) and (d) Hot electron energy. (b) and (e) Hot hole energy. (c) and (f) Generated interface trap density extracted using SHE of Boltzmann transport equation [33] under (a)–(c) ON and (d)–(f) OFF states. Hot electron and hole energy were extracted along the channel and 1 nm below the Si–SiO_2 interface. Interface trap density was extracted at the Si–SiO_2 interface. Devices were stressed for a duration of 10^5 s, at a gate bias which gives peak substrate current in ON state and $V_{GS} = 0$ V in OFF state. In both the condition, drain terminal was stressed close to drain-to-substrate junction breakdown voltage. Note that the gate edge for device with overlap engineering is larger than the other designs, and its corresponding scale is marked over the figure.

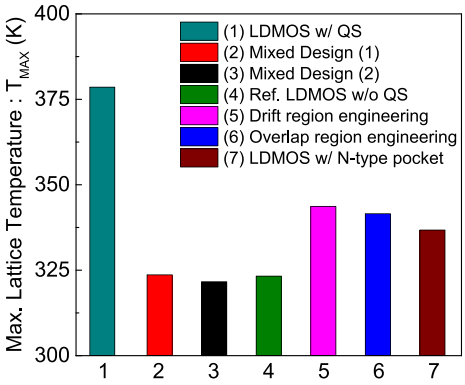

Fig. 10. Comparison of maximum lattice temperature across various devices engineered using individual and mixed design parameters. 100-ns pulse I–V electrothermal simulations were performed to capture lattice heating. Lattice temperature was extracted for a fixed drain voltage while keeping appropriate gate voltage to fix drain current.

in form of phonons. In semiclassical terms, lattice heating is directly related to electric field (E), current density within the peak E-field region, and thermal boundary conditions. If thermal boundary conditions remain the same, then device must be engineered to minimize electric field peaking and current crowding. Having explored the physics of QS and various key design parameters to mitigate QS and improve performance and reliability, it is worth investigating the self-heating behavior of LDMOS devices in terms of these design parameters while correlating it with QS. Besides thermal management, self-heating is critical from HCI reliability point of view as well. Fig. 10 compares lattice temperature across LDMOS devices engineered using various independent and mixed design parameters extracted using 100-ns pulse simulations for a fixed drain voltage and drain current. The devices without QS (mixed designs and reference LDMOS without QS) show the least self-heating when compared to device with marginal QS (drift region engineering, overlap region engineering, and LDMOS with n-type pocket) or quasi-saturated devices (conventional LDMOS). This is attributed to the absence of or lower: 1) electric field next to N^+ drain and 2) current crowing close to the surface when compared to conventional/quasi-saturated device. Based on these observations, it would not be an exaggeration to conclude that mitigating QS also helps in lowering self-heating across the device, which is attributed to absence or electric field peaking at higher currents and well distributed current flow in the drift region.

B. Safe Operating Area and ESD Reliability

Electrical, thermal, or electrothermal instability along the width plane of a device leads to voltage snapback (NDR region) and catastrophic failure of the device. The instability can be triggered due to regenerative n-p-n action and nonuniform bipolar turn-ON, thermal run-away, high-field mobility degradation, or a combination of all these [20], [23]. This leads to the formation of current filament and failure when device is stressed under high voltage or high current condition [24], [35]. A combination of both high voltage and high current stress is even critical. Such a stress during normal circuit operation is very usual, which in case of

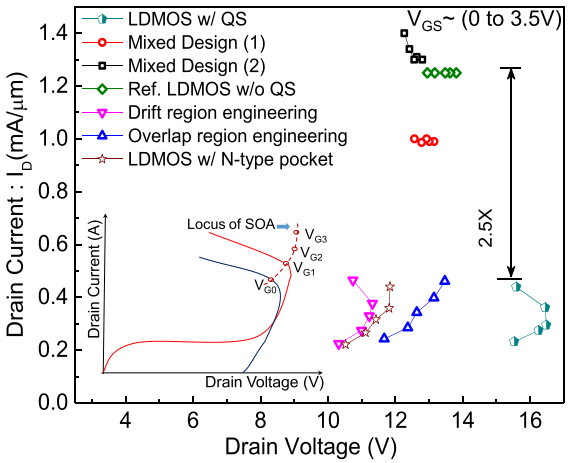

Fig. 11. Allowed SOA for various engineered LDMOS devices to mitigate QS using independent and mixed design parameters. QS-mitigated devices increase the current SOA boundary by two times while keeping voltage SOA intact. Inset: method used to extract SOA boundary. SOA boundary was extracted using 3-D electrothermal pulse (100 ns) *I–V* simulations.

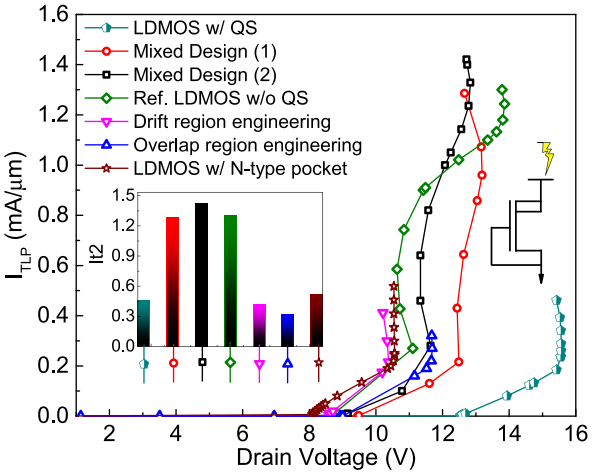

Fig. 12. Comparison of simulated TLP *I–V* characteristics of LDMOS device with QS and other QS mitigated independent and mixed designs. Inset: ESD failure current (It2) of various designs.

switching applications is generated from an inductive load and is attributed to impedance mismatch in case of RF power amplifiers. Therefore, the current or voltage, which initiates the voltage snapback or NDR, is the maximum permissible current allowed through the device for a given voltage. Beyond this current range, device is prone to fail due to electrothermal instabilities, hence the term SOA and SOA boundary. Devices can experience similar stress due to the transfer of static charge during manufacturing, packaging, and handling, which is commonly known as ESD. ESD reliability is a critical concern for LDMOS devices [20]. At this stage, it is worth investigating SOA boundary and ESD reliability of various LDMOS devices engineered using independent or mixed design parameters to mitigate QS.

Fig. 11 shows the SOA boundary of various LDMOS devices engineered to mitigate QS extracted using 3-D electrothermal pulse (100 ns) *I–V* simulations. Given that both QS and electrothermal instability causing SOA concerns are triggered by the onset of space charge modulation and mobility

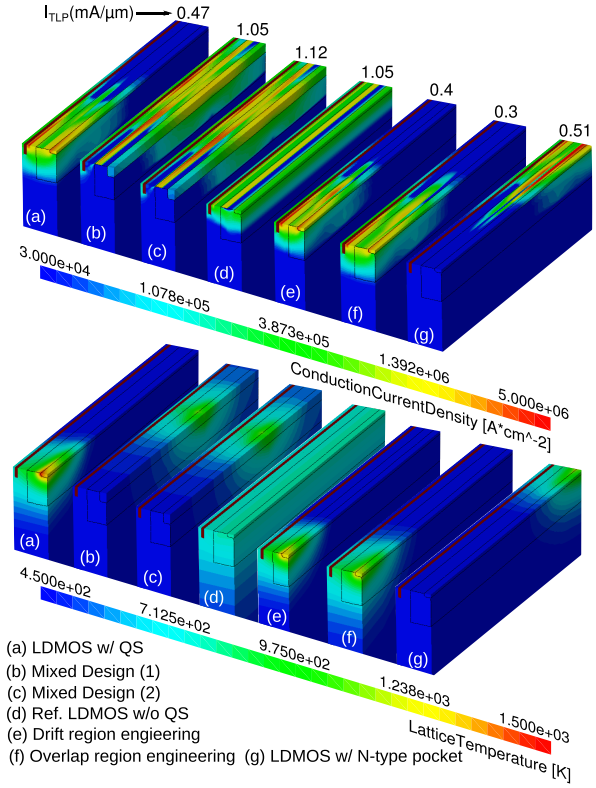

Fig. 13. (a) Conduction current density (A/cm^2) and (b) lattice temperature (K) contour extracted at failure current for various QS mitigated independent and mixed designs. Mixed and reference LDMOS designs without QS have uniform current conduction even under very high injection currents unlike the device with QS.

degradation [20], [21] and QS mitigated mixed designs, and reference LDMOS device without QS shows improved SOA boundary when compared with conventional LDMOS device. It is attributed to the fact that QS mitigated designs shift the onset of space charge modulation to higher currents, which in-turn improves the failure current.

Similarly, Fig. 12 shows that TLP *I–V* characteristics of grounded gate LDMOS device with QS compare it with other QS mitigated independent and mixed designs. It is evident that except the mixed and reference designs, all other devices fail at very low currents, right at the onset of space charge modulation. Whereas, the mixed design and reference design show a steep bipolar branch, which signifies uniform current conduction and the absence of space charge modulation. This is verified in Fig. 13, which depicts uniform current conduction through mixed and reference designs even under high current injection conditions, which leads to significantly relaxed lattice heating compared with independent designs. It further shows the presence of strong filament formation at very low currents in the independent design and device with QS. Hence, it can be concluded that avoiding QS is a key to improve SOA boundaries and ESD reliability.

VI. Conclusion

It was found that switching/analog/RF performance of LDMOS devices is directly related to onset and extent of QS. Attributed to the finding that QS leads to high field and current

crowding across the device, a strong correlation between QS and HCI degradation, self-heating, SOA concerns as well as ESD behavior of LDMOS devices was found. Drift region engineering using various mixed design parameters was found to be the key to mitigate QS in LDMOS devices. It can be concluded that serious concerns like HCI, thermal management, SOA, and ESD can be delayed, while maximizing the performance, if QS is avoided.

REFERENCES

[1] B. S. Kumar and M. Shrivastava, "Part I: On the unification of physics of quasi-saturation in LDMOS devices," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 191–198, Jan. 2018.

[2] M. N. Darwish, "Study of the quasi-saturation effect in VDMOS transistors," *IEEE Trans. Electron Devices*, vol. ED-33, no. 11, pp. 1710–1716, Nov. 1986.

[3] C. H. Kreuzer, N. Krischke, and P. Nance, "Physically based description of quasi-saturation region of vertical DMOS power transistors," in *IEDM Tech. Dig.*, Dec. 1996, pp. 489–492.

[4] J. Evans and G. Amaratunga, "The behavior of very high current density power MOSFETs," *IEEE Trans. Electron Devices*, vol. 44, no. 7, pp. 1148–1153, Jul. 1997.

[5] M. Knaipp, G. Rohrer, R. Minixhofer, and E. Seebacher, "Investigations on the high current behavior of lateral diffused high-voltage transistors," *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1711–1720, Oct. 2004.

[6] L. Wang *et al.*, "Physical description of quasi-saturation and impact-ionization effects in high-voltage drain-extended MOSFETs," *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 492–498, Mar. 2009.

[7] K. H. Lou, C. M. Liu, and J. B. Kuo, "Analysis of the quasi-saturation behavior considering the drain-to-source voltage and cell-spacing effects for a vertical DMOS power transistor," *Solid-State Electron.*, vol. 36, no. 1, pp. 85–91, 1993.

[8] C.-M. Liu and J. B. Kuo, "Quasi-saturation capacitance behavior of a DMOS device," *IEEE Trans. Electron Devices*, vol. 44, no. 7, pp. 1117–1123, Jul. 1997.

[9] D. Müller, A. Giry, D. Pache, J. Mourier, B. Szelag, and A. Monroy, "Architecture optimization of an N-channel LDMOS device dedicated to RF-power application," in *Proc. 17th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2005, pp. 159–162.

[10] C.-C. Cheng, J. F. Lin, and T. Wang, "Impact of self-heating effect on hot carrier degradation in high-voltage LDMOS," in *IEDM Tech. Dig.*, Dec. 2007, pp. 881–884.

[11] C. Hu, "Hot-electron effects in MOSFETs," in *IEDM Tech. Dig.*, vol. 29. Dec. 1983, pp. 176–181.

[12] S. Poli *et al.*, "Hot-carrier stress induced degradation in multi-STI-finger LDMOS: An experimental and numerical insight," *Solid-State Electron.*, volS. 65–666, pp. 57–63, Nov./Dec. 2011.

[13] C. Schlünder *et al.*, "Hot-carrier induced dielectric breakdown (HCIDB) challenges of a new high performance LDMOS generation," in *Proc. IEEE Int. Rel. Phys. Symp.*, Jun. 2012, pp. XT.15.1–XT.15.5.

[14] D. Varghese *et al.*, "OFF-state degradation in drain-extended NMOS transistors: Interface damage and correlation to dielectric breakdown," *IEEE Trans. Electron Devices*, vol. 54, no. 10, pp. 2669–2678, Oct. 2007.

[15] K. Mistry and B. Doyle, "How do hot carriers degrade n-channel MOSFETs?" *IEEE Circuits Devices Mag.*, vol. 11, no. 1, pp. 28–33, Jan. 1995.

[16] M. Shrivastava, M. S. Baghini, H. Gossner, and V. R. Rao, "Part II: A novel scheme to optimize the mixed-signal performance and hot-carrier reliability of drain-extended MOS devices," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 458–465, Feb. 2010.

[17] D. Brisbin, A. Strachan, and P. Chaparala, "Design optimization of N-LDMOS transistor arrays for hot carrier lifetime enhancement," in *Proc. 41st Annu. IEEE Int. Rel. Phys. Symp.*, Mar./Apr. 2003, pp. 608–609.

[18] A. Strachan and D. Brisbin, "Optimization of LDMOS array design for SOA and hot carrier lifetime," in *Proc. IEEE 15th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, Apr. 2003, pp. 84–87.

[19] M. Shrivastava, R. Jain, M. S. Baghini, H. Gossner, and V. R. Rao, "A solution toward the OFF-state degradation in drain-extended MOS device," *IEEE Trans. Electron Devices*, vol. 57, no. 12, pp. 3536–3539, Dec. 2010.

[20] M. Shrivastava and H. Gossner, "A review on the ESD robustness of drain-extended MOS devices," *IEEE Trans. Electron Devices*, vol. 12, no. 4, pp. 615–625, Dec. 2012.

[21] M. Shrivastava, H. Gossner, M. S. Baghini, and V. R. Rao, "Part I: On the behavior of STI-type DeNMOS device under ESD conditions," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2235–2242, Sep. 2010.

[22] M. Shrivastava, H. Gossner, M. S. Baghini, and V. R. Rao, "Part II: On the three-dimensional filamentation and failure modeling of STI type DeNMOS device under various ESD conditions," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2243–2250, Sep. 2010.

[23] P. L. Hower, "Safe operating area—A new frontier in LDMOS design," in *Proc. Int. Symp. Power Semiconductor Devices ICS*, Jun. 2002, pp. 1–8.

[24] A. Podgaynaya, D. Pogany, E. Gornik, and M. Stecher, "Improvement of the electrical safe operating area of a DMOS transistor during ESD events," in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2009, pp. 437–442.

[25] P. S. Swain, M. Shrivastava, M. S. Baghini, H. Gossner, and V. R. Rao, "On the geometrically dependent quasi-saturation and g_m reduction in advanced DeMOS transistors," *IEEE Trans. Electron Devices*, vol. 63, no. 4, pp. 1621–1629, Apr. 2016.

[26] P. S. Swain, M. Shrivastava, H. Gossner, and M. S. Baghini, "Device–circuit co-design for beyond 1 GHz 5 V level shifter using DeMOS transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3827–3834, Nov. 2013.

[27] M. Shrivastava, M. S. Baghini, H. Gossner, and V. R. Rao, "Part I: Mixed-signal performance of various high-voltage drain-extended MOS devices," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 448–457, Feb. 2010.

[28] A. Gupta *et al.*, "Drain extended MOS device design for integrated RF PA in 28 nm CMOS with optimized FoM and ESD robustness," in *IEDM Tech. Dig.*, Dec. 2014, pp. 3–5.

[29] A. Gupta, M. Shrivastava, M. S. Baghini, D. K. Sharma, H. Gossner, and V. R. Rao, "Part I: High-voltage MOS device design for improved static and RF performance," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3168–3175, Oct. 2015.

[30] A. Gupta, M. Shrivastava, M. S. Baghini, A. N. Chandorkar, H. Gossner, and V. R. Rao, "Part II: A fully integrated RF PA in 28-nm CMOS with device design for optimized performance and ESD robustness," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3176–3183, Oct. 2015.

[31] *TCAD Sentaurus: Sentaurus Device User Guide Release H-2013.03*, Synopsys, Mountain View, CA, USA, 2013.

[32] E. J. Yoffa, "Screening of hot-carrier relaxation in highly photoexcited semiconductors," *Phys. Rev. B, Condens. Matter*, vol. 23, no. 4, p. 1909, 1981.

[33] A. Gnudi, D. Ventura, G. Baccarani, and F. Odeh, "Two-dimensional MOSFET simulation by means of multidimensional spherical harmonics expansion of the Boltzmann transport equation," *Microelectron. Eng.*, vol. 19, pp. 917–924, Sep. 1992.

[34] N. Koike and K. Tatsuuma, "A drain avalanche hot carrier lifetime model for n- and p-channel MOSFETs," in *Proc. 40th Annu. Rel. Phys. Symp.*, Apr. 2002, pp. 86–92.

[35] P. L. Hower, J. Lin, and S. Merchant, "Snapback and safe operating area of LDMOS transistors," in *IEDM Tech. Dig.*, Dec. 1999, pp. 193–196.

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