Part I: Physical Insights Into the Two-Stage Breakdown Characteristics of STI-Type Drain-Extended pMOS Device

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***Abstract*— In this paper, we study breakdown characteristics in shallow-trench isolation (STI)-type drain-extended MOSFETs (DeMOS) fabricated using a low-power 65-nm triple-well CMOS process with a thin gate oxide. Experimental data of p-type STI-DeMOS device showed distinct two-stage behavior in breakdown characteristics in both OFF- and ON-states, unlike the n-type device, causing a reduction in the breakdown voltage and safe operating area. The first-stage breakdown occurs due to punchthrough in the vertical structure formed by p-well, deep n-well, and p-substrate, whereas the second-stage breakdown occurs due to avalanche breakdown of lateral n-well/p-well junction. The breakdown characteristics are also compared with the STI-DeNMOS device structure. Using the experimental results and advanced TCAD simulations, a complete understanding of breakdown mechanisms is provided in this paper for STI-DeMOS devices in advanced CMOS processes.**

***Index Terms*— Avalanche breakdown, drain-extended MOSFET (DeMOS), input–output (I/O), Kirk effect, parasitic bipolar triggering, safe operating area (SOA), shallow-trench isolation (STI), two-stage breakdown.**

I. Introduction

AVALANCHE breakdown phenomenon is an important physical limitation of all MOSFET devices. It determines maximum power supply voltage for device operation [1]. For standard bulk MOSFETs, OFF-state device breakdown can occur due to: 1) gate-controlled avalanche multiplication in reverse-biased drain-substrate junction at high drain voltages; 2) drain-to-source punchthrough or bulk drain-induced barrier lowering; 3) gate-induced drain leakage current due to band-to-band tunneling of carriers, limiting the drain breakdown voltage to lower than the junction avalanche breakdown voltage values, particularly for highly scaled devices with heavily doped drain-substrate junction [2]; and 4) gate oxide breakdown for thin gate oxide devices, or due to a combination of above factors. Snapback can occur in output characteristics after turn-ON of intrinsic parasitic bipolar transistor due to base–emitter voltage-drop caused by substrate current generated from avalanching junction. Devices operating in snapback mode are used as on-chip electrostatic discharge protection devices [3]. An understanding of drain breakdown mechanisms helps in optimizing devices to improve their breakdown voltage and device reliability margins in scaled technologies.

For high-voltage applications, such as automotive circuits, power management and RF circuits, lateral double-diffused MOSFETs (LDMOS), and drain-extended MOSFETs (DeMOS), that can be integrated in standard CMOS process are used to support high power supply voltages. Drain breakdown in these device structures has been linked to breakdown of p-n junction between the MOS body and the drift region [3]. For high-voltage devices, tradeoffs between OFF-state breakdown voltage, ON-state resistance, and safe operating area (SOA) need to be optimized [4]. Detailed analysis of avalanche behavior in output characteristics is useful in characterizing and enhancing the SOA and robustness of power devices. In [5], a study was carried out on quasi-saturation effect and impact ionization (II) occurring in the channel, drift, and drain junction regions that affect the output characteristics in LDMOS devices. The nonlinear dependence of carrier velocity saturation on electric field and Kirk effect (base-push effect) in the drift region play a dominant role in the output characteristics. In [6], an unusual drain current enhancement at high drain and gate voltages in shallow-trench isolation (STI)-LDMOS has been found to be due to II in drift region.

For advanced system-on-chip (SoC) applications requiring high-speed input–output (I/O) interfaces operating at 1.8–5 V, DeMOS devices that are fully compatible with standard CMOS process technology have been found useful [7]. Circuit applications of DeMOS devices include I/O interface circuits in SoCs, power amplifiers, line drivers, voltage level shifters, power-conditioning units, and CMOS-microelectromechanical

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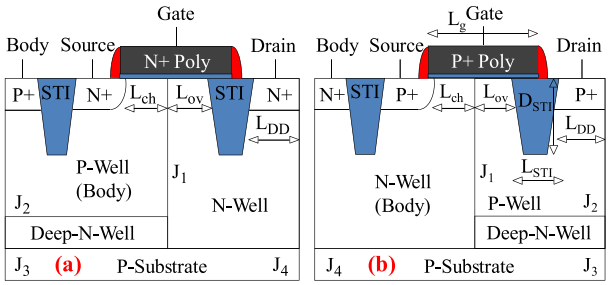

Fig. 1. Schematics of device structures under study. (a) STI-DeNMOS and (b) STI-DePMOS devices. Device geometric parameters are defined in Table I. Role of junctions J_1–J_4 in breakdown is described in Section III.

TABLE I
GEOMETRIC PARAMETERS

Parameter (μm)	STI-DeNMOS	STI-DePMOS
L_g	0.93	0.625
L_{ch}	0.45	0.1
L_{ov}	0.28	0.35
L_{DD}	0.15	0.4
L_{STI}	0.35	0.35
D_{STI}	0.35	0.35

L_g = poly-gate length, L_{ch} = channel length, L_{ov} = gate-to-drain overlap length, L_{DD} = drain diffusion length, L_{STI} and D_{STI} = length and depth of STI under gate-to-drain overlap, respectively.

systems interface circuits. In this section, we study a distinct breakdown behavior observed in dc output characteristics of p-type STI-type DeMOS (STI-DePMOS), which has not been reported before. Physical origin of both OFF-state and ON-state breakdown behavior in STI-DePMOS is studied in depth. In Part II, we design the well doping profiles to avoid such breakdown [8]. The organization of this paper is as follows. Section II describes the device structures under study and their output characteristics. Section III describes in detail the physics of two-stage breakdown in OFF-state and ON-state in STI-DePMOS as analyzed using TCAD simulations. In addition, the breakdown characteristics in STI-DePMOS are compared with those of STI-DeNMOS. Finally, the conclusion is drawn in Section IV.

II. Device Structures and Output Characteristics

A. STI-DeMOS Device Structures Under Study

The DeMOS device structures used in this paper are shown in Fig. 1. The STI-type device structures in Fig. 1(a) and (b) are fabricated using a standard low-power 65-nm triple-well SoC CMOS process technology. The process flow for DeMOS devices uses the same process flow for standard devices and requires no additional process steps. Both devices have STI structure under the gate-to-drain overlap edge. The devices use a thin gate oxide of thickness of ∼2 nm. p-well (n-well) and n-well (p-well) are used as a channel and drift region of the STI-DeNMOS (STI-DePMOS) device. The devices also have a deep-n-type layer (n-buried layer) below p-well that is used for isolation of analog and digital circuits in mixed-signal SoCs. Geometric parameters of the investigated devices are given in Table I.

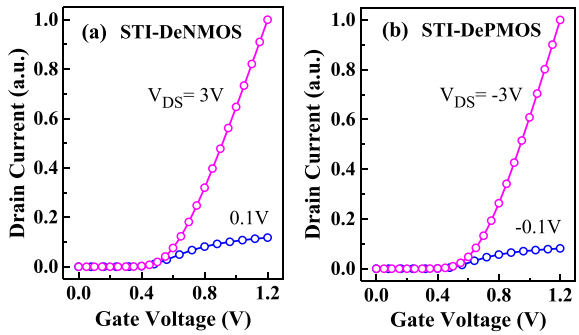

Fig. 2. Measured I_D–V_G characteristics in linear and saturation regions of (a) STI-DeNMOS and (b) STI-DePMOS devices.

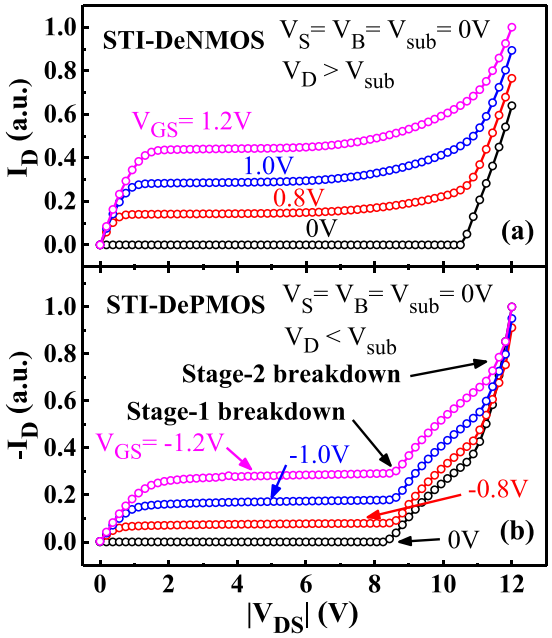

Fig. 3. Measured output I_D–V_D characteristics of (a) STI-DeNMOS and (b) STI-DePMOS devices. Two-stage drain breakdown occurs in p-type device, unlike in n-type device.

B. Experimental I–V Characteristics

The measured drain current versus gate voltage I_D–V_G characteristics in linear (at $|V_{DS}|$ = 0.1 V) and saturation (at $|V_{DS}|$ = 3 V) regions are shown in Fig. 2(a) and (b) for STI-DeNMOS and STI-DePMOS devices. Constant current threshold voltage (at 0.1 μA/μm of drain current) in a linear region is 0.39 V for STI-DeNMOS device and 0.42 V for STI-DePMOS device.

Experimental output characteristics of STI-DeNMOS and STI-DePMOS devices shown in Fig. 3(a) and (b) are extracted from dc voltage sweep measurements at $|V_{GS}|$ = 0, 0.8, 1, and 1.2 V. The output characteristics of STI-DeNMOS [Fig. 3(a)] exhibit the conventional n-well/p-well junction breakdown, parasitic bipolar triggering, and snapback in high current regime [3]. Due to STI architecture, a high OFF-state breakdown voltage of 10.5 V is observed in the experimental characteristics. For STI-DePMOS device [Fig. 3(b)], a distinct two-stage drain breakdown behavior is observed at high drain voltages in both OFF- and ON-states. The first-stage

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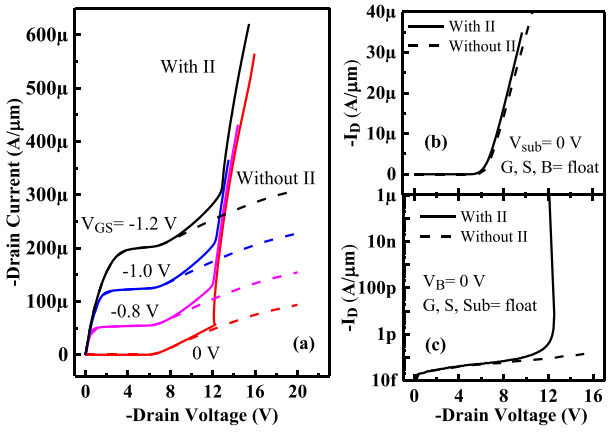

Fig. 4. (a) Simulated output I_D–V_D characteristics of STI-DePMOS device with and without II model. The qualitative two-stage breakdown behavior is observed with II model turned ON. The II of electrons and holes dominates the second stage of breakdown. Simulated two-terminal (b) drain-to-substrate and (c) drain-to-body I–V characteristics with and without II model.

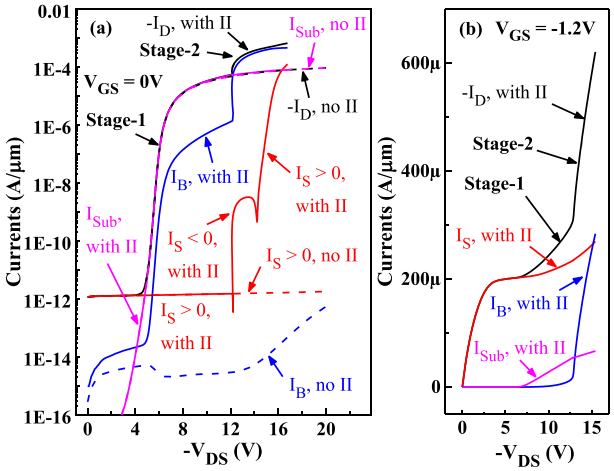

Fig. 5. Simulated terminal currents versus drain voltage V_{DS} at (a) $V_{GS} = 0$ V and (b) $V_{GS} = -1.2$ V ($V_S = V_B = V_{Sub} = 0$ V) of STI-DePMOS device. In (a), the terminal currents are shown both with (solid lines) and without (dashed lines) II model. Substrate current (I_{Sub}) dominates the first-stage breakdown and body current (I_B) dominates the second-stage breakdown. In (a), the absolute value of source current ($|I_S|$) is plotted with II to indicate I_S reversals at $V_{DS} = -12.1$ and -14 V.

drain breakdown occurs at $V_{DS} = -8.3$ V and the second-stage drain breakdown at $V_{DS} = -11$ V. Slope of I_D–V_D characteristics is higher in the second-stage breakdown as compared with the first-stage breakdown. These I_D–V_D characteristics [Fig. 3(b)] are not seen in n-type devices. It must be noted that even when the output characteristics are measured with p^+-source and n^+-body held at high voltage of 12 V ($V_S = V_B = 12$ V) and sweeping the drain voltage positive with respect to p-substrate (ground) ($V_D > V_{sub} = 0$ V, $V_{DS} < 0$V) at different gate-to-source voltages ($V_{GS} = 0$ to -1.2 V), the same two-stage drain breakdown behavior is observed. Hence, it can be concluded that the two-stage drain breakdown characteristics are the characteristics of p^+-drain-to-n^+-body structure. Details of the breakdown mechanisms are described in Section III.

III. Physics of Two-Stage Breakdown in STI-DePMOS

The STI-DeMOS devices are realized using a standard 65-nm CMOS process deck [9] while using Monte Carlo implants. For electrical simulations, hydrodynamic carrier transport model is used. Electron and hole impact ionization (II) are modeled using van Overstraeten-de Man model. Shockley–Read–Hall and Auger recombination models are included to account for carrier generation–recombination. In addition, the bandgap narrowing model for silicon, doping-dependent Masetti mobility model, Lombardi surface mobility degradation model at silicon–oxide interfaces, and high-field mobility saturation models are switched ON. Since the goal is to simulate the breakdown characteristics qualitatively, these models are used with their default parameters [10].

Fig. 4(a) shows the simulated I_D–V_D characteristics of STI-DePMOS both with and without II model. With II model turned ON, the qualitative two-stage drain breakdown behavior is observed. When the output characteristics are simulated without II model switched ON, a distinct increase in the drain current (I_D) is seen at all the values of V_{GS} [Fig. 4(a)]. In this case, the second stage of breakdown is removed, but the first stage of breakdown is still triggered and can be due to merging of depletion regions of two nearby p-n junctions. It is worth investigating the two-terminal reverse-biased I–V characteristics between drain and body and also between drain and substrate with and without II model (keeping other terminals floating). An additional (fifth) contact is added at p-substrate bottom in device simulation. The drain-to-substrate structure (formed by p-well, deep n-well, and p-substrate) shows lower breakdown voltage of $V_{BD} \sim -5$ V and is independent of II of carriers [Fig. 4(b)]. However, the drain-to-body structure shows higher breakdown voltage of $V_{BD} \sim -12$ V and is due to II of carriers [Fig. 4(c)]. The slightly negative differential resistance in Fig. 4(c) is due to carrier energy relaxation effects captured in avalanche generation in the hydrodynamic transport model [11]. The hydrodynamic model has been used, since it captures the device breakdown characteristics more accurately compared with the drift diffusion model. Hence, the drain-to-substrate structure is responsible for the first-stage breakdown, whereas the breakdown in the drain-to-body structure causes the second-stage breakdown.

Fig. 5 shows the simulated terminal currents in OFF- ($V_{GS} = 0$ V) and ON-states ($V_{GS} = -1.2$ V) breakdown. In OFF-state, as (magnitude of) drain voltage (V_{DS}) is increased, the substrate current (I_{Sub}) dominates the first stage of drain breakdown current. As drain voltage is further increased, body current (I_B) dominates over substrate current in the second stage of breakdown [Fig. 5(a)]. Body current (I_B) (at n^+ body diffusion) is negligible, when II model is OFF. However, when II model is ON, I_B rises steeply at the onset of stage-1 breakdown and rises more steeply at the onset of stage-2 breakdown. In addition, the source current (I_S) is negligible, until the onset of stage-2 breakdown at $V_{DS} = -12.1$ V. The I_S reverses to negative at $V_{DS} = -12.1$ V, and then again reverses to positive

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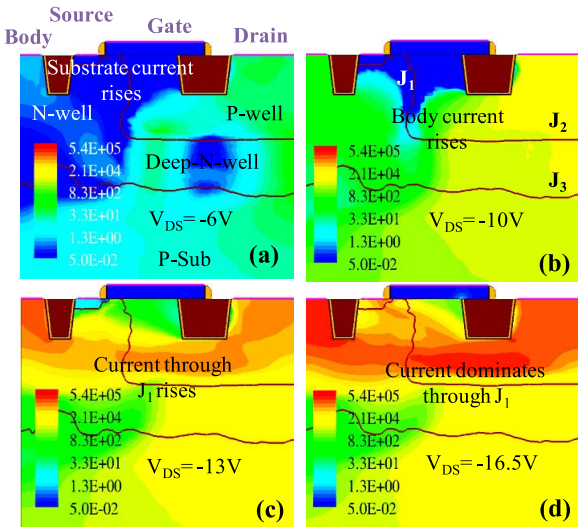

Fig. 6. Conduction current density (A/cm^2) contour in STI-DePMOS device at $V_{GS} = 0$ V and (a) $V_{DS} = -6$ V ($I_D = -120$ nA/μm), (b) $V_{DS} = -10$ V ($I_D = -33$ μA/μm), (c) $V_{DS} = -13$ V ($I_D = -0.25$ mA/μm), and (d) $V_{DS} = -16.5$ V ($I_D = -0.63$ mA/μm).

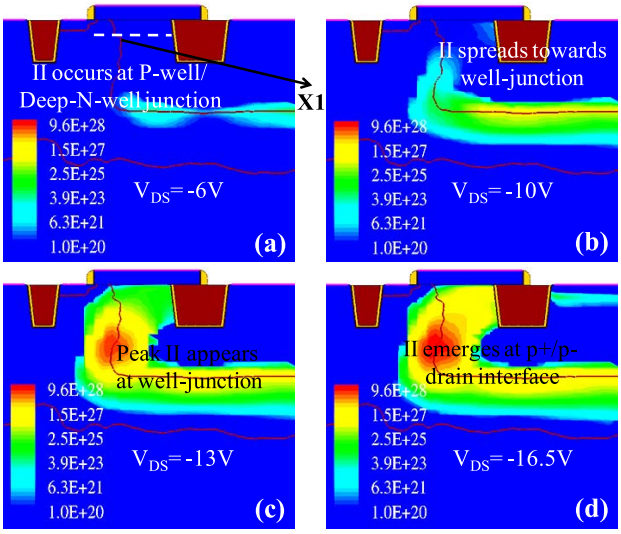

Fig. 7. II (1/cm^3) contour in STI-DePMOS device at $V_{GS} = 0$ V and (a) $V_{DS} = -6$ V ($I_D = -120$ nA/μm), (b) $V_{DS} = -10$ V ($I_D = -33$ μA/μm), (c) $V_{DS} = -13$ V ($I_D = -0.25$ mA/μm), and (d) $V_{DS} = -16.5$ V ($I_D = -0.63$ mA/μm). Location of lateral cutline X1 at 0.1-μm depth below the surface in the channel and overlap regions is shown, for use, in Fig. 14.

above $V_{DS} = -14$ V. The detailed physical breakdown mechanisms are explained next.

A. Detailed Mechanisms Causing Two-Stage Breakdown

1) Triggering of Stage-1 Breakdown: As shown in Fig. 4(b), the breakdown voltage of drain-to-substrate structure is ~ -5 V. At $V_{DS} = -4.9$ V [Fig. 5(a)], the substrate current rises above source current and then follows drain current as V_{DS} increases. Fig. 6 shows the conduction current density contours for different V_{DS} values at $V_{GS} = 0$ V. At $V_{DS} = -4.9$ V, the depletion region of p-well/deep-n-well junction J_2 spreads through deep-n-well layer to merge with the depletion region of deep-n-well/p-substrate junction J_3, hence, increasing the vertical current flow [Fig. 6(a)]. The simulated avalanche breakdown voltage of p-well/deep-n-well junction J_2 (if the bottom p-substrate is not included) is -12.6 V, which is much higher than the punchthrough voltage of -4.9 V. Since the peak doping concentration in the subsurface region of p-well is 10 times higher than the peak doping concentration of deep-n-well layer, fields are negligible at deep-n-well/p-substrate junction J_3 compared with the fields at the p-well/deep-n-well junction J_2. Since the current flow between drain and substrate is 2-D [Fig. 6(a) at $V_{DS} = -6$ V], the triggering of stage-1 breakdown at $V_{DS} = -4.9$ V is determined by the exact 2-D doping concentration profile of the p-well and deep-n-well layers. Due to punchthrough between J_2 and J_3 junctions, I_D rises from $\sim$1 pA to $\sim$50 μA level when V_{DS} is increased from -4.9 to -12 V [Fig. 6(b)]. The first-stage breakdown current is limited by the resistivity of deep-n-well layer (which is higher compared with that of p-well).

2) Onset of Impact Ionization: After punchthrough occurs, and V_{DS} is further increased, I_B increases due to the electrons generated from II (of junction leakage current) occurring primarily at junction J_2 [Fig. 7(a)]. At $V_{DS} = -5.5$ V, the II becomes significant at junction J_2 and I_B (the base current of vertical p-n-p formed by J_2 and J_3) rises above I_S due to II, but is still smaller than the substrate current [Figs. 5(a) and 6(a)]. In addition, I_B is negligible without any II [Fig. 5(a)]. As drain voltage increases toward $V_{DS} = -12$ V [Fig. 5(a)], peak field increases at both J_1 and J_2 junctions and II region, and hence, current flow spreads in deep-n-well layer [Figs. 6(b) and 7(b) at $V_{DS} = -10$ V] and in junction J_1 [Figs. 6(c) and 7(c) at $V_{DS} = -13$ V].

3) Triggering of Stage-2 Breakdown: As Fig. 5(a) shows at $V_{DS} = -12.1$ V, the second-stage breakdown is triggered and the drain current rises abruptly. This is due to avalanche breakdown at n-well/p-well junction J_1 [Figs. 6(c) and 7(c) at $V_{DS} = -13$ V].

Electron and hole current density contours in [Fig. 8(a)–(d)] are plotted at $V_{DS} = -13$ V and $V_{DS} = -16.5$ V to understand the behavior of current flow in the device and the terminal currents in the second-stage breakdown. In Fig. 9(a)–(d), J_H (hole current density) is plotted along a horizontal cutline X2 [Fig. 8(a)] at 20-nm depth below the silicon/gate-oxide interface and passing through p$^+$-source, n-well, and p-well regions.

At $V_{DS} = -12.1$ V, I_B rises abruptly due to impact ionized electrons and I_B follows I_D [Fig. 5(a)]. The electrons from both avalanching junctions J_1 and J_2 dominantly contribute to body current, whereas the holes dominantly contribute to drain and substrate currents [Fig. 8(a) and (b) at $V_{DS} = -13$ V].

Hole current density (J_H) is much higher than the electron current density (J_E) in p$^+$-source at $V_{GS} = 0$ V for V_{DS} up to -16.5 V (Fig. 8). Below $V_{DS} = -12.1$ V, the source current ($I_S > 0$) is subthreshold current due to hole diffusion, and holes flow from p$^+$-source through n-well to p-well ($J_{HX} > 0$) [Fig. 9(a)]. At $V_{DS} = -12.1$ V (the onset of the second-stage

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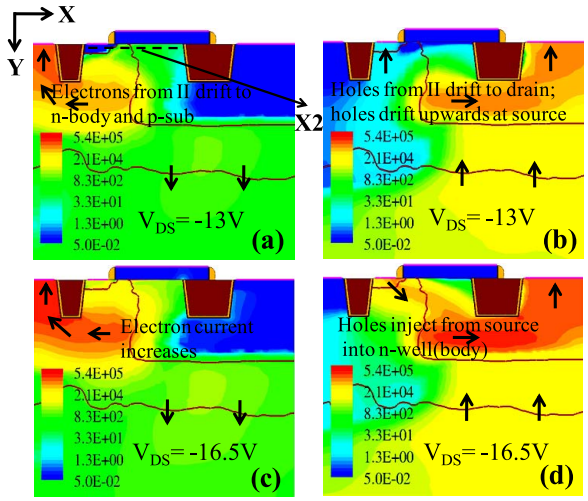

Fig. 8. Electron (a, c) and hole (b, d) current density (A/cm^2) contours in STI-DePMOS at $V_{GS} = 0$ V and (a) and (b) $V_{DS} = -13$ V and (c) and (d) $V_{DS} = -16.5$ V in the second-stage breakdown. Arrows: direction of electron and hole carrier flow. Contour range is kept the same as that of conduction current density in Fig. 6 for the sake of comparison.

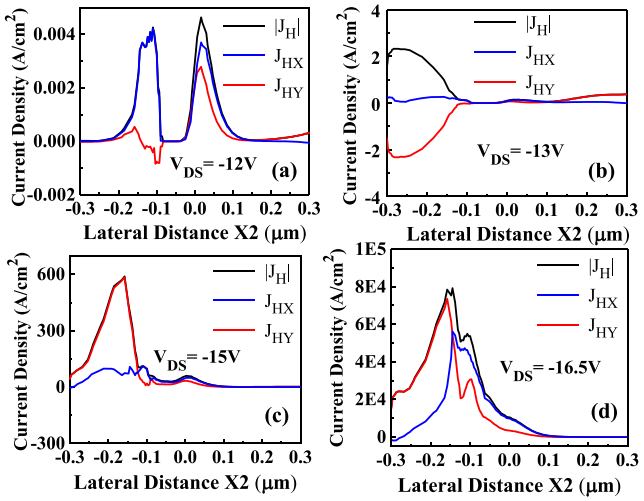

Fig. 9. Hole current density profiles ($|J_H|$: absolute value; J_{HX}: X-component of J_H; and J_{HY}: Y-component of J_H) along the lateral cutline $X2$ [Fig. 8(a)] at 20-nm depth below the surface and passing through only silicon regions between the two STI structures. The profiles are plotted for $V_{GS} = 0$ V and (a) $V_{DS} = -12$ V, (b) $V_{DS} = -13$ V, (c) $V_{DS} = -15$ V, and (d) $V_{DS} = -16.5$ V. The coordinate $X = 0$ is at the junction J_1 and $X = -0.09$ μm is the p$^+$-source/n-well junction.

breakdown), most of the electrons and holes due to II at J_1 are swept to n$^+$-body and p$^+$-drain, respectively; however, few holes reach the source terminal. At $V_{DS} = -13$ V, the J_E due to II outside the p$^+$-source region is much larger than J_H [Fig. 8(a) and (b)], the p$^+$-source (bottom side)/n-well junction is slightly reverse-biased. Hence, a small vertically upward directed hole drift current ($J_{HY} < 0$) [Fig. 9(b)] occurs across this junction. This explains why I_S turns negative at $V_{DS} = -12.1$ V [Fig. 5(a)]. However, such reversal in I_S is not seen at the onset of the avalanche breakdown at J_1, if the well doping profiles are such that hole current flow due to II hot spot at junction J_1 generates enough voltage drop in n-well to forward bias the p$^+$-source/n-well junction

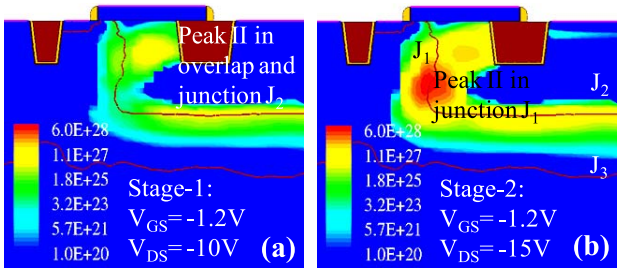

Fig. 10. II (1/cm^{3}s) contour in STI-DePMOS device at $V_{GS} = -1.2$ V and (a) $V_{DS} = -10$ V ($I_D = -0.24$ mA/μm) and (b) $V_{DS} = -15$ V ($I_D = -0.58$ mA/μm).

(and thereby preventing it to get reverse-biased), which triggers the injection of hole current from p$^+$-source into n-well (body).

At $V_{DS} = -16.5$ V, the current flowthrough junction J_1 primarily contributes to drain current relative to current flowthrough junction J_2 [Fig. 6(d)], and the peak II dominates at well junction J_1 [Fig. 7(d)]. However, a smaller II peak also appears at p$^+$-drain/p-well interface (which is the onset of Kirk effect). Hence, the body current dominates over substrate current [Figs. 5(a) and 8(c)]. At $V_{DS} = -14$ V, I_S reverses to positive value and rises as V_{DS} is increased up to $V_{DS} = -16.5$ V [Fig. 5(a)]. As the hole injection from p$^+$-source increases, $J_{HY} > 0$, $J_{HX} \sim 0$ at $V_{DS} = -15$ V [Fig. 9(c)] and $J_{HY} > 0$, $J_{HX} > 0$ at $V_{DS} = -16.5$ V [Fig. 9(d)]. Hence, the hole current flow above $V_{DS} = -14$ V is dominant from p$^+$-source toward junction J_1. However, the source (emitter) current is still smaller than the body (base) current [Fig. 5(a)]. Effectively, p$^+$-source-to-n-well junction does not get fully forward-biased and n-well is not yet conductivity modulated up to $V_{DS} = -16.5$ V. Hence, the parasitic bipolar p-n-p between p$^+$ source, n-well, and p-well is not triggered yet.

In addition, in ON-state ($V_{GS} = -1.2$ V), device shows two-stage breakdown [Fig. 5(b)]. Below $V_{DS} = -6$ V, channel hole inversion current dominates drain current. Above $V_{DS} = -6$ V, punchthrough occurs and so drain current increases. Above $V_{DS} = -10$ V, the II of channel current becomes significant in gate-to-drain overlap region and also in junction J_2 [Fig. 10(a)]. At $V_{DS} = -12.8$ V, the avalanche breakdown occurs in well junction J_1, and the second-stage breakdown is triggered [Fig. 10(b)]. In addition, a cross-over is seen between body and substrate currents [Fig. 5(b)]. Thus, the occurrence of two-stage breakdown leads to poor breakdown voltage in STI-DePMOS (compared with STI-DeNMOS), which severely reduces the SOA of I/O device operation.

B. Comparison of Breakdown Physics Between STI-DePMOS and STI-DeNMOS Devices

Two STI-DeNMOS devices [structure shown in Fig. 1(a)] of different channel lengths (0.1 and 0.45 μm) are used to study breakdown physics and compared with that of STI-DePMOS. Their output characteristics are shown in Fig. 11(a). Their OFF-state breakdown voltage is defined as V_{DS} voltage at which the drain current reaches 100 pA/μm (which is well above prebreakdown leakage current). The body current

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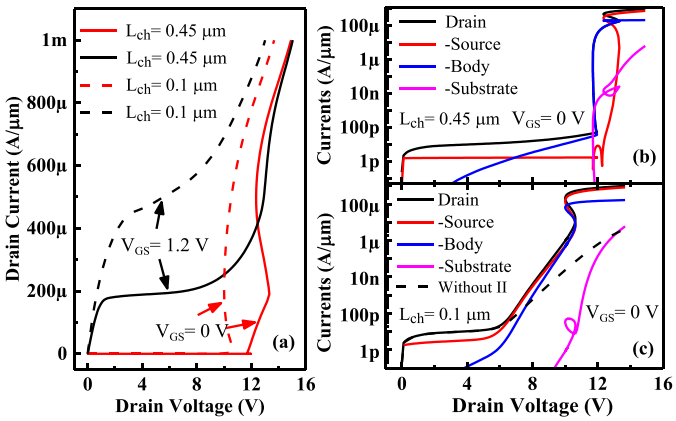

Fig. 11. (a) Simulated I_D–V_D characteristics of two STI-DeNMOS devices of 0.1- and 0.45-μm channel lengths (other layout parameters are given in Table I) with and without II model. Simulated currents versus drain voltage (on log scale) at $V_{GS} = 0$ V of STI-DeNMOS device with (b) 0.45- and (c) 0.1-μm channel length. Dotted line: drain current without II model (source-to-drain punchthrough current).

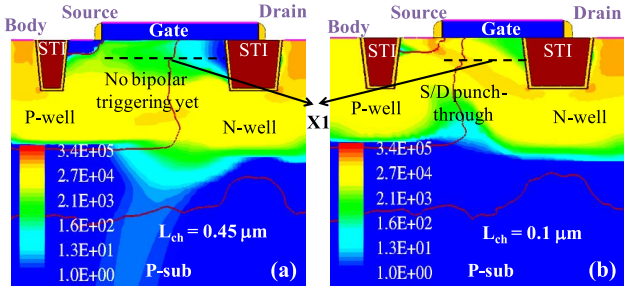

Fig. 12. Conduction current density (A/cm^2) contour in two STI-DeNMOS devices (different channel lengths) at $V_{GS} = 0$ V and $I_D = 0.1$ mA/μm. Location of lateral cutline X1 at 0.1-μm depth below the surface in channel and overlap regions is shown, for use, in Fig. 14.

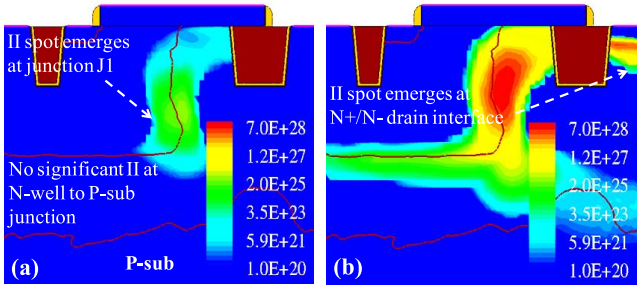

Fig. 13. II (1/cm^{3}s) contour in STI-DeNMOS device with 0.45-μm channel length at $V_{GS} = 0$ V and (a) $I_D = 100$ nA/μm and (b) $I_D = 1$ mA/μm. Peak II occurs at n-well/p-well junction. Due to base-push effect, II spot emerges at n^+/n^- drain interface.

in the larger channel length device shows abrupt increase at $V_{DS} = 11.9$ V in Figs. 11(b) and 12(a) due to avalanche breakdown at n-well/p-well junction at $V_{DS} = 11.9$ V [Fig. 13(a)]. The shorter channel length device breaks down due to source-to-drain punchthrough at $V_{DS} = 6.8$ V [Figs. 11(c) and 12(b)]. This is confirmed since the device breaks even when II model is switched OFF [Fig. 11(c)]. Fig. 13(b) shows that the peak II spot occurs at both well junction and n^+ drain/n-well interface at high drain current level of $I_D = 1$ mA/μm. Substrate current is much smaller in both devices, because field at junction J_4 is much smaller

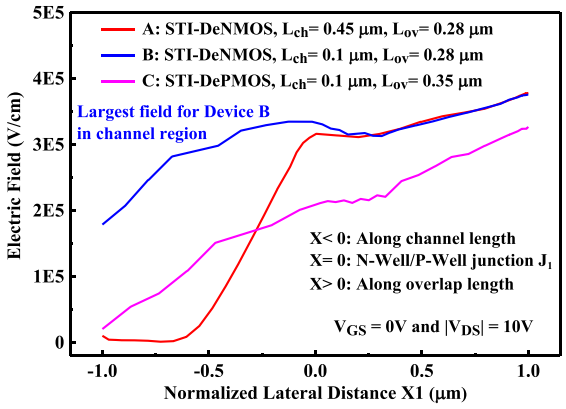

Fig. 14. Electric field (V/cm) profile versus normalized lateral distance at 0.1-μm depth below the surface of two STI-DeNMOS and one STI-DePMOS devices [cutline locations X1 shown in Figs. 7(a) and 12(a) and (b)]. Difference in field distribution between $L_{ch} = 0.1$-μm STI-DeNMOS and $L_{ch} = 0.1$-μm STI-DePMOS devices are visible.

than junction J_1. Bipolar is fully ON when source current becomes significant compared with body current (above $I_D = 0.4$ mA/μm). Therefore, breakdown in STI-DeNMOS is determined by the breakdown characteristics of lateral n-well/p-well junction and does not have two-stage behavior.

Fig. 14 compares the lateral field profiles in channel and overlap regions (at 0.1-μm depth below the silicon surface) in two STI-DeNMOS and one STI-DePMOS devices at $V_{GS} = 0$ V and $|V_{DS}| = 10$ V. Since this bias point is the prebreakdown region for device A, fields are much smaller in channel region compared with the overlap region. But, for device B, this is well after source-to-drain punchthrough occurs and so much higher field is seen in channel than devices A and C. For device C, this bias is inside the first-stage breakdown regime, but the field is smaller than device B of the same channel length and no source-to-drain punchthrough occurs. Therefore, 100-nm channel length is critical to n-type DeMOS devices.

Figs. 15 and 16 show OFF-state field profiles in STI-DeNMOS (of larger channel length) and STI-DePMOS, respectively. In STI-DeNMOS, the peak field along the lateral cutline rises as long as drain voltage increases until the onset of parasitic bipolar triggering after junction breakdown, but then falls after V_{DS} snapbacks at 13.3 V ($I_D = 0.19$ mA). In addition, field distribution expands in the overlap region at higher current levels. Along the vertical cutline, the peak field emerges near n^+ drain/n-well interface at high current levels due to base-push effect [Fig. 13(b)]. This aids in the relaxation of peak field in junction J_1. In STI-DePMOS, the peak field first rises then falls along the lateral cutline after the triggering of second breakdown.

In STI-DePMOS, the stretching of field distribution in the overlap region is even greater than in STI-DeNMOS (since junction J_2 is in proximity to J_1 and p^+ drain). Peak field along vertical cutline is centered on p-well-to-deep n-well junction J_2 and a smaller peak appears at p^+ drain/p-well interface. High-field region spreads inside deep n-well, which is the lightly doped side of the junction J_2. Because of the highest peak field at lateral n-well/p-well junction in both

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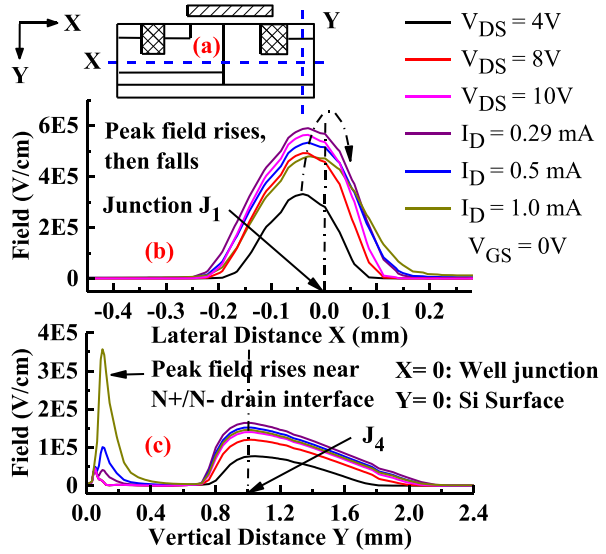

Fig. 15. (a) Cross section of STI-DeNMOS with locations of lateral cutline at 0.4-μm depth below the surface and vertical cutline through the middle of drain diffusion region. Electric field profiles along (b) lateral cutline X and (c) vertical cutline Y at $V_{GS} = 0$ V and at different V_{DS} and I_D levels in prebreakdown and postbreakdown regimes. The coordinate $X = 0$ is at the well junction J_1 and $Y = 0$ at the silicon surface.

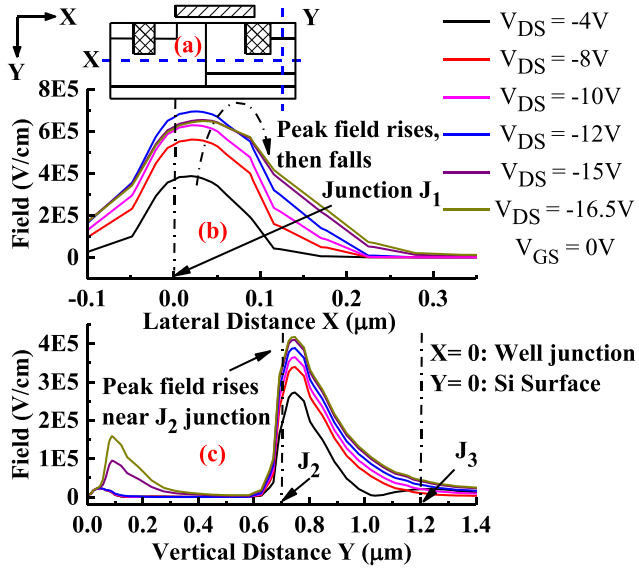

Fig. 16. (a) Cross section of STI-DePMOS with locations of lateral cutline at 0.5-μm depth below the surface and vertical cutline through the middle of drain diffusion region. Field profiles along (b) lateral cutline X and (c) vertical cutline Y at $V_{GS} = 0$ V and $V_{DS} = -4, -8, -10, -12, -15$, and -16.5 V. The coordinate $X = 0$ is at the well junction J_1 and $Y = 0$ at the silicon surface.

STI-DeNMOS [Fig. 15(b)] and STI-DePMOS [Fig. 16(b)] (relative to junction J_2), II dominates there and contributes to avalanche breakdown in both devices (the second-stage breakdown in STI-DePMOS). The different behaviors of spatial field distribution are reflected in I–V characteristics at high current levels.

IV. Conclusion

Experimentally observed two-stage breakdown characteristics in STI-DePMOS device were analyzed using TCAD simulations. The first-stage breakdown is due to punchthrough between the junctions of the three vertical layers, p-well, deep n-well, and p-substrate. The second-stage breakdown is due to an avalanche breakdown at the lateral n-well/p-well junction. The breakdown mechanisms in STI-DePMOS were compared with STI-DeNMOS device structures. The analyses show that the two-stage breakdown is the fundamental characteristic of p-type DeMOS devices with lowly doped deep n-wells. Due to p-well/deep-n-well junction in proximity to p^+ drain, the second-stage breakdown mechanisms in STI-DePMOS differ from STI-DeNMOS device breakdown. This understanding is useful to develop methods to optimize the SOA of p-type DeMOS devices. Future work may consider optimizing CMOS process for both core logic and I/O devices.

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