Fin Enabled Area Scaled Tunnel FET

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Abstract—While keeping the technological evolution and commercialization of FinFET technology in mind, this paper discloses a novel concept that enables area-scaled or vertical tunneling in Fin-based technologies. The concept provides a roadmap for beyond FinFET technologies, while enjoying the advantages of FinFET-like structure without demanding technological abruptness from the existing FinFET technology nodes to beyond FinFET nodes. The proposed device at 10-nm gate length, when compared with the conventional vertical tunneling FET or planar area-scaled device, offers 100% improvement in the ON-current, 15× reduction in the OFF-current, 3× increase in the transconductance, 30% improvement in the output resistance, 55% improvement in the unity gain frequency, and more importantly 6× reduction in the footprint area for a given drive capability. Furthermore, the proposed device brings the average and minimum subthreshold slope down to 40 and 11 mV/decade at 10-nm gate length. This gives a path for beyond FinFET system-on-chip applications, while enjoying the analog, digital, and RF performance improvements.

Index Terms—Area-scaled tunnel FET (TFET), FinFET, green TFET, line tunneling, point tunneling, Sandwiched Tunnel Barrier FET (STBFET), vertical tunneling FET.

I. INTRODUCTION

IT TOOK almost 20 years for FinFET technology to mature and become a reality for semiconducting products by replacing planar devices. However, as the technology evolution does not allow abrupt changes, the FinFETs too enjoy the advancements from planar nodes, such as high-κ metal gate, raised/episource–drain, strained-silicon, and gate last process. This recent technological evolution has raised two serious questions: 1) what would replace Si or SiGe FinFET and 2) would there be serious change in technological evolution while scaling below 10-nm nodes? To answer the first question, various competing concepts, such as quantum well channel FinFET, III–V FinFET, nanowire FET, and tunnel FETs (TFETs), are floating around. Given the fact that the FinFET and nanowire FET devices are limited by thermionic injection ($SS_{min} = 60$ mV/decade), TFETs are proposed to replace the FinFET/nanowire FET devices beyond 11-nm node. In last 15 years, there have been extensive investigations on TFET devices for ultralow-power and high-performance operation. Tunneling phenomena allows sub-60-mV subthreshold operation thereby has a potential to scale leakage and

improve ON-current at lower supply voltages. The very early TFET concept (gated p-i-n diode) despite several advancements, such as SiGe source, low-κ drain spacer, high-κ source spacer, low drain doping, highly doped source, abrupt source junction profiles, post silicidation implant, bandgap engineering, and double-gate architectures, suffered from extremely low ON-currents. This was primarily attributed to limited tunneling cross section/area available in gated p-i-n diodes (also known as point tunneling FETs) [1]–[9]. To overcome this problem, vertical tunneling [10], [11]/area-scaled tunneling [12], [13]/line tunneling [14]–[16] devices were proposed, which theoretically show significantly improved ON-current, reduced leakage, and subthreshold slope (SS), attributed to increased tunneling cross section and gate-field-aligned binary tunneling mechanism [17], [18]. Concerns related to trap assisted tunneling (TAT) and diffused junction profiles, which adversely affects ON current, increases leakage and SS of vertical tunneling devices, have also been addressed recently [19], [20]. However, the bigger question is how to take this concept to Fin-based technologies, allowing smooth transition from FinFET technology to Fin-based vertical TFETs, while enjoying the benefits of FinFET architecture.

This paper, while addressing the question raised above, proposes a novel Fin-enabled vertical or area-scaled tunneling FET for sub-10-nm channel length operation. We have shown that the gate-field aligned tunneling in Fin-based architecture enjoys improved ON-current due to increased electric field and band alignment, which is attributed to increased gate control over the tunneling region. The 3-D nature of Fin-based architecture further enjoys increased ON-current per footprint area, when compared with its planar counterpart. Furthermore, it also improves the SS and OFF-current due to increased gate control over tunneling region and channel, respectively. This eventually results in improved circuit's figure of merit.

This paper is organized as follows. To emphasize the validity and accuracy of our estimations, the details of the TCAD setup, the calibration flow, and the calibration results are given in Section II. Section III discloses the proposed device and its physics of operation, and explains technological predictions. Section IV comprehends how the proposed device is unique when compared with its planar counterpart and shows the advantages of the proposed device. Finally, the conclusion is drawn in Section V.

II. DEVICE TCAD STRATEGY

In the past few years, there has been some level of skepticism on the computation of tunneling field-effect phenomena by using semiclassical methods. Therefore, its worth highlighting that a rigorous calibration approach has been

followed for the device TCAD setup used in this paper, thanks to the nonlocal tunneling approach with two-band dispersion and quantum confinement (QC), and a two-step calibration strategy used in this paper—as explained in the subsequent sections.

A. Band-to-Band Tunneling and Quantum Confinement

To accurately capture band-to-band tunneling phenomena, a nonlocal band-to-band tunneling approach, as proposed by Ieong *et al.* [21], however, with several enhancements [22], is followed in this paper. This approach uses Wentzel–Kramer–Brillouin (WKB) approximation with two-band dispersion relation, while using electron–hole wave-vector throughout the tunneling path for evaluating the tunneling probability. The impact of carrier velocity on the transmission coefficients across the interface was also captured. Moreover, the QC was accounted by self-consistent solution of Schrödinger equation. Our simulations with QC, when compared with the simulation results without QC, show shift of turn-ON voltage by 0.1–0.3 V, like reported recently in [23]. The simulation approach is as follows. First, the local wave numbers are evaluated using the following equations [22]:

$$\kappa_{C,v}(r, E) = \sqrt{2m_C(r)|E_{C,v}(r) - E|}\,\Theta[E_{C,v}(r) - E]/\hbar \quad (1)$$

$$\kappa_{V,v}(r, E) = \sqrt{2m_V(r)|E_{V,v}(r) - E|}\,\Theta[E_{V,v}(r) - E]/\hbar \quad (2)$$

where E is the energy of the particle and $m(r)$ is the effective tunneling mass. From these local wave numbers, the tunneling probability using WKB approximation is calculated

$$\Gamma_{CC,v}(u, l, E) = T_{CC,v}(l, E)$$
$$\cdot \exp\left(-2\int_l^u \kappa_{V,v}(r, E)dr\right) T_{CC,v}(u, E) \quad (3)$$

$$\Gamma_{VV,v}(u, l, E) = T_{VV,v}(l, E)$$
$$\cdot \exp\left(-2\int_l^u \kappa_{V,v}(r, E)dr\right) T_{VV,v}(u, E) \quad (4)$$

where T_{CC} and T_{VV} are the transmission coefficients. Finally, from the tunneling probabilities evaluated above, the tunneling current density is calculated by integrating the transmission probabilities over the entire spacial and energy range across the tunneling interfaces.

B. Calibration Approach

A well-calibrated device TCAD setup, while using a two-step calibration strategy, was used. The TCAD setup was first calibrated against drift-diffusion transport, with thin-body mobility model and quantum corrections at the oxide–Si channel interface. Since silicon–germanium source has been demonstrated in this paper, to ensure the accuracy of the TCAD results, the mobility and tunneling models were calibrated against the experimental characteristics of ultrathin-body SiGe FET, as shown in Fig. 1(a) [24]. Furthermore, the tunneling models were calibrated against the SiGe TFET
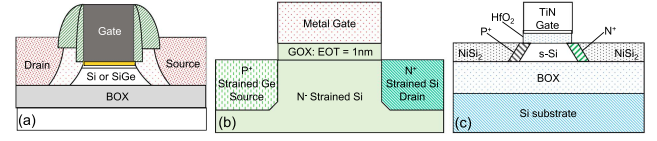

Fig. 1. Ultrathin-body MOSFET and TFET devices referred in this paper for TCAD calibration. (a) SiGe MOSFET reported in [24]. (b) SiGe TFET reported in [25]. (c) Cross-sectional view of the 3-D point TFET reported in [26].
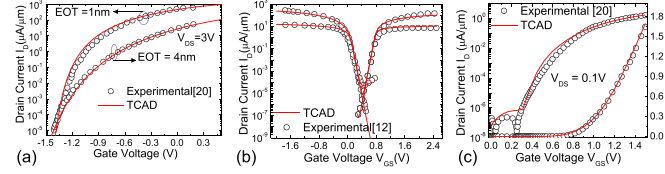

Fig. 2. Calibration of (a) drift-diffusion transport and mobility model with QC against the SiGe MOSFET reported in [24]. (b) Barrier tunneling and TAT model parameters against a Ge source TFET device reported in [25]. (c) Second stage fine calibration of barrier tunneling and TAT model parameters with QC against a recently reported 3-D point TFET device reported in [26].

shown in Fig. 1(b), which was earlier reported in [25]. Device design, dimensional parameters, and doping profiles were borrowed from [24] and [25] for precise calibration. Good agreement between the simulations and the experiments, with less than 1% error, is shown in Fig. 2(a) and (b). Note that the other mobility models, such as effect of gate field, velocity saturation, doping dependence, carrier–carrier scattering, and bandgap narrowing model, were also considered for calibration and subsequently used in all the simulations. It is worth highlighting that the nonlocal BTBT simulation approach used in this paper accounts for tunneling across all possible interfaces, junctions, and corners.

As the second step, the calibrated TCAD setup was validated for the 3-D TFET device proposed in [26], as shown in Fig. 1(c). Good agreement between the simulated and experimental data, with less than 20% error, was found. Further, the model parameters were fine-tuned to match the simulations with the experimental data, with less than 2% error, as shown in Fig. 2(c). Doping profiles, device geometrical parameters, Effective Oxide Thickness (EOT), and gate metal work function, as reported in [26], were reproduced for calibration accuracy. It is worth highlighting that the impact of TAT was captured by using Shockley–Read–Hall (SRH) recombination along with field-enhanced TAT model. TAT has been reported several times to be a major contributor to the OFF-state leakage in TFET devices. This is attributed to high electric fields across the tunneling interface [27], which mitigates the subthreshold operation by excess carrier generation and increases the SS. The key model parameters are disclosed in Table I. For completeness, we have reported the calibrated model parameters with and without QC effect.

III. PROPOSED AREA-SCALED Fin-TFET AND TECHNOLOGICAL PREDICTIONS

Fig. 3 shows the proposed area-scaled Fin-TFET (ASF-TFET). An area-scaled tunneling concept is known for
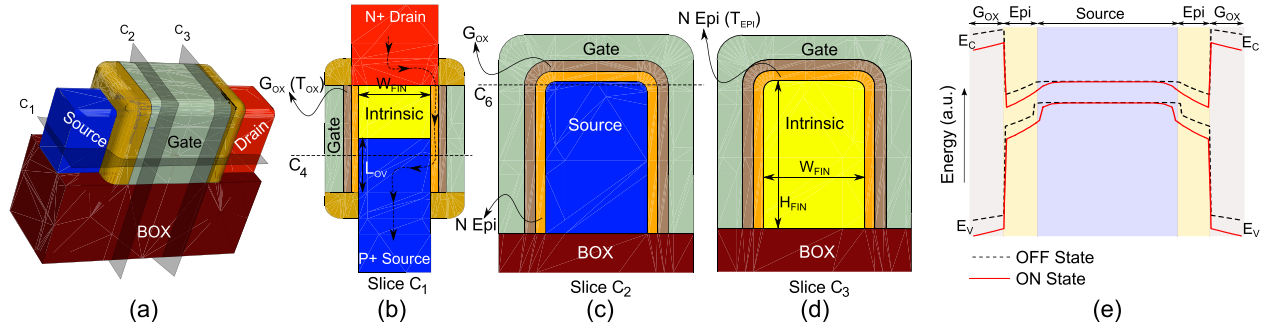
Fig. 3. Proposed ASF-TFET device. (a) 3-D or isometric view. (b)–(d) 2-D view/slice along C_1, C_2, and C_3 planes, respectively. (e) Conduction and valance band diagram showing band alignment and bending under OFF- and ON-states of the proposed device along cut line C_4.

TABLE I

CALIBRATED PARAMETERS OF THE BARRIER TUNNELING MODEL USED FOR THE 3-D TCAD SIMULATIONS. HERE, m_{te} IS THE ELECTRON TUNNELING MASS, m_{th} IS THE HOLE TUNNELING MASS, τ_{max} IS THE MAXIMUM SRH RECOMBINATION TIME, AND $\hbar\omega$ IS THE EFFECTIVE PHONON ENERGY

Parameter	Calibrated Value w/o QC	Calibrated Value $w/$ QC
m_{te}	$0.185 * m_0$	$0.12 * m_0$
m_{th}	$0.275 * m_0$	$0.23 * m_0$
τ_{max}	2×10^{-5} s	4×10^{-6} s
$\hbar\omega$	0.063 eV	0.046 eV

Fig. 4. Representative process flow for the proposed ASF-TFET device.

the past few years by terminologies, namely, Sandwiched Tunnel Barrier FET (STBFET), green TFET, and line TFET. The idea of area tunneling is to enable tunneling along the gate electric field to enhance the tunneling cross-sectional area. The proposed device enables the area-scaled tunneling in a Fin-based technology, which allows smooth transition from FinFET to Fin-TFET technology without significant technological changes. Fig. 3(a) shows the 3-D (as simulated) view of the proposed device, whereas Fig. 3(b)–(d) shows the 2-D slices of the proposed device along the planes C_1, C_2, and C_3, respectively. The proposed device has a Fin-based structure with p+ source and n+ drain with a lightly (n) doped epitaxial layer partially over the source. Furthermore, the lightly doped epitaxial region is wrapped from three directions by a gate-stack (dielectric and metal stack), which enables channel formation in the epitaxial region and enhances tunneling from source to the channel. It is worth highlighting that in the proposed device, epitaxial region hosts the channel or inversion layer and tunneling takes place from the source to epitaxial region (vertical tunneling) when gate voltage is applied. Such a device architecture improves the tunneling cross-sectional area $A_{\text{Tunnel}} = L_{\text{OV}} \times (2H_{\text{Fin}} + W_{\text{Fin}})$, and reduces the tunneling barrier ($T_{\text{Barrier}} < T_{\text{Epi}}$), while reducing the device footprint. Moreover, Fin structure improves the control over the channel region, which improves the OFF-state behavior. However, it also enhances the electric field under ON-state condition and increases the drive current. Smaller device footprint, higher

ON-current, and improved subthreshold operation increase the ON-current per device footprint area and reduce the power dissipation (the details are in Section IV).

Fig. 3(e) shows the band diagram along the C_4 slice marked in Fig. 3(b), which shows the conduction and valance band bending under ON- and OFF-states of the device. At $V_G = 0$ (dotted lines), zero alignment between the valence band of source and the conduction band of epitaxial region clearly reveals an OFF-state behavior, attributed to lack of tunnel states across the interface. When a gate voltage is applied, the conduction band of the epitaxial region aligns with the valence band of the source, allowing tunneling of electrons from source to the epitaxial region. These carriers are swept away, via the channel formed in the epitaxial region under the gate, by the drain electric field. In this way, current flows from drain through epitaxial layer to source, as marked in Fig. 3(b). Reader should note that the tunneling barrier width of the proposed device is less than that of the epitaxial layer thickness, which is evident from the following relation: $T_{\text{Barrier}} = T_{\text{Epi}} - T_{\text{Inv}}$, where T_{Inv} is the inversion region thickness. This allows greater control on the tunneling barrier width.

The next question is whether this device can be fabricated using the standard CMOS process flow or not. To answer this question, a process flow is proposed in Fig. 4. Clearly, gate last process and the low temperature local epigrowth process can be exploited to enable the proposed device in the standard FinFET CMOS process line.

A. Motivation for Low Bandgap Source

The ON-current improvement using a SiGe source has previously been demonstrated in [1]–[11]. The recent
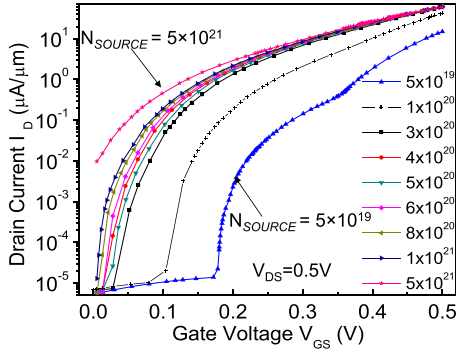
Fig. 5. Drain current versus gate voltage as a function of source region doping of the proposed device. OFF-current is mostly unchanged up to a certain doping level; however, ON-current and SS significantly improve as the source doping was increased. Device design parameter values used for this investigation are: H_{FIN} = 40 nm, EOT = 0.4 nm, T_{EPI} = 2 nm, W_{FIN} = 10 nm, L_G = 20 nm, N_{EPI} = 3 × 10^{19}, L_{OV} = 40 nm, and Ge% = 30.

technological establishments for controlled SiGe growth up to 45% Ge content promote the use of SiGe as a source material in TFETs. The SiGe source in principle, due to its lower bandgap, reduces the barrier height, lowers the effective mass, and enhances the electric field at the source–epi region interface. Higher interface electric field lowers the tunneling distance, which together with reduced barrier height and effective mass, and improves the tunneling probability [28] (5), without significantly affecting the leakage characteristics

$$T_{BTBT} = \exp\left(-\frac{4\lambda\sqrt{2m^*E_g^3}}{3q\hbar(E_g + \Delta\phi)}\right). \qquad (5)$$

B. Source Engineering: A Critical Requirement

We have found that the source region doping is a very critical device design parameter, especially for area scaled concepts. Fig. 5 shows I_D versus V_G characteristics of the proposed device for different source region doping concentrations with 30% germanium content. A clear ON-current improvement by increasing the source doping is evident from Fig. 5 without significantly affecting the leakage current before onset of band-to-band tunneling. Of course, lowering of threshold voltage can be seen, which in-turn is advantageous for the TFET device in conjunction with QC effects. This behavior is attributed to an increased electric field across the source–epi interface as a function of source doping, which in-turn reduces the depletion width and causes the valance band of source to move upward. These two effects reduce the tunnel barrier width and move the conduction band in the epitaxial region relatively down. This eventually reduces the turn-ON voltage of the device and improves the ON-current by increasing the tunneling probability. As the epitaxial layer is depleted by the gate electric field at $V_G = 0$, no significant change in the OFF-current up to a certain doping can be seen. Above the source doping of 1×10^{21}, an alignment of valance (source side) and conduction (channel) bands under OFF-state condition was observed, which in-turn increases the leakage current at $V_G = 0$ V. Above a certain source doping, which also

depends on the Ge%, an exponential increase in the leakage current with respect to the source doping was observed. On the other hand, ON-current does not increase significantly due to limited tunneling width above $N_{Source} = 1 \times 10^{21}$ with Ge% = 30.

The germanium % of the SiGe source is another key parameter that seriously affects the SS, ON, and OFF currents. As mentioned earlier, increasing Ge% reduces the bandgap, hence improves the tunneling current [Fig. 6(a)]. However, at the same time, it increases the OFF-current if Ge% is sufficiently high, which is attributed to an early alignment of conduction and valence bands. Moreover, decreased bandgap also results in an increased SRH recombination [Fig. 6(b)], thereby increasing the drain-to-source leakage. Fig. 6(a) shows the I_D versus V_G characteristics as a function of Ge mole fraction, which clearly shows a significant improvement in ON-current with very small change in leakage current up to 45% of Ge content. Moreover, no significant increase in the channel leakage can be seen for the germanium content up to 45% for the source doping of 5×10^{20}.

C. Epitaxial Layer: What Role Does it Play?

As explained earlier, ON-current improvement by increasing source doping is limited up to a certain doping concentration, which is a function of Ge%. In order to improve device's performance further, epitaxial layer region can be engineered carefully. There are three parameters as far as the epitaxial layer engineering is concerned: 1) doping (N_{Source}); 2) its thickness (T_{Epi}); and 3) its overlap with source (L_{OV}). An increased n-type doping in this region results in higher electric field (i.e., smaller tunneling width), across the tunnel junction. Moreover, it brings conduction band in the epitaxial region closer to the valance band of source. This results in an increase in ON-current, as shown in Fig. 7(a), at the cost of a minimal leakage current increase, which is attributed to field enhanced TAT across the junction. Moreover, increasing the epitaxial region doping lowers the conduction band edge relative to source. Hence, above a given doping, as a function of epiregion thickness, leakage current increases exponentially as shown in Fig. 7(b).
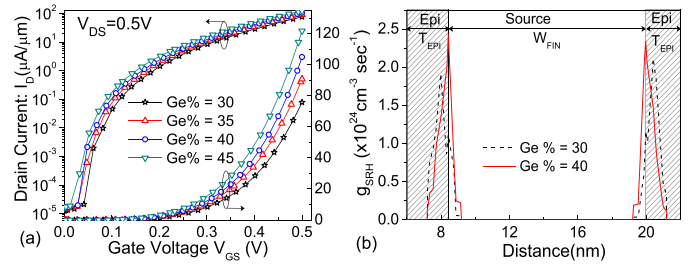

Fig. 6. (a) Drain current versus gate voltage as a function of Ge mole fraction of SiGe source of the proposed device. Left: log scale. Right: linear scale. OFF-current is mostly unchanged; however, ON-current greatly improves with the increased Ge mole fraction, which justifies the need for low bandgap source. Shift of I_D versus V_G characteristics toward the left is attributed to lowering of conduction band energy, which reduces the turn-ON voltage. Device design parameter values used for this investigation are: H_{FIN} = 40 nm, EOT = 0.4 nm, T_{EPI} = 2 nm, W_{FIN} = 10 nm, L_G = 20 nm, N_{EPI} = 3 × 10^{19}, L_{OV} = 20 nm, and N_{Source} = 5 × 10^{20}. (b) Impact of Ge mole fraction on SRH generation rate. g_{SRH} is the SRH generation rate.
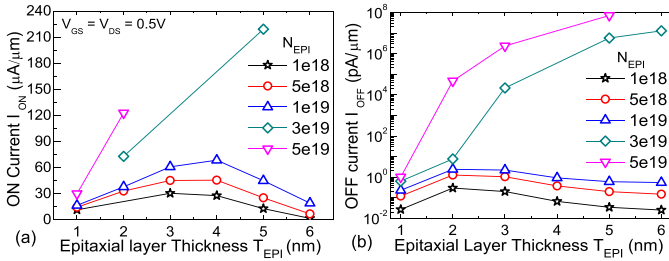
Fig. 7. Impact of epitaxial region engineering over (a) ON-current and (b) OFF-current. Device design parameter values used for this investigation: $H_{FIN} = 40$ nm, EOT $= 0.4$ nm, $W_{FIN} = 10$ nm, $L_G = 20$ nm, $L_{OV} = 20$ nm, and $N_{Source} = 5 \times 10^{20}$.

Fig. 9. Proposed device's (a) ON-current and (b) OFF-current as a function of gate to source overlap length (L_{OV}). Device design parameter values used for this investigation are: $H_{FIN} = 40$ nm, EOT $= 0.4$ nm, $W_{FIN} = 10$ nm, $L_G = 20$ nm, $L_{OV} = 20$ nm, $T_{EPI} = 3 \times 10^{19}$, and $N_{Source} = 5 \times 10^{20}$.
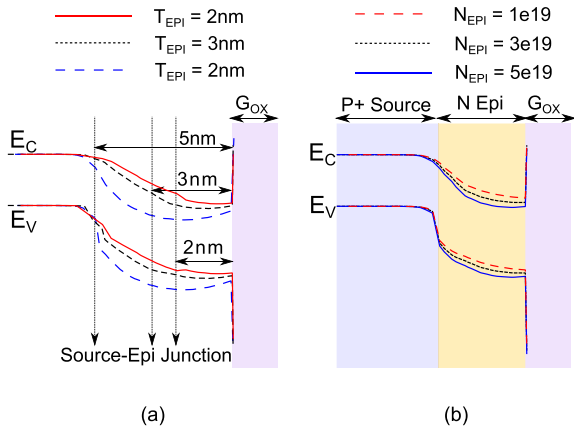

Fig. 8. Conduction and valance band diagram showing band alignment and bending under OFF-state of the proposed device along cut line C_4 as a function of (a) epilayer thickness for $N_{EPI} = 3 \times 10^{19}$ and (b) epilayer doping for $T_{EPI} = 2$ nm.

Fig. 10. Change in electric field profile, along C_6, as a function of Fin shape or curvature at its top.

The second engineering parameter is the epitaxial region thickness (T_{Epi}), which defines the tunneling width under ON-state condition. In principle, we would like to keep the tunneling width as low as possible in order to improve the ON-current; however, lowering epitaxial region thickness, to reduce tunneling width, causes serious mobility degradation due to an increased field enhanced scattering. These competing behaviors result in an optimum epitaxial region thickness for a given epiregion doping. At lower T_{Epi}, current falls due to increased scattering; however, the same at higher T_{Epi} is attributed to increased tunneling width. It is worth highlighting that above a certain epiregion doping, it is hard to deplete the channel completely by gate field, which attributes to an OFF-state tunneling between the source and the epitaxial layer, as evident from the band diagrams along the slice C_4 in Fig. 7. This eventually results in an increased leakage for highly doped epiregion with an increased T_{Epi}.

The third engineering parameter is source to epiregion overlap length (L_{OV}). For area-scaled TFET concepts, L_{OV} determines the tunneling area, and thereby the ON-current of the device. Increasing L_{OV} linearly increases the ON-current, as the tunneling area increases linearly, which is shown in Fig. 9(a). However, for higher L_{OV}, ON-current increases sublinearly, which is attributed to an increased channel resistance of the device that leads to nonuniform
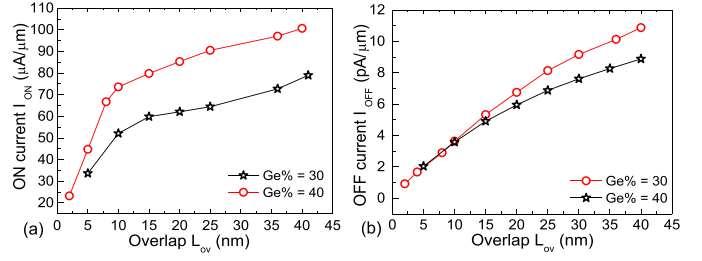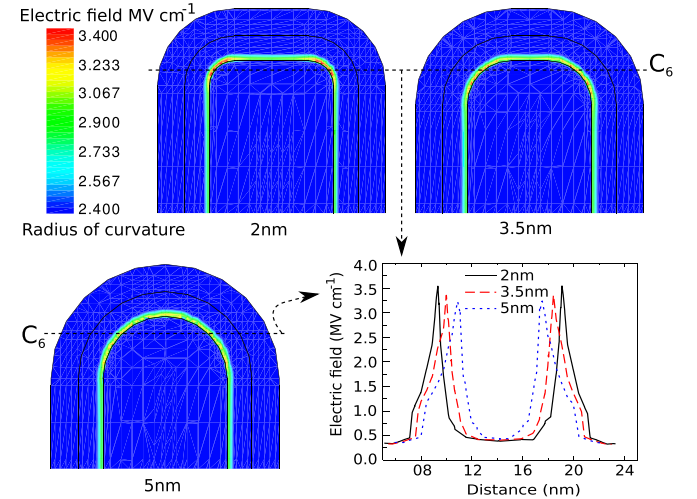
electric field across the overlap area. Finally, at very high L_{OV}, ON-current saturates and is limited by MOS channel in series with tunnel junction. It is worth highlighting that OFF-current also increases linearly due to an increased tunneling cross-sectional area in which the field enhanced TAT dominates. This is clearly shown in Fig. 9(b).

D. Importance of the Fin Shape and Device Layout

Fin edge radius, Fin shape, Fin width, and its height have been discussed at different occasions to be important device design parameters for FinFETs. Therefore, similar characteristics and impact of respective parameters on the proposed ASF-TFET design are worth investigating. Figs. 10 and 11(a) show the electric field distribution for different edge top radius (r_{Cur}) across the C_6 slice of the device and the device's I_D versus V_G characteristics as a function of fin edge radius, respectively. It is clear from Figs. 10 and 11(a) that the Fin edge radius plays an important role in the proposed ASF-TFET design. As the Fin edge radius is decreased from 5 to 2 nm, the peak electric field at the source–channel interface near the Fin edge increases by 10% (Fig. 10). This eventually results in a 10% increase in ON-current without affecting the leakage characteristics (Fig. 11). These results clearly show the impact of an increased electrostatic control
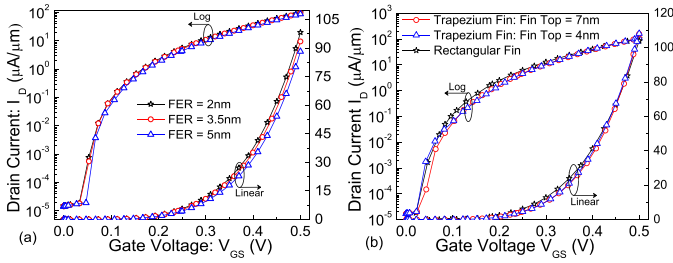
Fig. 11. Input characteristics of the proposed device as a function of (a) Fin top curvature and (b) its shape.
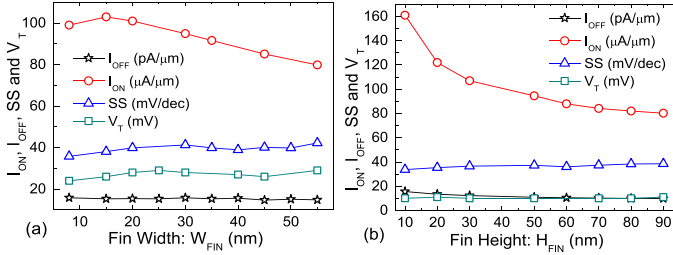

Fig. 12. Impact of (a) Fin width and (b) Fin height on the OFF-current, ON-current, SS, and V_T of the proposed device.

on the channel and the tunnel junction, which justify the importance of Fin enablement of area-scaled TFET. Similarly, the effect of Fin shape on the I_D versus V_G characteristics of the proposed device was investigated, as shown in Fig. 11(b). To study this, trapezium-shaped Fins with bottom width of 10 nm and top region's widths of 10, 7, and 4 nm were simulated. Interestingly, the device's characteristics were found to be robust against the Fin shape.

Fig. 12(a) and (b) shows the impact of Fin width and Fin height, respectively. Interestingly, OFF-current, threshold voltage, and SS do not change as a function of Fin width and Fin height, however, ON-current significantly improves as the Fin width and Fin height are scaled from 55 and 90 nm to 15 and 10 nm, respectively. This is attributed to an improved electrostatic control over the tunneling interface as the Fin width and Fin height are scaled down, which further justifies the relevance of Fin technology for area-scaled TFET concept.

IV. ASF-TFET VERSUS PLANAR COUNTERPART

In the past, a range of planar area-scaled TFET devices have been proposed by various groups, namely, vertical tunneling FET [10], [11]/STBFET [12], and [13]/line tunneling FET [14]–[16], which theoretically show significantly improved ON-current, reduced leakage, and SS, attributed to increased tunneling cross section [17], [18] when compared with point TFET devices. The planar area-scaled TFET concept can be generalized, as shown in Fig. 13(a). This section presents a comparison of the proposed device with its planar counterpart and demonstrates the advantages of Fin geometry over the planar device. For completeness of work, a well designed point TFET device [Fig. 13(b)], as recommended by various works [1]–[9], is also considered for the comparison.

Fig. 14 compares the drain current per unit area extracted from 3-D TCAD simulations of the proposed ASF-TFET
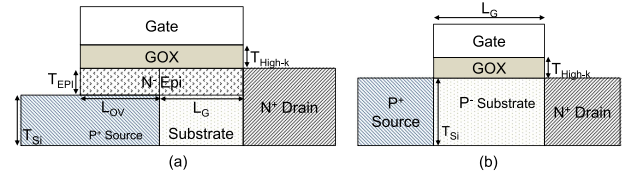

Fig. 13. Prior art TFET devices considered for comparison with the proposed device in this paper. (a) Planar area-scaled TFET. (b) Point TFET (gated p-i-n) device.
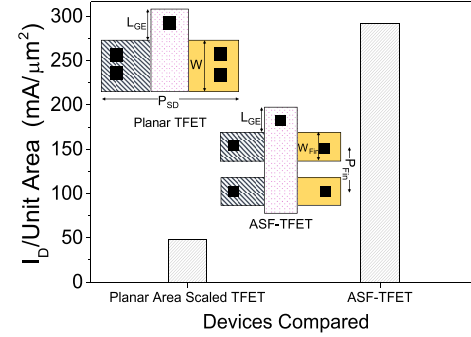

Fig. 14. Drain current density per unit area of the proposed ASF-TFET and the planar area-scaled devices. Inset: their respective layout/footprint views.

TABLE II
DEVICE DESIGN PARAMETERS USED FOR TCAD SIMULATION AND COMPARISON OF THE PROPOSED ASF-TFET, PLANAR AREA-SCALED TFET, AND POINT TFET

Parameter	Unit	Point TFET	Planar Area Scaled TFET	Proposed ASF-TFET
EOT	nm	0.4	0.4	0.4
$\mathbf{L}_G$	nm	20	20	20
$\mathbf{L}_{OV}$	nm	-	40	40
$\mathbf{N}_{Source}$	cm^{-3}	5x10^{20}	5x10^{20}	5x10^{20}
$\mathbf{N}_{Drain}$	cm^{-3}	1x10^{20}	1x10^{20}	1x10^{20}
$\mathbf{N}_{EPI}$	cm^{-3}	-	3x10^{19}	3x10^{19}
$\mathbf{T}_{Epi}$	nm	-	2	2
$\mathbf{N}_{Substrate}$	cm^{-3}	1x10^{16}	1x10^{16}	1x10^{16}
$\mathbf{T}_{Si}$	nm	5	7	-
$\mathbf{W}_{FIN}$	nm	-	-	10
$\mathbf{H}_{FIN}$	nm	-	-	40
$\mathbf{r}_{Cur}$	nm	-	-	2

device and its planar counterpart. Clearly, the proposed ASF-TFET shows a 6× improvement over the planar device, which shows a significant area scalability of the proposed device. Fig. 14 (inset) shows the respective device layouts used for this comparison.

Furthermore, the input (I_D versus V_G) and output (I_D versus V_D) characteristics extracted from 3-D TCAD simulations, as presented in Figs. 15 and 17, respectively, clearly show that the proposed ASF-TFET device outperforms its planar counterpart, i.e., the earlier proposed line TFET devices or planar area-scaled TFET device [10]–[18]. For a fair comparison, the same device design, as discussed and optimized in Section III, is used for both planar area-scaled TFET and proposed ASF-TFET. The device design details are further disclosed in Table II.
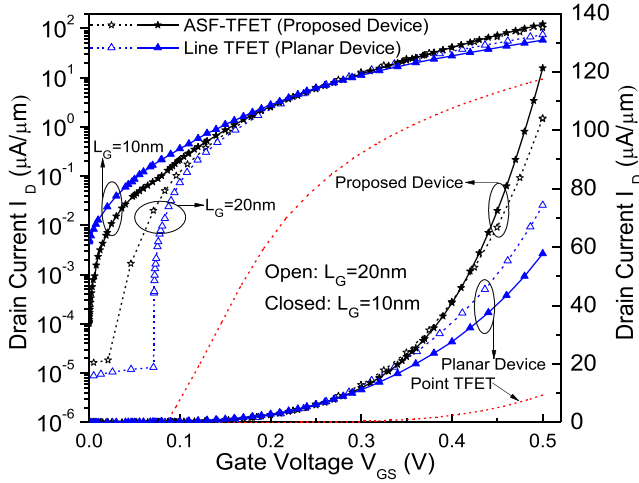
Fig. 15. Input characteristics, on log (left) and linear (right) scales, of the proposed ASF-TFET, planar area-scaled TFET, and point TFET for $L_G = 10$ nm and $L_G = 20$ nm.
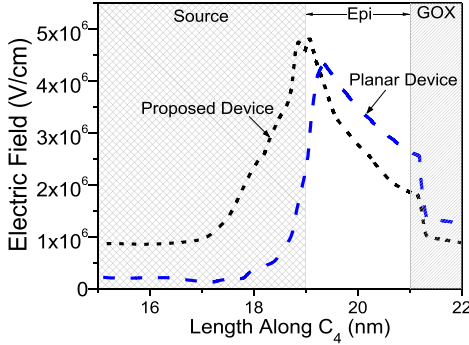

Fig. 16. Electric field profile along C_4 to compare maximum electric field at the source—overlap region interface of the proposed and planar devices.
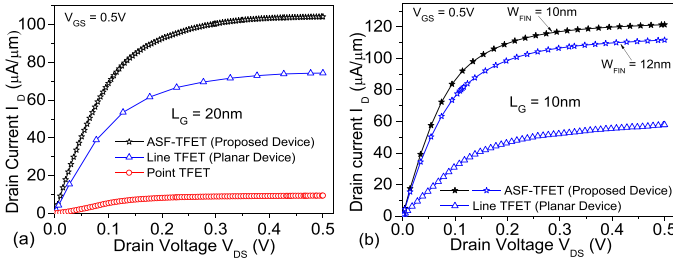

Fig. 17. Output characteristics of the proposed ASF-TFET, planar area-scaled TFET, and point TFET for (a) $L_G = 20$ nm and (b) $L_G = 10$ nm.

In order to justify the scalability and the advantages of the proposed device, the comparisons are made for 20 nm as well as 10 nm-channel length devices. Moreover, different Fin width devices were also used for the comparison. In all the cases, an ON-current improvement from 40% ($L_G = 20$ nm) to 100% ($L_G = 10$ nm) per unit electrical width can be seen, when compared with the planar area-scaled TFET device (Fig. 15). The reported improvement is due to increased gate electric field in the overlap region, as shown in Fig. 16. The increased gate field in the overlap region increases the tunneling probability and it is because of the 3-D nature of the gate, which enhances the electrostatic control of gate over the channel and overlap regions.

It is worth highlighting that the planar device unexpectedly shows an ON-current reduction when channel length was
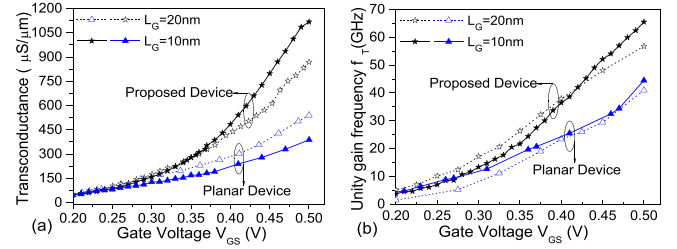

Fig. 18. (a) Transconductance and (b) unity gain frequency of the proposed ASF-TFET and planar area-scaled TFET devices. The proposed device clearly shows its applicability for high gain–high frequency applications for advance SoCs.

scaled from 20 to 10 nm. This is attributed to an effective gate electric field lowering, in the overlap region, due to an increased drain field. However, on the other hand, drain field in the proposed device does not significantly influence the gate electric field in the overlap region due to 3-D gate and fully depleted channel. This leads to an ON-current improvement by 100% when scaled down to 10 nm channel length. For channel length scaling, the key challenge is the OFF-state source-to-drain tunneling, which increases exponentially when channel length is scaled. To mitigate the OFF-state source-to-drain tunneling, an excellent electrostatic control of gate over the channel is required. Fig. 15 further shows a $15\times$ reduction in the source-to-drain leakage current for the 10-nm channel length device, which is attributed to an improved electrostatic integrity due to 3-D nature of gate and fully depleted Fin. This allows scalability below 10 nm channel lengths by keeping the leakage current unchanged. These observations prove that the planar device cannot be scaled below $L_G = 20$ nm, whereas the proposed device has a potential to be scaled below 10 nm gate lengths.

Fig. 17 compares the output characteristics of the proposed ASF-TFET and its planar counterpart for $L_G = 20$ nm and $L_G = 10$ nm. Lower ON-resistance, improved saturation characteristics, higher ON-current, and 30% higher output resistance ($1/g_{ds}$) clearly prove the advantage of the proposed device over its planar counterpart.

Finally, analog and RF performances of the proposed device are discussed. Fig. 18(a) and (b) compares the transconductance and unity gain frequency of both the proposed and planar devices, respectively. The proposed device results $3\times$ higher transconductance and 55% higher unity gain frequency when compared with the planar area-scaled TFET device for $L_G = 10$ nm. Improved unity gain frequency is because of increased transconductance, which is attributed to enhanced electric field and better gate control of the proposed device over the overlap region. Higher transconductance (g_m) and output resistance ($1/g_{ds}$) enable the proposed device for high gain amplifier design when compared with the planar area-scaled TFET devices. The increased unity gain frequency further enables the proposed device for high-gain – high-frequency applications.

V. CONCLUSION

The proposed area-scaled Fin-TFET device has shown great potential for scalability below 10 nm gate lengths. The proposed device offers 40% to 100% ON-current improvement

per electrical width, depending on the channel length and other device design parameters, when compared with its planar counterpart. The same per unit area or device footprint shows a 6× improvement due to the 3-D nature of the device. The 15× reduction in the source-to-drain leakage at $L_G = 10$ nm has been reported for the proposed device, which allows scalability below 10 nm gate lengths while keeping the leakage current unchanged. The proposed ASF-TFET device offers an average (over four decades of drain current) and minimum SSs of 40 and 11 mV/decade, respectively, which promises low power operation. A gain of 30% in output resistance, 3× improvement in transconductance, and 55% higher unity gain frequency of the proposed device, when compared with its planar counterpart, clearly demonstrate its applicability for analog and RF circuits even in the scaled technologies. These improvements show that the proposed device is suitable for future ultradense and low-power system-on-chip (SoC) applications.

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