Part II: A Fully Integrated RF PA in 28-nm CMOS With Device Design for Optimized Performance and ESD Robustness

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***Abstract*— In this paper, we report drain-extended MOS device design guidelines for the RF power amplifier (RF PA) applications. A complete RF PA circuit in a 28-nm CMOS technology node with the matching and biasing network is used as a test vehicle to validate the RF performance improvement by a systematic device design. A complete RF PA with 0.16-W/mm power density is reported experimentally. By simultaneous improvement of device-circuit performance, 45% improvement in the circuit RF power gain, 25% improvement in the power-added efficiency at 1-GHz frequency, and 5× improvement in the electrostatic discharge robustness are reported experimentally.**

***Index Terms*— CMOS, device-circuit codesign, drain-extended MOS (DeMOS), electrostatic discharge (ESD), power amplifier (PA), RF, shallow-trench-isolation (STI), system-on-chip (SoC).**

I. Introduction

TREMENDOUS growth in wireless systems operating at radio-frequencies requires a system-on-chip (SoC) solution for power amplifier (PA) circuits [1]. Drain-extended MOS (DeMOS) devices are explored by various researchers as a suitable candidate for the RF PA application due to its cost advantage and integration compatibility with a standard foundry process [2]–[5]. In [2], the RF power capability of 0.092 W/mm at 0.9 GHz is reported with 53% power-added efficiency (PAE) for DeMOS device using probe-station-based measurements. Chang *et al.* [3] also demonstrated recently that the DeMOS can be used to provide high output power at radio-frequencies. However, the RF PA design by DeMOS is still challenging, because the transistor structure suffers from limited mobility, comparatively lower cutoff frequency (f_t), and large terminal capacitances. Since achieving the system-level specifications using a standard DeMOS device is very challenging, the option to improve the device design itself also needs to be considered. Until now, studies on the design of the device and its relation to the complete system-level performance improvement have been fairly limited. Moreover, most of the earlier work is reported using the probe-station-based measurements on the device, which does not incorporate significant losses occurring in microstrips/passive components at the radio-frequencies.

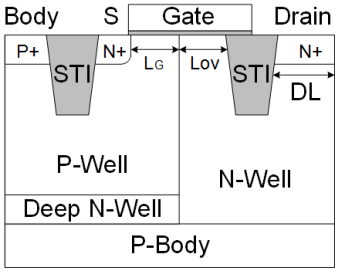

Fig. 1. STI-based DeNMOS device realized using 28-nm standard CMOS foundry process.

In Part I of this paper, we investigated the improvement in the device intrinsic performance by device-circuit codesign using TCAD-based simulations. In [6], we reported an RF PA circuit fabricated using the DeNMOS device (Fig. 1) in standard CMOS process and experimentally shown the circuit-level improvements by device design, for the first time. In this paper, we include design of a PA in 28-nm CMOS technology using DeMOS transistor design and trend of the circuit behavior with respect to the device design parameters, circuit fabrication details, time, and frequency domain measurement results. An enhanced analysis of the high-frequency linearity of RF PA is presented as a function of circuit bias conditions. It is experimentally shown that an RF PA circuit with better linearity can be achieved compared with [6], by optimally choosing the bias voltages.

This paper is organized as follows. Section II discusses the process of realizing complete RF PA circuit on board using fabricated devices. Section III discusses various small- and large-signal measurements performed on complete PA. Section IV presents the improvement in various circuit

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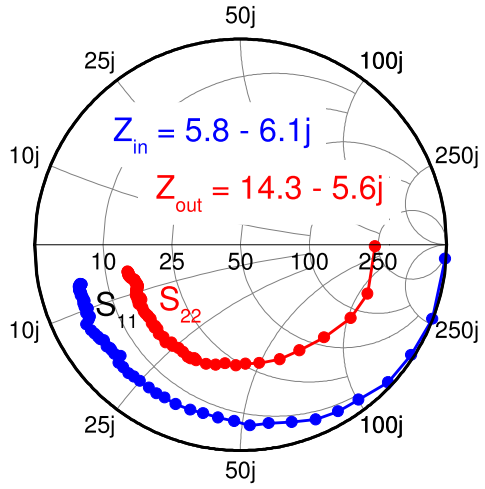

Fig. 2. Small signal S_{11} and S_{22} of the 1.6-mm device measured on wafer using RF probe-station. Input and output impedance are shown for a frequency of 1 GHz.

figures-of-merit (FoMs) by device design. Impact on linearity of the complete PA is discussed in Section V. Section VI discusses about various electrostatic discharge (ESD) and thermal reliability issues. Section VII summarizes the important results and findings of this paper.

II. RF PA Circuit Realization

To investigate the impact of device design on circuit-level performance, a PA circuit is prepared as a test vehicle. The total fabricated device gate width was 1.6 mm. The small-signal RF measurements were performed on the device using RF probe-station in order to obtain input and output impedance for matching network design. Measurements were performed using Agilent's PNA-X N5244A vector network analyzer (VNA). Fig. 2 shows S_{11} and S_{22} of the device for a frequency range of 1 MHz–1 GHz. The measured input and output impedance of the device is $Z_{\mathrm{IN}} = 5.8 - 6.1j$ and $Z_{\mathrm{OUT}} = 14.3 - 5.6j$, respectively, at 1 GHz of frequency of operation.

In order to prepare the complete PA circuit, a printed circuit board (PCB) was manufactured on glass substrate similar to [7] and [8]. The laminate had a dissipation factor (Tan δ) of 0.0004 which corresponds to a very low loss occurring in the PCB microstrips at high frequencies. PCB thickness was 0.8 mm, and the copper cladding used was 70 μm. A rise in junction temperature adversely impacts the device performance, and hence carrying away the heat in integrated PA circuit is very important. So, die was pasted on the patterned PCB using thermally conductive epoxy to carry away the heat generated by the device. Electrical connections from die to PCB were made using 25-μm gold wire, as shown in Fig. 3(a). The PCB tracks were electroplated with gold to achieve good adhesion of gold bond wire with the microstrip surface. Complete circuit schematic of the fabricated PA is shown in Fig. 4 along with the off-chip matching and biasing network. A ladder of decoupling capacitors (C1–C5) was used at both input and output dc supply to suppress the high-frequency noise generated due to large signal and harmonics generated by the device. An RC network is used at the gate

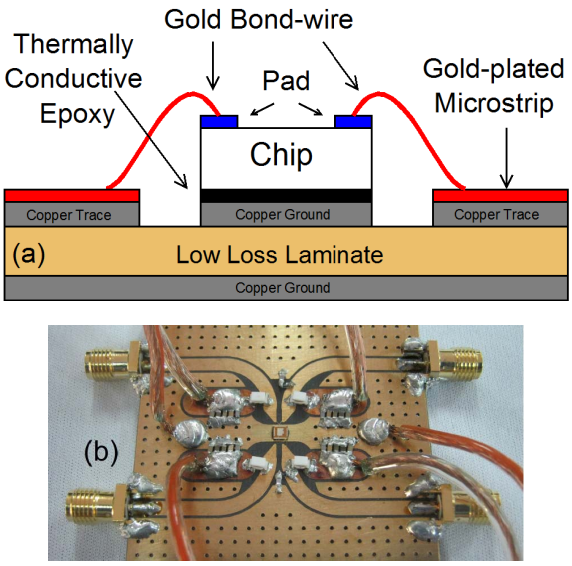

Fig. 3. (a) Chip placement on the PCB using thermally conductive epoxy. (b) Photograph of the fabricated PA on a low loss laminate.

terminal to stabilize the circuit. Input and output matching is achieved off-chip for the ease of optimization. Photograph of the fabricated PA structure is shown in Fig. 3(b).

III. Experiments and Results

The small-signal measurements were performed on this fabricated PCB using Agilent's E5071C VNA. Fig. 5 shows the measured S_{11} of the device, which represents the matching of the device with the signal source with respect to the frequency. Matching network was designed in order to achieve S_{11} below -10 dB to have good matching condition at 1-GHz frequency of operation. This also shows the small-signal gain (S_{21}) with respect to the frequency. Since the circuit uses RF choke (RFC) inductors, the gain drops at low frequencies due to low impedance path provided by RFC. The gain increases with frequency and again drops due to the limited -3-dB frequency of the device. The measured small-signal gain at 1-GHz frequency is 10.8 dB.

Large signal at 1 GHz is applied at the input port of PA using signal generator and the output power was measured using spectrum analyzer. Circuit was biased at a gate voltage of VGS1 for a Class-AB mode of operation. Drain supply voltage was kept at $\mathrm{VDS_{MAX}}$. Results are shown in Fig. 6. Output power of the PA increases linearly, and the RF gain remains constant with the input power for low signal levels. However, at high power levels, output power saturates because the device enters into saturation. When the circuit RF gain degrades by 1 dB compared with its small-signal value, the point is called 1-dB compression point ($P_{\mathrm{1\text{-}dB}}$). Circuit achieves an output power of 24 dBm at $P_{\mathrm{1\text{-}dB}}$. Measured drain-efficiency (DE) and PAE on the board are 46% and 40.2%, respectively, as shown in Fig. 6.

Device terminal voltages were measured using oscilloscope when the circuit was operated at its peak output power ($P_{\mathrm{1\text{-}dB}}$). Fig. 7 shows the voltage at device gate terminal which is less than the gate breakdown voltage. Though circuit was biased

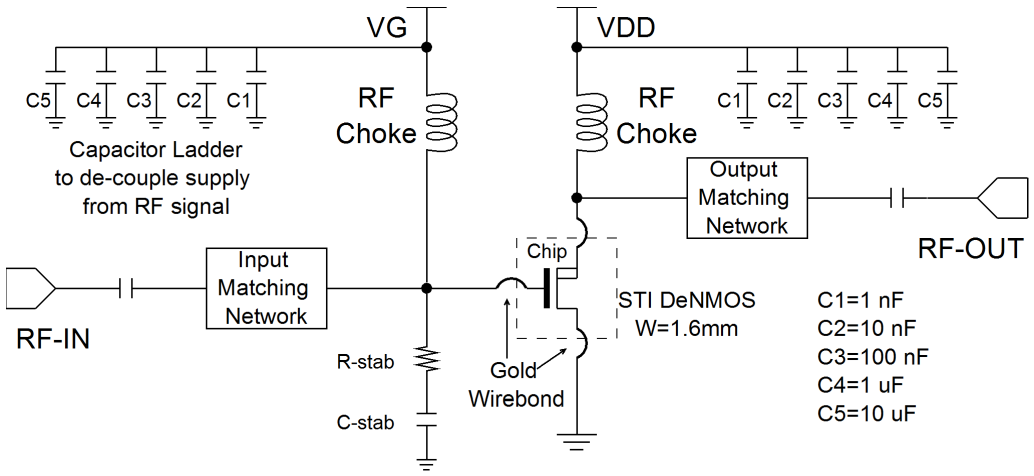

Fig. 4. Schematic of the fabricated PA circuit. Off-chip matching and biasing networks are shown along with the capacitor ladder at the dc power supplies to reduce the noise generated by the circuit. An RF network at the gate is used to stabilize the circuit.

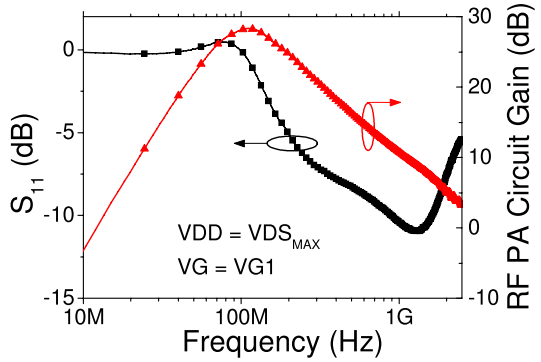

Fig. 5. Small-signal matching (S_{11}) and small-signal gain (S_{21}) of RF PA circuit measured on board for a range of frequency.

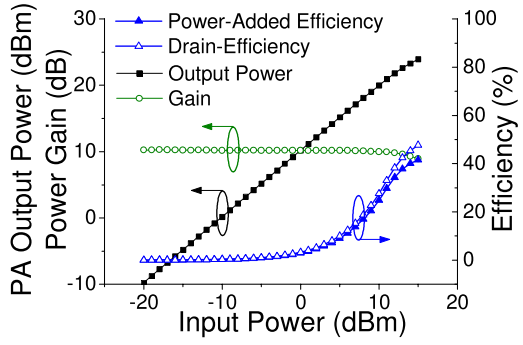

Fig. 6. Large-signal performance of the implemented DeNMOS-based RF PA, measured experimentally using Class-AB mode of operation at 1-GHz operating frequency.

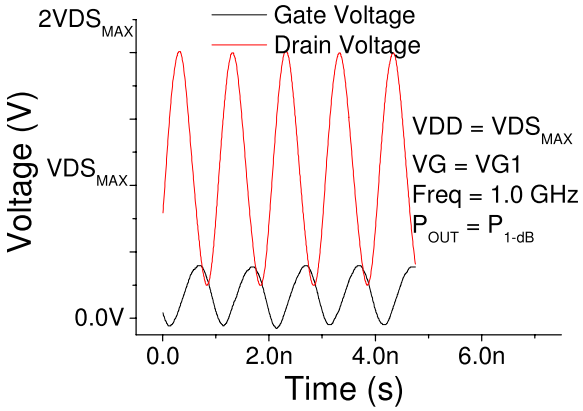

Fig. 7. Voltages at the gate and the drain terminal of the device measured using oscilloscope when circuit is operating at its peak output power of 24 dBm at 1 GHz.

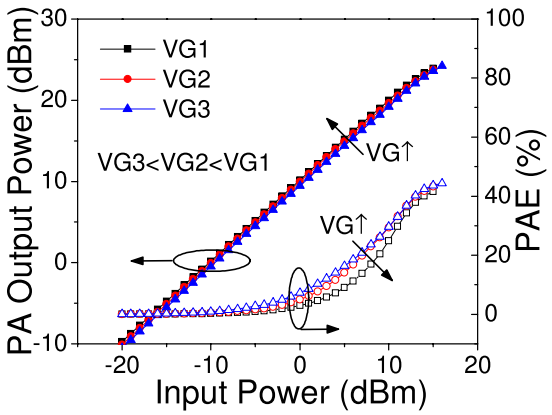

Fig. 8. Impact of the device gate bias voltage on the output power and efficiency of the circuit.

at VDS_{MAX} at the drain, the drain terminal voltage reaches up to $2VDS_{MAX}$ due to the RFC action. It is important to have drain breakdown voltage of the device higher than $2VDS_{MAX}$ to support this swing.

Class-AB mode of operation was chosen for the circuit operation, which gives better tradeoff between efficiency and linearity and widely used in wireless industry [9]. Gate bias was further reduced by 100 mV (VG2) and 50 mV (VG3) to drive the circuit into deep Class-AB mode, and the results are analyzed in Fig. 8. Efficiency of the circuit improves for complete range of input power. However, the improvement is more at intermediate power level. At high power levels, output power (and hence efficiency) is governed by VDD, which is kept constant in the experiment. However, RF gain of

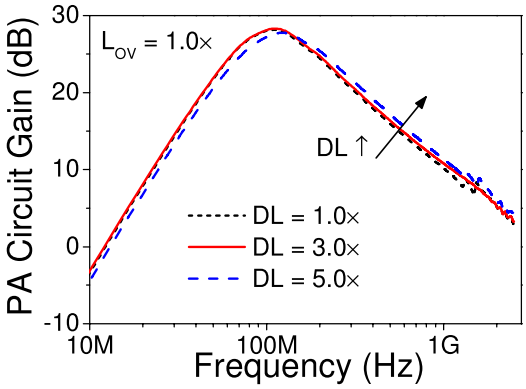

Fig. 9. Measured small-signal RF gain of the PA circuit as a function of frequency for various DL values.

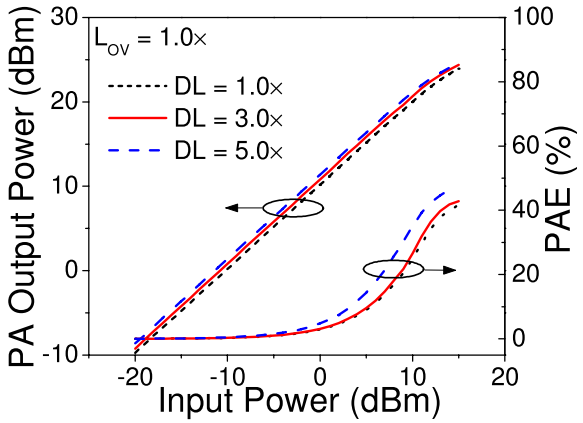

Fig. 10. Output power of the circuit measured at 1-GHz frequency. PAE of the circuit is also shown as a function of applied input power.

the circuit decreases marginally (0.2 dB for VG2 and 0.5 dB for VG3) when circuit is driven to deep Class-AB mode.

IV. Impact of the Device Design on the PA Performance

Part I of this paper discussed the device design and optimization by the TCAD simulations. In this part, these novel devices with DL = 1×, 3×, and 5× were fabricated, and RF performance was measured at board level in a similar way as explained earlier. Input and output bias supply voltages were kept constant at VG1 and VDS_{MAX}, respectively. Performance of RF PA circuit with DL = 1× reported in Section III is taken as a reference for benchmarking.

A. Impact of DL on RF PA Performance

Fig. 9 shows the amplifier gain as a function of frequency for various DL values of the device. This was measured at a small input power of −20 dBm, and the frequency was swept from 1 MHz to 2.5 GHz. As the drain diffusion length (DL) is optimized from 1× to 5×, there is monotonous improvement in the gain of the circuit. The circuit shows an improvement of ∼45% in gain at 1 GHz. This improvement in the gain is suggested by mixed-mode TCAD simulations (Part I) and can be correlated with the improvement of gm by optimizing DL from 1× to 5×. Power-added efficiency (PAE) is shown in Fig. 10 as a function of applied input power at 1 GHz of frequency of operation. Input power was swept from a small value of −20 dBm to a large value of 15 dBm. PAE also shows a continuous increase by the optimization of DL from 1× to 5×. There is an improvement in PAE from 40% to 50% at $P_{1\text{-dB}}$. It is worth mentioning here that the gain and the efficiency have a tradeoff in PA circuit design and product of these quantities remains constant. However, optimization of the active device itself can cause an increase in both and improve their product.

Output power delivered by the circuit to 50-Ω load at 1-GHz frequency is also shown in Fig. 10 as a function of input power level. The output bias voltage is constant at VDS_{MAX}, which limits the swing at drain terminal to $2VDS_{MAX}$. All the devices show power characteristics with monotonous improvement in power gain corresponding to their small-signal values.

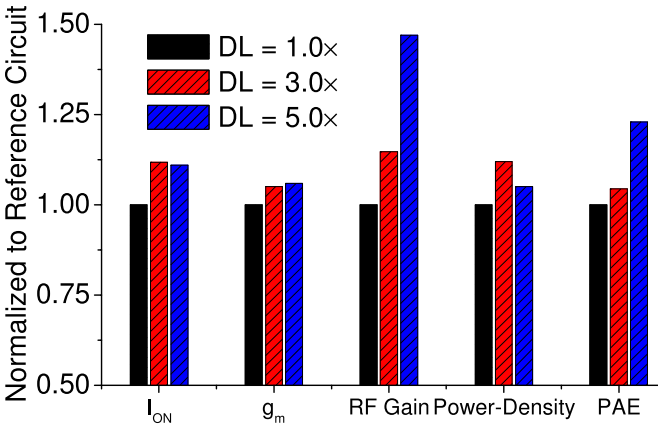

Fig. 11. Improvement in the RF PA circuit FoM by device design.

However, as the circuit approaches $P_{1\text{-dB}}$, the allowable maximum swing is limited by the constant output supply voltage. Hence, all the devices have almost the same peak output power of 24 dBm delivered to 50-Ω load.

Fig. 11 shows the relative improvement in various device and circuit-level FoMs by this drain engineering. As shown, significant improvements in various system-level FoMs can be achieved by device design and optimization.

B. Impact of L_{OV} on RF PA Performance

To further investigate the possibility of circuit improvement by device design, L_{OV} was changed from 0.6× to 1.4× and the similar set of measurements were carried out on a fabricated circuit. Fig. 12 shows the small-signal gain of the circuit for optimization of L_{OV}. The change in L_{OV} impacts the device dc characteristics (e.g., gm) and ac characteristics (e.g., gate capacitance) simultaneously as discussed in Part I. By reducing L_{OV}, there is degradation in the gm but improvement in the gate capacitance. Combined effect of both of these factors is nonlinear and seen at radio-frequencies. The gain of the circuit improves as L_{OV} is reduced from 1.4× to 0.6× as shown. RF gain of the circuit at 1 GHz is 9.9 dB at $L_{OV} = 1.4\times$, which increases to 11.5 dB for $L_{OV} = 0.6\times$.

PAE of the circuit also improves from 42% to 48% at $P_{1\text{-dB}}$, as shown in Fig. 13. Fig. 13 shows the output power with respect to swept input power. The output power at $P_{1\text{-dB}}$

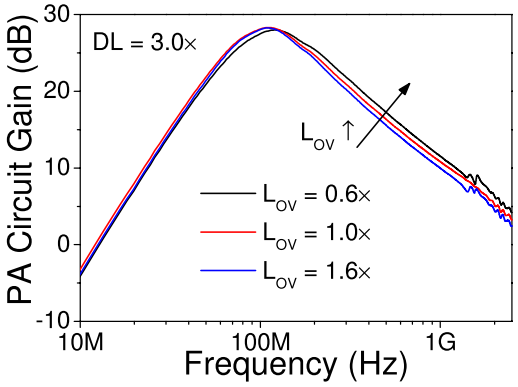

Fig. 12. Measured small-signal gain of the circuit as a function of frequency for L_{OV} optimization.

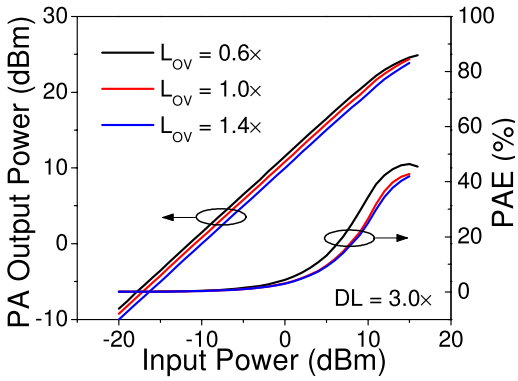

Fig. 13. Measured output power and PAE of the PA circuit at 1-GHz frequency as a function of applied input power.

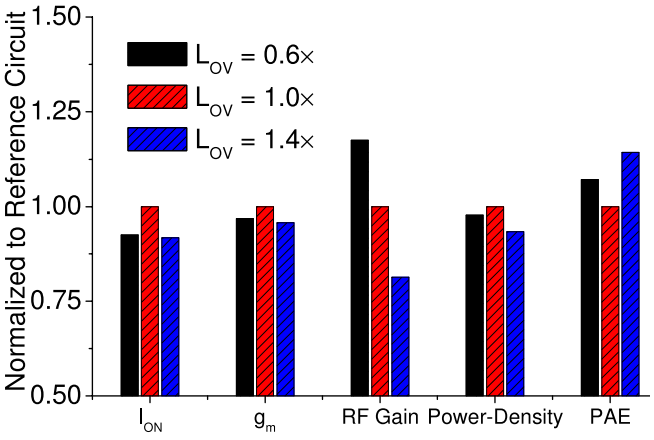

Fig. 14. Improvement in the RF PA circuit FoM by L_{OV} design.

is ~24 dBm due to the swing limited by VDD as explained earlier. Fig. 14 shows the relative improvement in various device and circuit-level FoMs by L_{OV} optimization.

V. Impact on Linearity by Device Design

Linearity of the PA circuit is also an important criterion to determine its usability in the RF applications. Linearity of the PA is generally characterized by two-tone test where two frequencies (f_1 and f_2) centered at 1 GHz with a small spacing of 1 MHz are applied at the PA input. A linear circuit should produce only the fundamental frequency at the output without any other harmonics of the frequency. However, practically,

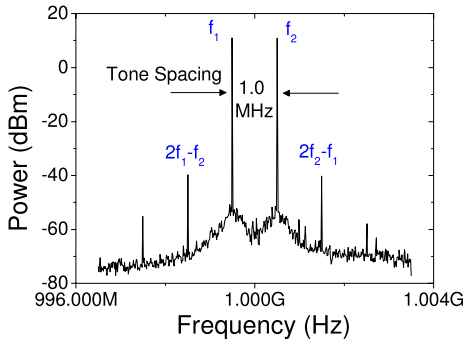

Fig. 15. Power spectrum measured at the output of the circuit at input power of 0 dBm.

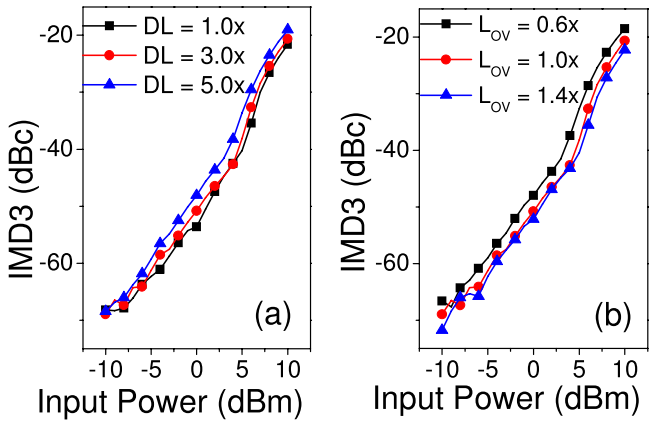

Fig. 16. Measured IMD3 with respect to input power for (a) various DL values and (b) various L_{OV} values.

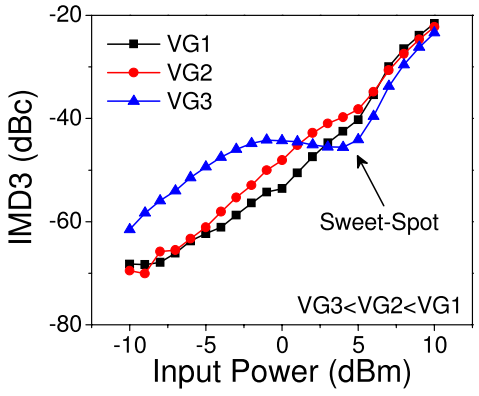

Fig. 17. Measured IMD3 at the output power spectrum of the circuit for Class-AB and deep Class-AB mode of operation.

all the active devices have some nonlinearity and produce undesired harmonics at the output. Measured output spectrum of the circuit contains third harmonics ($2f_1-f_2$ and $2f_2-f_1$) along with the fundamental frequencies, as shown in Fig. 15. Magnitude of these third harmonics measured for various DL and L_{OV} values are plotted in Fig. 16, which shows very low values of third-order intermodulation distortion (IMD3) generated by the device.

Furthermore, the impact of gate bias voltage on the circuit linearity is analyzed in Fig. 17. Gate voltage is decreased from VG1 to VG3, and IMD3 is measured from the output

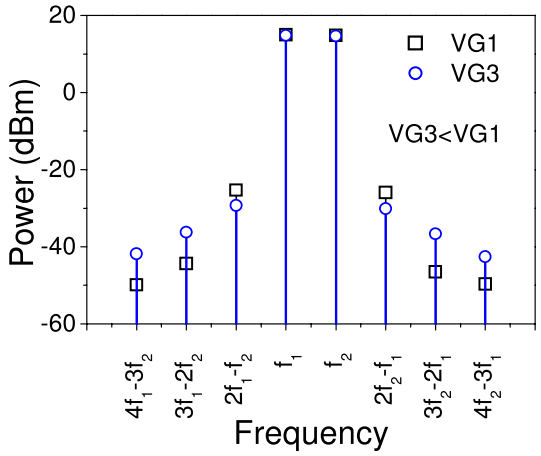

Fig. 18. Simplified output power spectrum at 5-dBm input power that corresponds to sweet-spot creation in IMD3.

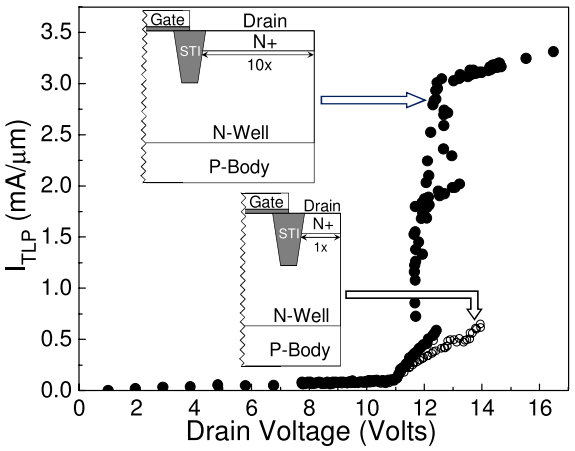

Fig. 19. TLP characteristics of conventional and modified drain engineered device. The figure clearly depicts significant improvement in the device's ESD robustness by drain engineering.

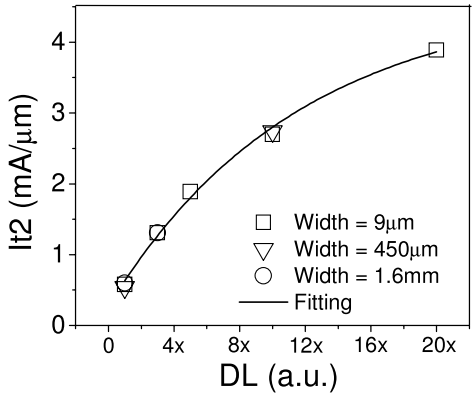

Fig. 20. Consistent improvement in the failure current (It2) by increasing drain DL.

power spectrum. At higher gate bias when the circuit is in Class-AB mode, IMD3 monotonically increases with a slope of 3 from small-signal conditions (lower input power levels) to large-signal conditions (higher input power levels). However, when the gate bias is very close to the device threshold voltage (VG = VG3), IMD3 contains a minima for a range of input power levels. This behavior of IMD3 and creation of sweet spot has already been reported in [9]. However, in order to investigate the impact of this sweet spot on the RF performance, the simplified measured power spectrum is plotted in Fig. 18 at 5-dBm input power for VG1 (Class-AB mode), and VG3 (deep Class-AB mode). Due to this sweet-spot formation in case of VG3, third-harmonic contents ($2f_1-f_2$ and $2f_2-f_1$) produced by the device reduces. At the same time, the power content of fifth harmonics ($3f_1-2f_2$ and $3f_2-2f_1$) and seventh harmonics ($4f_1-3f_2$ and $4f_2-3f_1$) increases. This means that the generated noise in the frequencies adjacent to the channel is comparatively less but higher in the entire RF spectrum. This is in agreement to the fact that linearity of the circuit degrades with reduction in the gate bias voltage for low input power levels <0 dBm. As input power increases, beyond 0 dBm, there is a crossover point from where the device with lower gate bias voltage shows the reduced intermodulation nonlinearity.

VI. ESD and Thermal Reliability

PA devices are directly connected to the PCB antenna traces. Hence, any ESD event causes significant voltage overstress across the device terminals. Therefore, robustness toward ESD is an important feature of a PA driver stage. Fig. 19 shows the transmission line pulsing (TLP) measurements performed on the standard device and modified device [10]. It is shown that the standard device fails early at 0.6 mA/μm of failure drain current. However, the modified device with longer DL region shows significantly improved failure current of 3.3 mA/μm. This shows that the ESD robustness of the device improves by 5× compared with standard device. Since in case of RF PA the devices are of the order of millimeter gate width with few hundred fingers in parallel, measurements were performed on the multifinger structures. TLP characteristic shows a multifinger triggering for modified devices at TLP current of 2 mA/μm (Fig. 19). This proves that good device robustness can be achieved in case of multiple finger structure.

Fig. 20 shows the TLP results on devices with various DL. A monotonous improvement in the ESD robustness of the device is found for an increase in DL. The 3-D TCAD simulations were performed in order to investigate the physics behind the improvement in robustness by DL. Fig. 21(a) shows the current density contour in the device when subjected to TLP conditions. It depicts a localized peak of electric current (filament formation) confined in a narrow region of total drain width. This causes a rise in the lattice temperature, which in turn causes an early damage to the device. However, when similar simulations were performed on the modified device with larger DL, the current density is uniformly distributed over the entire width of the device [Fig. 21(b)]. This uniform spreading of current filament prevents the rise of lattice temperature beyond the critical temperature, which significantly improves the device robustness [10].

One of the bottlenecks in integrating high-power devices on silicon is the rise in temperature of the die due to power dissipation inside the device. Thermal measurements were carried out using thermocouple probe to check the rise in die temperature when the circuit was operated at its peak

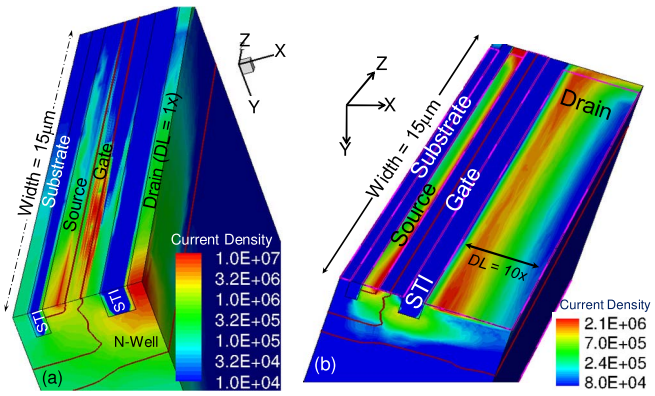

Fig. 21. (a) 3-D TCAD pictures depicting current filamentation in the standard DeNMOS device at low currents ($I_{TLP} = 0.5$ mA/μm). (b) Device survives filamentation after drain engineering, even at very high currents ($I_{TLP} = 3.5$ mA/μm) [10].

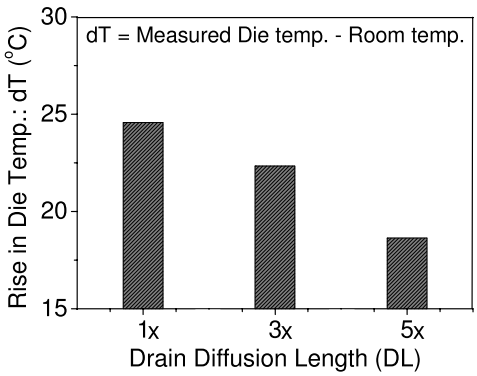

Fig. 22. Rise in the die temperature as a function of drain DL, measured at 24 dBm of RF power level.

output power (i.e., 24 dBm). Though all the devices produce the same output power, the efficiency of DL = 5× is more, which causes less dc power dissipation inside the device. In addition, the area for the current to flow is more extended in the case of higher DL. Both these factors combined causes a significant reduction in die temperature for optimized DL = 5× compared with DL = 1×. Fig. 22 shows a reduction of ∼8 °C in the die temperature for DL = 5× compared with DL = 1×. Due to the lower increase in die temperature, a watt level (30 dBm) integrated RF PA for the SoC applications seems to be therefore feasible.

VII. Conclusion

In this paper, we realized a complete RF PA using shallow-trench-isolation (STI)-based DeNMOS device in the state-of-the-art 28-nm CMOS technology node. A peak output power of 24 dBm is achieved at $P_{1\text{-dB}}$ with a power density of 0.16-W/mm and an efficiency of 50% for a Class-AB mode of operation. Furthermore, we experimentally showed an optimization strategy of DeMOS device to obtain better RF performance of the circuit. It is shown that ∼10% improvement in dc and ∼45% improvement in RF FoMs can be achieved by proper optimization of device intrinsic parameters.

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