Part I: High-Voltage MOS Device Design for Improved Static and RF Performance

Ankur Gupta, *Student Member, IEEE*, Mayank Shrivastava, *Member, IEEE*, Maryam Shojaei Baghini, *Senior Member, IEEE*, Dinesh Kumar Sharma, *Senior Member, IEEE*, Harald Gossner, *Senior Member, IEEE*, and V. Ramgopal Rao, *Senior Member, IEEE*

***Abstract*— In this paper, for the first time, the key design parameters of a shallow trench isolation-based drain-extended MOS transistor are discussed for RF power applications in advanced CMOS technologies. The tradeoff between various dc and RF figures of merit (FoMs) is carefully studied using well-calibrated TCAD simulations. This detailed physical insight is used to optimize the dc and RF behavior, and our work also provides a design window for the improvement of dc as well as RF FoMs, without affecting the breakdown voltage. An improvement of 50% in R_{ON} and 45% in RF gain is achieved at 1 GHz. Large-signal time-domain analysis is done to explore the output power capability of the device.**

***Index Terms*— Advanced CMOS, drain-extended MOS (DeMOS), high-power RF, integrated RF power amplifier (PA), system-on-chip (SoC).**

I. Introduction

RECENT growth in the mobile communication market is one of the driving factors for system-on-chip (SoC) solutions on silicon [1]–[3]. These advanced SoCs require the integration of all the analog/RF and wireless communication functionalities along with digital processing on the same Si substrate. Accordingly, various subsystems, such as power management and RF power amplifier (PA), need to be fabricated using standard silicon process. However, presently, RF PA is realized using either GaN high-electron mobility transistors or SiC-based power MOSFETs due to their higher carrier mobility and breakdown voltage (V_{BD}) compared with silicon-based devices [4]. The integration of these GaN or SiC devices on the silicon substrate is not trivial [5]. Furthermore, difficulty in scaling of these compound semiconductor devices is also reported in [6]. Hence, for CMOS-based advanced SoCs, a Si-based RF PA is of interest.

Manuscript received April 27, 2015; accepted August 13, 2015. Date of publication September 9, 2015; date of current version September 18, 2015. The review of this paper was arranged by Editor H. Jaouen.

A. Gupta, M. S. Baghini, D. K. Sharma, and V. R. Rao are with the Center of Excellence in Nanoelectronics, Department of Electrical Engineering, IIT Bombay, Mumbai 400076, India (e-mail: agupta@ee.iitb.ac.in; mshojaei@ee.iitb.ac.in; dinesh@ee.iitb.ac.in; rrao@ee.iitb.ac.in).

M. Shrivastava is with the Advance Nanoelectronic Device and Circuit Research Laboratory, Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore 560012, India (e-mail: shrivastva.mayank@gmail.com).

H. Gossner is with the Intel Communication Device Group, Munich 80336, Germany (e-mail: harald.gossner@intel.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2015.2470117

A design of RF PA in advanced CMOS processes is difficult to achieve due to limited available power, significant tradeoff with the performance, very high sensitivity toward the electrostatic discharge (ESD), and the inherent nonlinearity of the advanced MOS devices [7]–[9]. V_{BD} of the devices in the advanced CMOS nodes is also very low, which limits the maximum output drain voltage swing and hence the output power capability of the device. Most of the modern SoCs have 5 V supply available for the interfacing circuits. However, to utilize this supply for the power amplification, V_{BD} (i.e., breakdown voltage) of the integrated device should be double of this voltage (9–12 V). The RF subsystems have significantly different signal and power level requirements as compared with the digital logic blocks, which make them even more complex to integrate on the same substrate with other modules. Furthermore, the PA circuits are generally directly connected to the off-chip antenna and relatively thin gate oxides of the devices make them very susceptible to the ESD damage.

Shallow trench isolations (STIs)-based drain-extended MOS (DeMOS) is a high-voltage device, of which the fabrication process is compatible with the CMOS processing steps. Our group has earlier reported a detailed analysis of this device and its comparison with other high-voltage MOS structures such as LDMOS devices [10], [11]. DeMOS transistor can sustain high terminal breakdown voltages due to the reduced surface field action, which makes it suitable for high-power applications [12]. The DeMOS transistor can be fabricated along with the conventional MOS devices with minor process cost penalty, and hence, it is already being used in various I/O circuits, such as high-voltage line drivers and level shifters [13]–[16]. Due to the simplicity and the process compatibility, the DeMOS is available as a standard foundry offering even in most advanced CMOS technology nodes. In [17], the output power capability of the DeMOS is explored using probe-station-based RF measurements. Similar types of measurements have been conducted to show the device suitability for RF PA applications in [18]. However, there are limited publications about the underlying physical behavior of the device and its correlation with the complete performance at system level.

In Part I of this paper, we start with the simulation of a foundry standard DeNMOS device and investigate its various dc, analog, and RF intrinsic performance along with the underlying physical phenomenon. Based on these investigations,

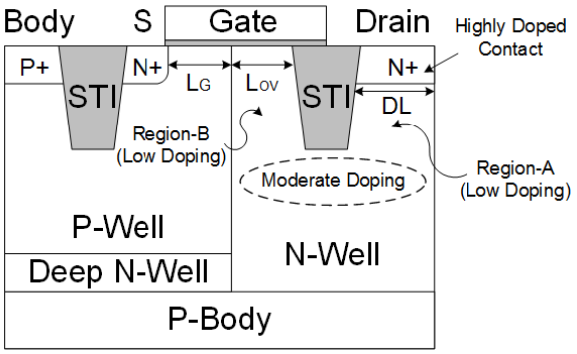

Fig. 1. Cross-sectional view of the STI-type DeNMOS device. The figure shows a single-finger structure; however, the device is realized in a two-finger structure on silicon with the sharing of n-well between two fingers.

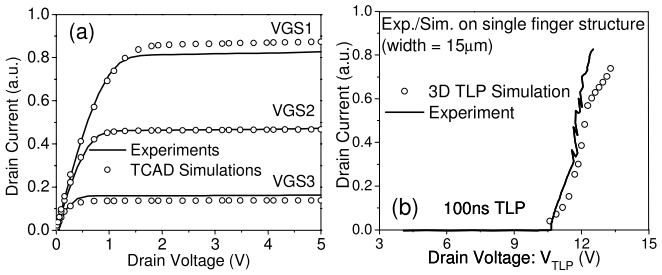

Fig. 2. Calibration of the models used in the TCAD simulations for the STI-type DeNMOS devices used in Part I of this paper. (a) Calibration of the mobility models including quantum corrections. (b) Calibration of avalanche generation and high field velocity saturation models for high voltage and high current operation.

we come up with a device design to achieve better system-level performance specifications. The device intrinsic performance is analyzed by extensive TCAD-based simulations and linked to its effects at the complete system-level improvement. A new device optimization strategy is also discussed in this paper. In Part II, for the first time, we report an integrated RF PA circuit using the DeMOS transistors fabricated in 28-nm CMOS technology. Measurement results of the complete PA circuit fabricated along with passive bias and matching networks will be provided.

This paper is organized as follows. Section II discusses the device realization and the simulation setup. Section III describes the static performance of the DeMOS for various layout parameters optimization. Section IV presents the small-signal analog performance of the device, whereas Section V discusses the large-signal RF output power and linearity of the devices when used for the RF PA applications. Finally, the conclusion is drawn in Section VI.

II. Device Under Test

We analyze STI-based DeMOS devices in this paper (Fig. 1) with thin gate dielectric and triple well CMOS technology. Minimum allowed spacing and dimensions as per the design rules were exploited while realizing the DeMOS devices to reduce the device's footprint as enabled by technology scaling. The device based on minimum allowed design rules is named as standard 1× device in this paper. Scaling factor is kept constant throughout this paper with respect to the standard

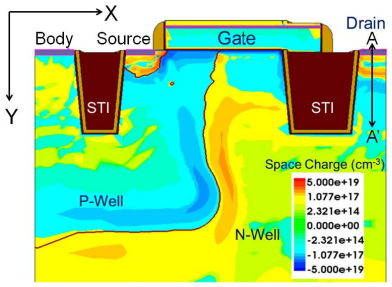

Fig. 3. Early space charge formation in the device when subjected to high current conditions (TCAD simulations).

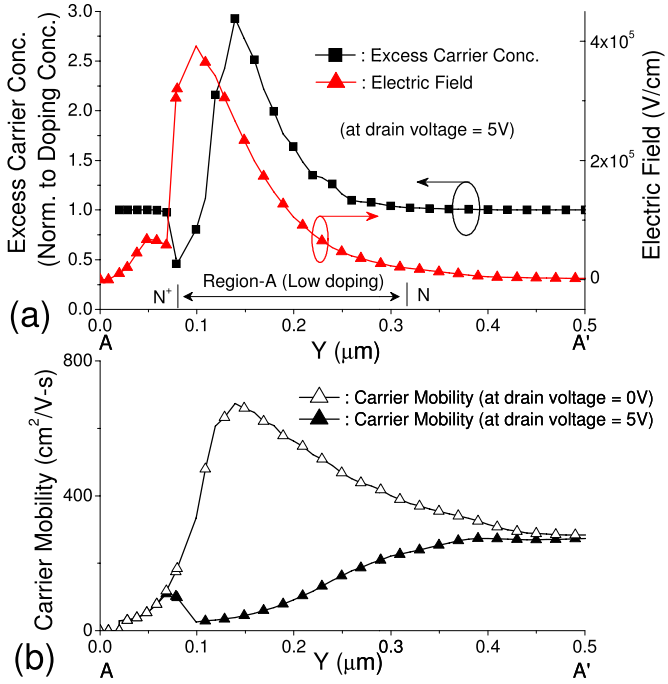

Fig. 4. (a) Mobile charge carrier density and electric field profile along A-A′ cut in the device. (b) Carrier mobility comparison for $V_{DS} = 0$ V and $V_{DS} = 5$ V.

DeMOS device. Furthermore, to develop detailed physical insight into the devices, a well-calibrated device TCAD deck was also developed. Both process and device models were calibrated against experimental data. For example, Monte-Carlo model for the ion implantation of deep wells was used and was calibrated using the secondary ion mass spectroscopy data. Doping-dependent and high field mobility model was calibrated to match the dc I–V characteristics [Fig. 2(a)]. Moreover, the avalanche generation model was calibrated to match the breakdown characteristics [Fig. 2(b)]. Further details on the TCAD calibration can be found in [19].

III. Static Performance of the Device

As shown in Fig. 1, regions under the drain junction and under the gate to n-well overlap (region A and region B) have relatively low-doping concentration compared with other parts of the drain region. This happens due to the retrograde-doping profile of the device. Retrograde-doping profile should be used to support high terminal breakdown voltages up

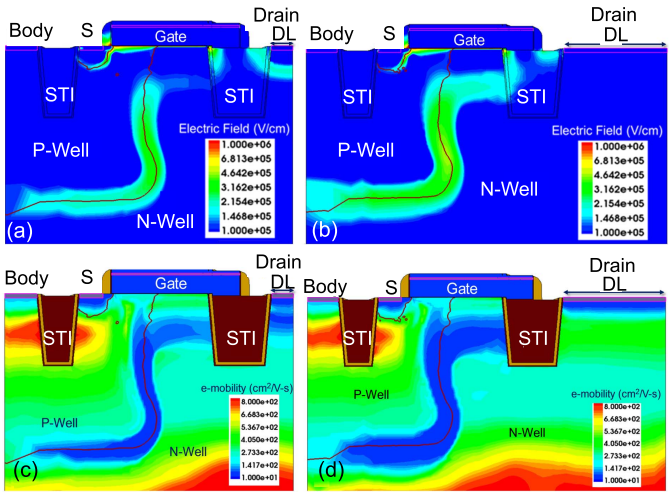

Fig. 5. (a) and (c) Electric field and carrier mobility contours, respectively, for standard foundry device with DL = 1×. (b) and (d) Electric field and carrier mobility contours, respectively, for improved device with DL = 5×.

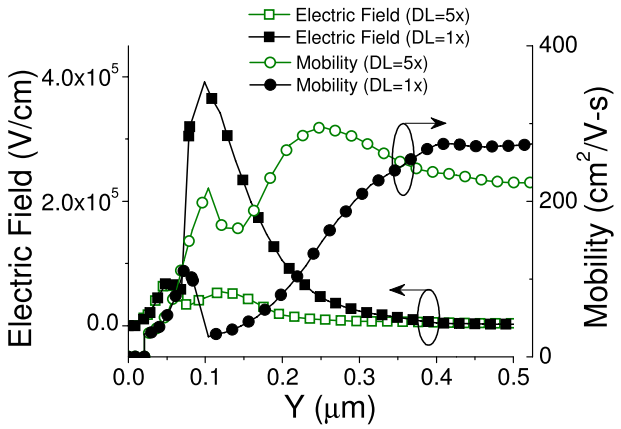

Fig. 6. Reduced electric field and increased mobility under drain n^+ (region A) by improved device design at high current conditions.

to 10 V. Drift region under STI has higher doping to lower the drift resistance of this region. Since region A is sandwiched between two highly doped junctions, this region forms local n^+-n^--n junctions where the mobile charges get accumulated or depleted depending on the applied bias voltages.

For high-power applications, it is required to bias the drain at high voltages to maintain high signal swings as well as high current levels. Fig. 3 shows the TCAD simulations performed on the device at high current conditions (V_{GS} = 2 V and V_{DS} = 5 V). As shown, there is an early formation of space charge within the device, which leads to quasi-saturation effects in the device characteristics and various device reliability issues [20]–[22]. In order to investigate the fundamental cause of this quasi-saturation effect and its relation to the device performance, we take a cut along the A-A′ and plot the characteristics along this cut in Fig. 4. Excess carrier concentration is shown in Fig. 4(a) for V_{DS} = 5 V, which is normalized to background doping concentration of the device. It is shown that a significant amount of mobile charge carriers accumulate in this region when the drain is biased at high voltage. This nonuniform distribution of charge carriers

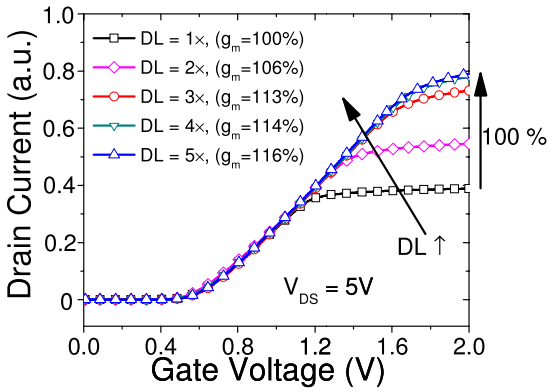

Fig. 7. Impact of DL on I_D–V_G characteristics of the DeNMOS device simulated at a fixed drain bias of 5 V. The figure shows a 100% improvement in device characteristic by DL optimization at saturation.

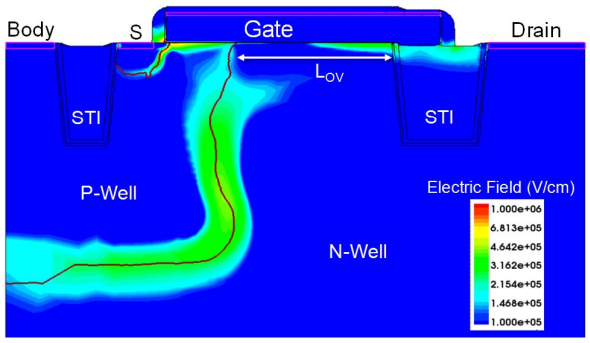

Fig. 8. Reduction in the nonuniform electric field under the gate to n-well overlap region by L_{OV} optimization.

gives rise to the localized peaking of electric field underneath the drain contact diffusion (i.e., drain n^+). As shown in Fig. 4(b), increased electric field results in the significant degradation of carrier mobility across this region compared with its low electric field value, which indeed is the root cause of high drift resistance and early quasi-saturation in this region.

To mitigate early space charge generation, the electron density in the drift region should be reduced. To reduce the electron density under the drain n^+, a drain diffusion length (DL) was increased. Fig. 5 shows the simulated electric field and carrier mobility contours for the standard device (DL = 1×) and improved device (DL = 5×). As shown, the nonuniform peaking of the electric field under the drain diffusion region [Fig. 5(a)] is suppressed by an increase in DL [Fig. 5(b)], which in turn improves the carrier mobility in this region [Fig. 5(d)] compared with standard device [Fig. 5(c)]. The extension of DL also reduces the overall drain contact resistance. Fig. 6 compares the electric field profile along the A-A′ in the standard device and the improved device at high current conditions (V_{GS} = 2 V and V_{DS} = 5 V). Fig. 6 clearly shows that the electric field significantly reduces in the lightly doped drift region, which causes a many fold improvement in the charge carrier mobility.

Fig. 7 shows the I_D–V_G characteristics of the device for DL optimization. It is shown that the saturation characteristic

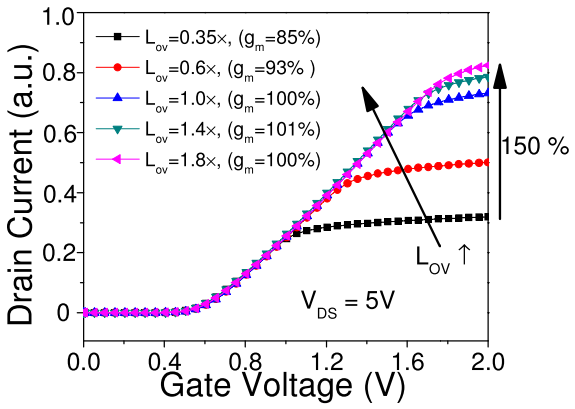

Fig. 9. Impact of L_{OV} on I_D–V_G characteristics of the DeNMOS device simulated at a fixed drain bias of 5 V. The figure shows a 150% improvement in device characteristic at saturation by L_{OV} optimization.

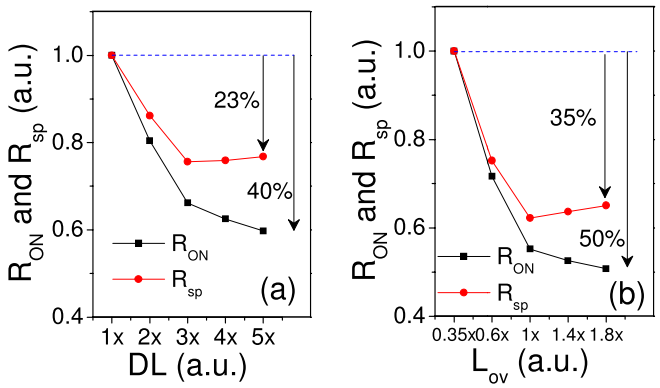

Fig. 10. Improvement in the device ON-resistance (R_{ON}) and specific-resistance (R_{sp}) for optimization of (a) DL and (b) L_{OV}.

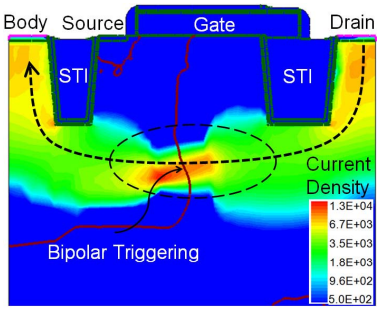

Fig. 11. Current density (cm^{-3}) extracted from the 2-D TCAD simulations. The figure shows the bipolar triggering well below the surface, which remains unaffected by the change in DL and L_{OV}.

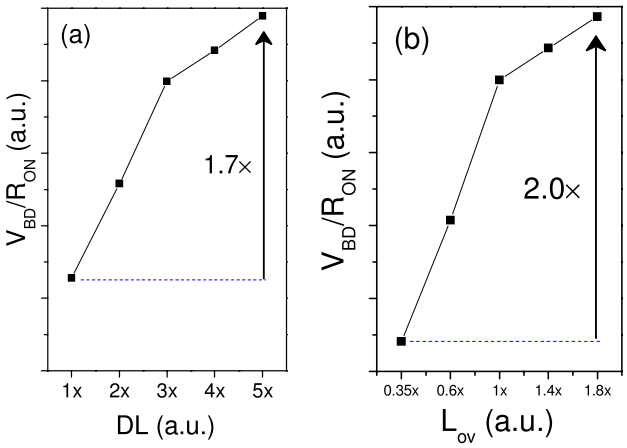

Fig. 12. V_{BD}/R_{ON} is an FoM for power applications. Improvement in FoM (a) when DL is optimized and (b) when L_{OV} is optimized.

improves monotonically as DL is optimized from 1× to 5×. Since the optimization of DL does not influence the device active channel region; there is no impact on the device characteristic for low and medium gate overdrive voltages. Fig. 7 also shows the peak transconductance (gm) of the device for multiple DL values. As DL is increased, peak gm improves because of the relaxation in the carrier crowding. Further increase in DL after 5× gives marginal improvements in the device characteristics.

We now focus on the second lowly doped drift region (region B) underneath the gate and n-well overlap (L_{OV}), as shown in Fig. 1. L_{OV} is very important and widely reported to improve the device characteristics without impacting V_T, subthreshold slope, or leakage of the device [23]. L_{OV} optimization significantly improves the flatness of I_D–V_D curve, which improves high power capability of the device [24]. Furthermore, L_{OV} optimization is also reported to reduce the hot-carrier-induced degradation, which is very beneficial for high-power applications [25]. Region B, shown in Fig. 1, is also sandwiched between two comparatively high-doped junctions and can cause quasi-saturation in the device. Charge carriers drift into this region from the channel and pulled away by the drain voltage. For narrow L_{OV}, there is a peak in the localized electric field similar to the earlier case of DL. As L_{OV} is increased (Fig. 8), there is a reduction in the nonuniform electric field under gate to n-well overlap compared with Fig. 5(b). Fig. 9 shows the I_D–V_G characteristics of the devices for multiple L_{OV} values. This is shown that the dc performance improves monotonically with the L_{OV} value. However, increase in L_{OV} also increases the total gate capacitance, which can adversely impact the device performance at high frequency. This effect will be discussed later in detail. Fig. 9 also shows the peak gm of the devices. As shown, narrow L_{OV} region severely impacts the device performance and provides a narrow operating region. Peak gm of the device improves with L_{OV} increase due to the improvement in current density profile up to a certain point. After that the increase in the drift region resistance due to longer length degrades the gm of the device.

R_{ON} of the device, measured at $V_{GS} = 2$ V and $V_{DS} = 0.1$ V, is shown in Fig. 10. This is the maximum voltage that can be applied at the gate terminal. Since all the device variants have the same gate oxide thickness; this voltage is the same for all the devices. R_{ON} improves by 40% when DL is optimized from 1× to 5×. When L_{OV} is varied from 0.35× to 1.8×, there is more than 50% improvement in R_{ON}. Specific ON-resistance (R_{sp}) is a key figure of merit (FoM) for power devices, which is defined as the product of the device area and R_{ON}. R_{sp} also shows a significant improvement with DL and L_{OV} optimization (Fig. 10). Breakdown voltage (V_{BD})

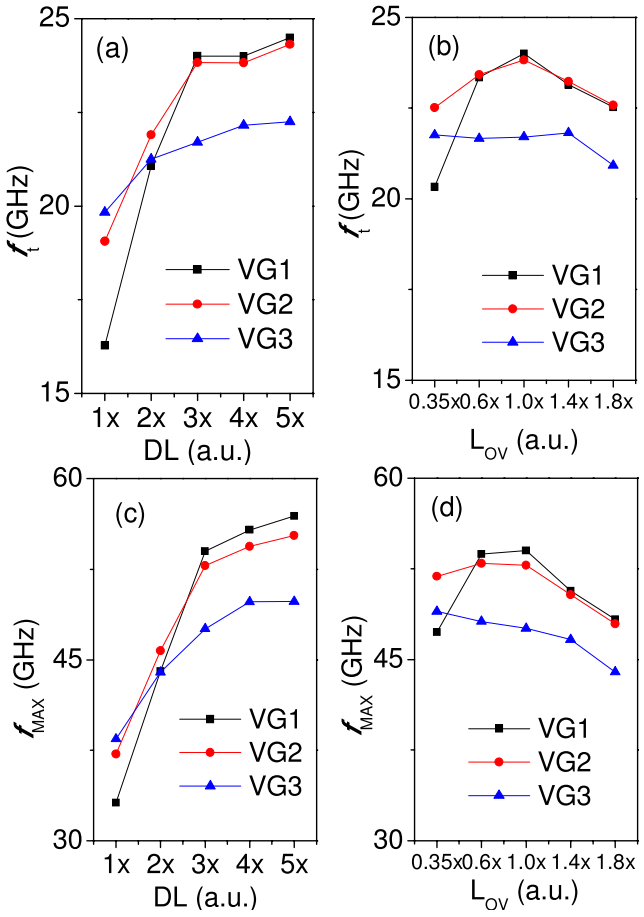

Fig. 13. Unity gain frequency (f_t) and maximum oscillations frequency (f_{max}) for various DL (a and c) and L_{OV} (b and d). (VG3 = 0.6 V, VG2 = 0.7 V, and VG1 = 0.8 V).

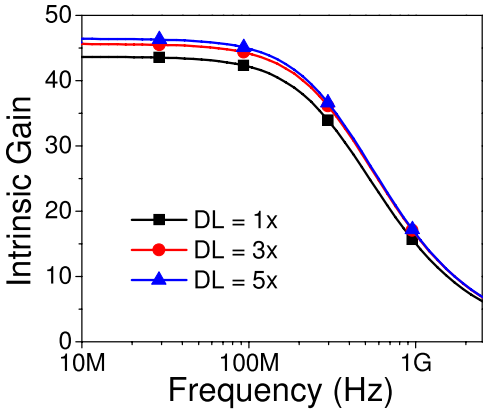

Fig. 14. Simulated small-signal intrinsic gain of the DeNMOS transistor plotted as a function of frequency for DL optimization. Gain of the device improves monotonously with DL.

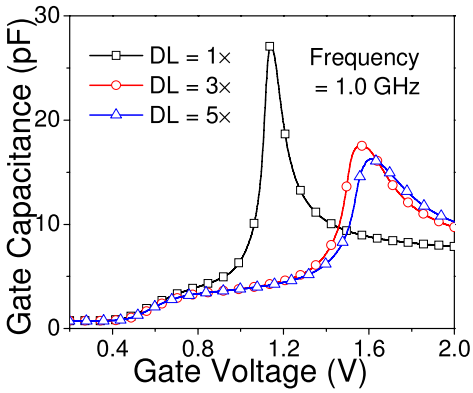

Fig. 15. Total gate capacitance of the device simulated at 1-GHz frequency. Significant reduction in the peak capacitance is observed with DL optimization.

divided by R_{ON} is an important FoM for a device to represent its power amplification capabilities [18]. Since the device uses a retrograde junction profile, the breakdown occurs deep inside the bulk at the n-well/p-well contact region, as shown in Fig. 11. By changing the lateral dimensions (i.e., DL and L_{OV}), the field profile does not change significantly in this region, and therefore, the breakdown voltage remains unchanged. V_{BD}/R_{ON} for DL and L_{OV} optimization is shown in Fig. 12, which follows the trend governed by R_{ON}.

IV. Small-Signal RF Performance

Small-signal device parameters, such as unity gain frequency (f_t) and maximum oscillation frequency (f_{max}), are shown in Fig. 13 as a function of DL and L_{OV} for multiple gate voltages. VG3, VG2, and VG1 are 0.6, 0.7, and 0.8 V, which correspond to weak, moderate, and strong channel inversion conditions in the device, respectively. f_t is extracted from small-signal S-parameters as the frequency where current gain drops to unity (i.e., $H_{21} = 0$ dB). This also corresponds to the intrinsic delay of the device. f_t in its simplified form can be expressed as

$$f_t = \frac{g_m}{2\pi (C_{gs} + C_{gd})} \approx \frac{1}{2\pi \tau_t} \quad (1)$$

where C_{gs} is the gate-to-source capacitance, C_{gd} is the gate-to-drain capacitance, and τ_t is the transit time between source and drain. Fig. 13(a) shows f_t for DL optimization. The higher values of DL improve the gm of device and also reduce the total gate capacitance. f_t of the device experiences combined effect of both of them and monotonically increases with DL. However, increase in L_{OV} improves the gm but simultaneously increases the total gate capacitance (C_{gg}) as well. Hence, f_t first increases due to an increase in gm but starts degrading after $L_{OV} = 1\times$ caused by a significant increase in C_{gg} [Fig. 13(b)]. f_{max} of a device is a narrow-band FoM, which is useful in classifying the device for the design of tuned amplifiers. This is in contrast to f_t, which is a wideband FoM more suitable for large-signal applications. f_{max} is also extracted from small-signal S-parameters as the frequency where unilateral power gain falls to unity. Fig. 13(c) and (d) shows the f_{max} characteristics of the device for DL and L_{OV} optimization, which follow similar trends as f_t.

Fig. 14 shows the small-signal gain (S_{21}) of the device as a function of frequency for 1-mm gate electrical width at a drain bias of 5 V and a gate bias of VG1. The gate voltage is chosen to bias RF PA in class-AB mode. Low-frequency gain of the device is given by gm $\times$ r_o, which improves by optimizing DL from $1\times$ to $5\times$. As the frequency increases, the gate capacitance starts suppressing the gain. Small-signal RF power

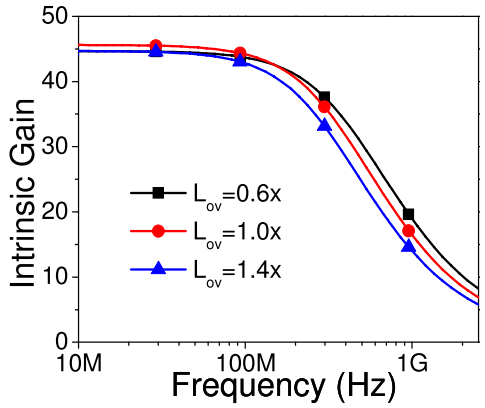

Fig. 16. Simulated small-signal intrinsic gain (S_{21}) of the DeNMOS transistor plotted as a function of frequency for L_{OV} optimization. At low frequency, S_{21} of the device first improves due to improved current density, and then degrades due to increase in total gate area.

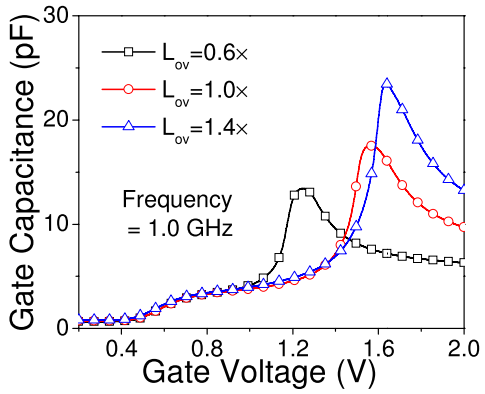

Fig. 17. Total gate capacitance of the device simulated at 1-GHz frequency. Peak capacitance increases due to increase in total gate area but also shifts toward higher gate overdrive due to relaxation in current crowding.

gain improves from 14 dB for DL = 1× to 15.5 dB for DL = 5× at 1 GHz, which is ∼45% in linear scale. Fig. 15 shows the total gate capacitance (C_{gg}) at 1 GHz as a function of gate bias voltage for multiple DL values. For DL = 1×, C_{gg} increases almost linearly up to the voltage where gm reaches maximum. After this point, C_{gg} increases nonlinearly and peaks at the gate bias where device enters into current saturation region. As DL is optimized to 5×, the magnitude of this nonlinear capacitance reduces and also pushed toward the higher value of gate bias. This happens due to the shift of current saturation region toward higher gate biases. S_{21} for L_{OV} optimization (Fig. 16) at low frequency first increases because of gm improvement and then decreases caused by the degradation in drift region resistance as discussed earlier. However, at a higher frequency (∼1 GHz), L_{OV} of 0.6× has a higher gain due to the shift in the 3-dB frequency to a higher value (because of smaller gate capacitance). By increasing L_{OV}, current saturation region shifts to the higher value of gate overdrive but unlike DL, and the peak value of nonlinear gate capacitance increases (Fig. 17). This happens because of an increase in the depletion region capacitance between the gate and n-well overlap.

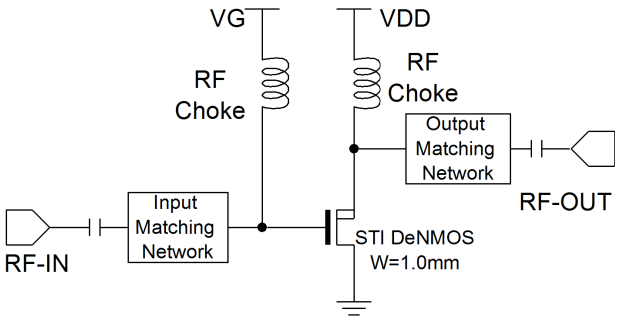

Fig. 18. Schematic of the complete PA circuit simulated under mixed-mode TCAD environment. Device input and output are matched to standard 50-Ω termination.

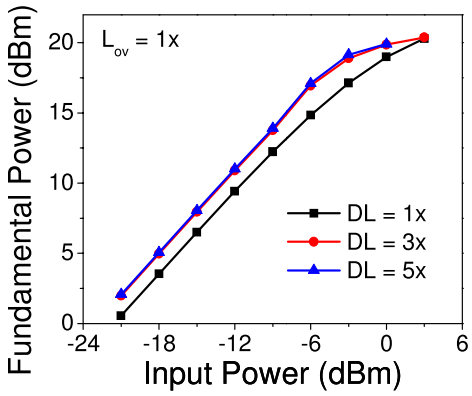

Fig. 19. Simulated output power delivered to 50-Ω load as a function of input power at a fundamental frequency of 1 GHz for various DL values.

V. Large-Signal RF Analysis

We further investigate the device performance for the large-signal RF applications by preparing a complete PA circuit. Input and output device impedances were matched to standard 50-Ω RF termination at an operational frequency of 1 GHz. Fig. 18 shows the PA circuit used as a test vehicle to benchmark the large-signal performance of the devices. DL and L_{OV} were optimized by keeping total device gate width to 1 mm. Gate and drain bias voltages were kept at VG1 and 5 V, respectively, for a class-AB mode of operation. Harmonic balance device simulation is reported earlier to check the device power and linearity [26]. But at large-signal levels, the nonlinear gate and drain capacitances of the device can change significantly. Therefore, more accurate mixed-mode time-domain simulations were performed. The time-domain simulations give a more accurate estimation, but at the expense of larger simulation time. Simulations were carried out for enough number of cycles to allow the circuit to reach steady state.

Fig. 19 shows the output power with respect to input power when circuit is excited with a fundamental frequency of 1 GHz. Standard device with DL = 1× delivers less power to the load despite matching at the input and the output. When DL is optimized to 3×, there is a significant change in the output power delivery of the PA circuit as shown. Further optimizing DL from 3× to 5× also shows a marginal improvement in the output power. This is in agreement with the improvement in intrinsic small-signal gain of the device, as shown in Fig. 14.

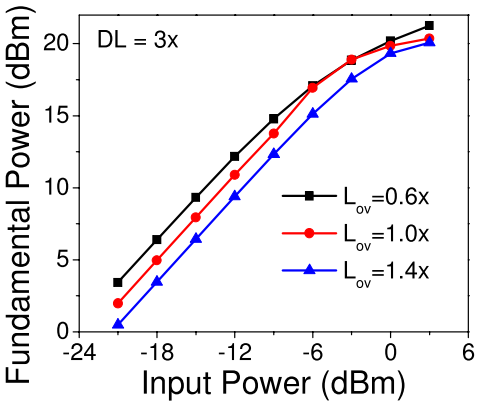

Fig. 20. Simulated output power delivered to 50-Ω load as a function of input power at a fundamental frequency of 1 GHz for various L_{OV} values.

Input–output power characteristic for L_{OV} optimization is shown in Fig. 20. The results are in agreement with the small-signal high-frequency intrinsic gain of the device, as shown in Fig. 16.

VI. Conclusion

In this paper, the STI DeMOS has been systematically analyzed and designed for device parameters such as drain DL and gate to n-well overlap (L_{OV}) by extensive TCAD-based simulations. The effect of these parameters is linked to device intrinsic behavior and various dc, analog, and RF FoMs. The presented analysis suggests the optimum value of DL and L_{OV} for various dc, analog, and RF FoMs. This optimization process helps in obtaining an improved device design window and also in the understanding of device physics for the optimum system-level RF performance.

References

[1] D. Yang, Y. Ding, and S. Huang, "A 65-nm high-frequency low-noise CMOS-based RF SoC technology," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 328–335, Jan. 2010.

[2] F. Arnaud *et al.*, "Technology-circuit convergence for full-SOC platform in 28 nm and beyond," in *IEDM Tech. Dig.*, Dec. 2011, pp. 15.7.1–15.7.4.

[3] C.-H. Jan *et al.*, "RF CMOS technology scaling in high-*k*/metal gate era for RF SoC (system-on-chip) applications," in *IEDM Tech. Dig.*, Dec. 2010, pp. 27.2.1–27.2.4.

[4] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers," *Proc. IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008.

[5] D. Marcon *et al.*, "Manufacturing challenges of GaN-on-Si HEMTs in a 200 mm CMOS fab," *IEEE Trans. Semicond. Manuf.*, vol. 26, no. 3, pp. 361–367, Aug. 2013.

[6] Y.-R. Wu, M. Singh, and J. Singh, "Sources of transconductance collapse in III-V nitrides—Consequences of velocity-field relations and source/gate design," *IEEE Trans. Electron Devices*, vol. 52, no. 6, pp. 1048–1054, Jun. 2005.

[7] J. Scholvin, D. R. Greenberg, and J. A. del Alamo, "Fundamental power and frequency limits of deeply-scaled CMOS for RF power applications," in *IEDM Tech. Dig.*, Dec. 2006, pp. 1–4.

[8] K. Lee *et al.*, "The impact of semiconductor technology scaling on CMOS RF and digital circuits for wireless application," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1415–1422, Jul. 2005.

[9] M. Shrivastava, J. Schneider, M. S. Baghini, H. Gossner, and V. Ramgopal Rao, "On the failure mechanism and current instabilities in RESURF type DeNMOS device under ESD conditions," in *Proc. IEEE Int. Rel. Phys. Symp.*, May 2010, pp. 841–845.

[10] M. Shrivastava, M. S. Baghini, H. Gossner, and V. Ramgopal Rao, "Part I: Mixed-signal performance of various high-voltage drain-extended MOS devices," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 448–457, Feb. 2010.

[11] M. Shrivastava, M. S. Baghini, H. Gossner, and V. Ramgopal Rao, "Part II: A novel scheme to optimize the mixed-signal performance and hot-carrier reliability of drain-extended MOS devices," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 458–465, Feb. 2010.

[12] Z. Parpia and C. A. T. Salama, "Optimization of RESURF LDMOS transistors: An analytical approach," *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 789–796, Mar. 1990.

[13] A. Gupta, R. Chauhan, V. Menezes, V. Narang, and H. M. Roopashree, "A robust level-shifter design for adaptive voltage scaling," in *Proc. Int. Conf. VLSI Design*, Jan. 2008, pp. 383–388.

[14] P. J.-H. Lee, D. G. Chen, A. Bermak, and M.-K. Law, "A high voltage zero-static current voltage scaling ADC interface circuit for micro-stimulator," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Jun. 2014, pp. 1380–1383.

[15] P. S. Swain, M. Shrivastava, H. Gossner, and M. S. Baghini, "Device–circuit co-design for beyond 1 GHz 5 V level shifter using DeMOS transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3827–3834, Nov. 2013.

[16] H. Xiao *et al.*, "A novel RF LDMOS fabricated with standard foundry technology," *IEEE Electron Device Lett.*, vol. 30, no. 4, pp. 386–388, Apr. 2009.

[17] T. Chang, H. L. Kao, Y. J. Chen, S. L. Liu, S. P. McAlister, and A. Chin, "A CMOS-compatible, high RF power, Asymmetric-LDD MOSFET with excellent linearity," in *IEDM Tech. Dig.*, Dec. 2008, pp. 1–4.

[18] D. Muller *et al.*, "High-performance 15-V novel LDMOS transistor architecture in a 0.25-μm BiCMOS process for RF-power applications," *IEEE Trans. Electron Devices*, vol. 54, no. 4, pp. 861–868, Apr. 2007.

[19] M. Shrivastava, H. Gossner, and C. Russ, "A drain-extended MOS device with spreading filament under ESD stress," *IEEE Electron Device Lett.*, vol. 33, no. 9, pp. 1294–1296, Sep. 2012.

[20] Y. Shi, N. Feilchenfeld, R. Phelps, M. Levy, M. Knaipp, and R. Minixhofer, "Drift design impact on quasi-saturation & HCI for scalable N-LDMOS," in *Proc. IEEE 23rd Int. Symp. Power Semiconductor Devices ICs*, May 2011, pp. 215–218.

[21] A. Gupta *et al.*, "Drain extended MOS device design for integrated RF PA in 28 nm CMOS with optimized FoM and ESD robustness," in *IEDM Tech. Dig.*, Dec. 2014, pp. 3.5.1–3.5.4.

[22] A. Chatterjee, S. Pendharkar, Y.-Y. Lin, C. Duvvury, and K. Banerjee, "A microscopic understanding of nanometer scale DENMOS failure mechanism under ESD conditions," in *IEDM Tech. Dig.*, Dec. 2007, pp. 181–184.

[23] J. Roig, P. Moens, F. Bauwens, D. Medjahed, S. Mouhoubi, and P. Gassot, "Accumulation region length impact on 0.18 μm CMOS fully-compatible lateral power MOSFETs with shallow trench isolation," in *Proc. Int. Symp. Power Semiconductor Devices ICs*, Jun. 2009, pp. 88–91.

[24] S. Mouhoubi, F. Bauwens, J. Roig, P. Gassot, P. Moens, and M. Tack, "Solutions to improve flatness of Id-Vd curves of rugged nLDMOS," in *Proc. Int. Symp. Power Semiconductor Devices ICs*, 2011, pp. 200–203.

[25] S. Reggiani *et al.*, "Analysis of HCS in STI-based LDMOS transistors," in *Proc. IEEE Int. Rel. Phys. Symp.*, May 2010, pp. 881–886.

[26] C.-Y. Chen, O. Tornblad, and R. W. Dutton, "Linearity analysis of lateral channel doping in RF power MOSFETs," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3389–3394, Dec. 2009.

Ankur Gupta (S'14) is currently pursuing the Ph.D. degree in electrical engineering with IIT Bombay, Mumbai, India.

He was a Circuit Designer with Texas Instruments, Bangalore, India, where he developed high-voltage and low-power interfacing circuits. He has several papers and patent in the field of high-voltage device and circuit design. His current research interests include high-voltage device design, RF microelectronics, and device–circuit co-design.

Mayank Shrivastava (S'09–M'10) received the Ph.D. degree from IIT Bombay, Mumbai, India, in 2010.

He is currently an Assistant Professor with the Indian Institute of Science, Bangalore, India. He has over 40 publications in international journals/conferences and has 23 patents issued or pending in his field of interest. His current research interests include advanced and beyond CMOS, On-chip ESD protection, and power devices.

Maryam Shojaei Baghini (M'00–SM'09) received the M.S. and Ph.D. degrees in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 1991 and 1999, respectively.

She joined the Department of Electrical Engineering, IIT Bombay, Mumbai, India, in 2001, as a Post-Doctoral Fellow, where she is currently a Professor.

Dr. Shojaei is a joint recipient of 11 awards.

Dinesh Kumar Sharma (SM'–) received the Ph.D. degree from the Tata Institute of Fundamental Research, Mumbai, India.

He has been with the Department of Electrical Engineering, IIT Bombay, Mumbai, since 1991, where he is currently a Professor. His current interests include mixed-signal design, interconnect technology, and the impact of technology on design styles.

Dr. Sharma is a fellow of the Institution of Electronics and Telecommunication Engineers.

Harald Gossner (M'06–SM'11) received the B.S. (Dipl.Phys.) degree in physics from the Ludwig-Maximilians-Universität München, Munich, Germany, and the Ph.D. degree in electrical engineering from Universität der Bundeswehr, Munich, in 1990 and 1995, respectively.

He is currently a Senior Principal Engineer with Intel Mobile Communications, Munich, where he is involved in the development of robust mobile systems.

Valipe Ramgopal Rao (M'98–SM'02) received the M.Tech. degree from IIT Bombay, Mumbai, India, in 1991, and the Dr.Ing. degree from Universität der Bundeswehr München, Munich, Germany, in 1997.

He is currently a P. K. Kelkar Chair Professor with the Department of Electrical Engineering and the Chief Investigator with the Centre of Excellence in Nanoelectronics, IIT Bombay.