Sub 0.5 V Operation of Performance Driven Mobile Systems Based on Area Scaled Tunnel FET Devices

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***Abstract*— Advanced mobile applications demand low power and high performance systems. In this paper, a technology computer aided design (TCAD)-based feasibility investigation of a recently proposed area tunneling field effect transistor (FET) structure is carried out from the point of high volume and ultralow power mobile applications. We demonstrate that for realization of future ultralow power and high performance systems, unique properties of area tunneling class of tunnel FET structures need to be employed. These devices are realized by engineering the tunneling region profile and tunneling cross-sectional area. The optimized devices are found to leverage up to ∼7× energy reduction when compared with the 20-nm node MOS device options while meeting the high performance targets. Device design insights for such an area tunneling class of tunnel FET structures are discussed in this paper for the first time. It is shown that by lowering the supply voltage below 0.5 V, up to 10× reduction of the energy delay product is feasible by using area tunneling devices.**

***Index Terms*— Area tunneling field effect transistor (FET), energy minimization, line tunneling FET and TFET, low voltage operation, SOC, tunnel field effect transistor.**

I. Introduction

A SURGE in handheld consumer electronics such as smart phones and tablet PCs [1] requires to minimize active and leakage power [2]–[4] by scaling down the supply voltage below 0.5 V. This needs to be done while still maintaining acceptable operating frequencies in a few GHz range. CMOS technologies do not offer much design space in the sub 0.5 V operating regime, because of their limited subthreshold swings, which cannot be scaled below 60 mV/dec at room temperature [5].

The proposed steep subthreshold device [6], known as tunnel FET, is found to be energy-efficient only at low frequency [7], [8] as it suffers from either a low subthreshold slope [9] or a low I_{ON} [10], [11]. In the past, several remedies were proposed to circumvent the low ON current [12]–[15]. As shown in Fig. 1(a), in conventional tunnel field effect transistor (TFET) devices, tunneling takes place within 1–2 nm (T_{TUN}) of inversion layer; however, the fundamental bottleneck is that T_{TUN} cannot be increased significantly by changing technology or process parameters, so drive current is limited by tunneling area ($W \times T_{TUN}$), W being the device width.

Recently, a new class of tunneling devices have been proposed that resolve this problem by allowing tunneling across a wider area under the gate [16]–[24]. These devices possess a large tunneling cross section ($W \times L_G$); therefore we call them as area tunneling FET devices. As the underlying device behavior differs from known MOS devices, the question arises how logic circuits, e.g., inverter chains will perform when area tunneling devices are used. In this paper, we compare power and performance behavior of low V_T, high V_T MOS and area tunneling devices using detailed technology computer aided design (TCAD) simulations. While detailed tunneling models are still under development [25], [26], fundamental trends in the circuit behavior of tunnel FET circuits can be extracted using the methodology presented in this paper. Out of the various proposed area scaled devices, the sandwiched barrier tunnel FET (STBFET) is used in this paper as a reference for implementation of an area scaled device [Fig. 1(a)] [21] for further circuit analysis. It roughly possesses a tunneling area, which increases with L_G for very small gate lengths and then reaches a saturation for $L_G > 20$ nm.

This paper is organized as follows. Section II describes the simulation setup and methodology used for device assessment, while device optimization is described in Section III. This is followed by an investigation of the feasibility of area scaled devices along with MOSFET and TFET devices for system assessment based on delay, energy, and energy-delay product (EDP) matrix for sub 0.5 V supply voltage operation.

II. Simulation Setup and Methodology

A. Simulation Setup

We used a well-calibrated TCAD setup with drift-diffusion transport and nonlocal band-to-band tunneling model [27] for capturing the tunneling phenomenon. The nonlocal model uses Wentzel–Kramer–Brillouin approximations to calculate the tunneling probability using electron-hole wave-vector throughout the tunneling path. Since we have used SiGe in this paper, mobility and tunneling models were calibrated against experimental data of SiGe MOSFET and TFET devices presented in [12] and [28] [Fig. 2(a) and (b)]. Quantum confinement

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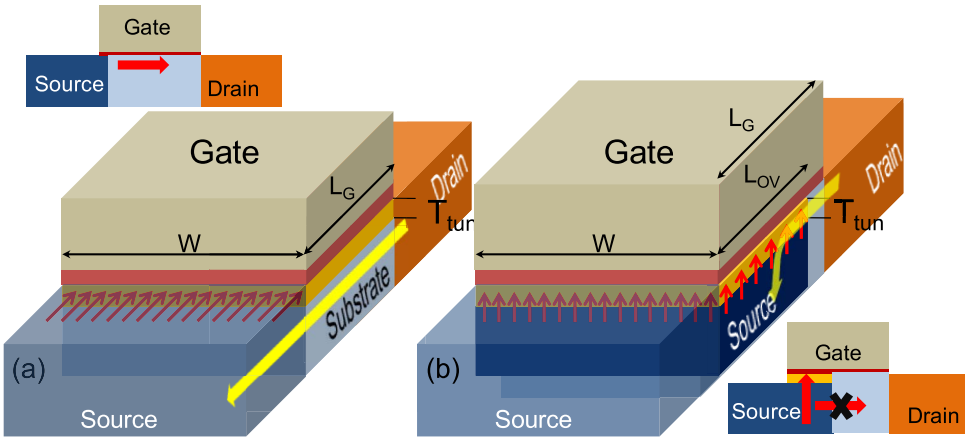

Fig. 1. Cross sectional diagram of (a) conventional or width scaled TFET and (b) nonconventional or area scaled TFET. In a width scaled TFET, direction of electron tunneling (red arrows) is normal to source-channel interface and tunneling cross section is given by $W \times T_{\mathrm{TUN}}$. As T_{TUN} is a few nm, tunneling can be viewed as point tunneling in 2-D picture. While in an area scaled TFET, tunneling appears as line tunneling in 2-D scenario that occurs normal to source pocket interface with a tunnel cross section $W \times L_{\mathrm{OV}}$. L_{OV} is source overlap under gate that can be made larger equivalent to the channel length L_G. Solid yellow arrow: direction of current flow in the device which for the case of a conventional TFET flows parallel to gate while for area scaled TFET case, flows normal to gate under source gate overlap and again parallel to gate under spacer region.

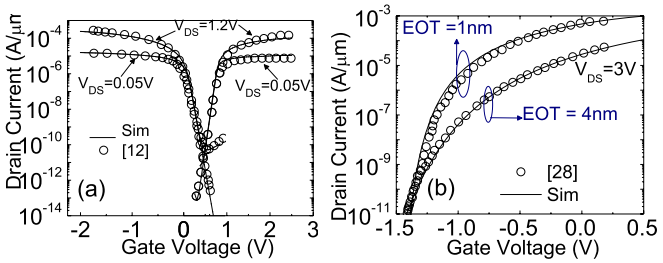

Fig. 2. Calibration of drift-diffusion models for (a) SiGe-based MOSFET from [12] and (b) band-to-band tunneling models from [28].

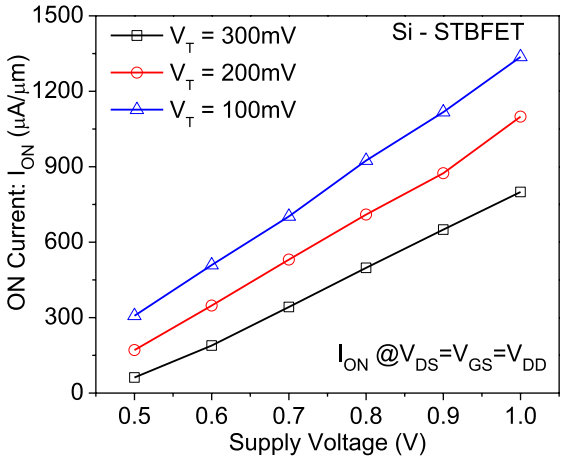

Fig. 3. Silicon STBFET (N-Type) ON current as a function of supply voltage for different threshold voltages. When supply voltage varies from 1 to 0.5 V, the ON current decreases by five times for a V_T = 100-mV device. Sandwich barrier tunnel FET using a SiGe source is an implementation of an area scaled TFET.

due to strong electric gate field as recently reported by Vandenberghe *et al.* [29], which reduces density of states and increases bandgap which in turn affects the tunneling rate, could be neglected to first order, as the impact of quantization on tunneling rate is much less relevant in a heterostructure device having an epitaxial layer thickness of more than 2 nm as compared with a purely Si-based device [30]. Strain in a Si/SiGe hetrostructure will increase the I_{ON} [31]. However, in this paper we did not consider those effects.

B. Methodology

For the energy-performance evaluation, a loaded inverter stage with a fan-out of 1 is used with a load capacitance of 2.4 fF (C_{INT}). The input pulse to the inverter has a rise and fall time of 20 ps and the maximum and minimum of voltages are V_{DD} and 0, respectively. The width of P-type (N-type) device is set for the same drive current at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = V_{\mathrm{DD}}$ as that of N-type (P-type) width of 30 nm, if I_{ntype} $(A/\mu\mathrm{m}) > I_{\mathrm{ptype}}$ $(A/\mu\mathrm{m})$ and vice versa. Standard definition of delay is used to extract per stage delay [32]. Total energy (E_{total}) is the sum of static energy (E_{static}) due to off current and dynamic energy during switching activity including a probability of such event (α). Dynamic energy is calculated by integrating the pull-up transistor current and voltage waveforms for one-half cycle (E_{pMOS}) and other-half for pull-down device (E_{nMOS}) using TCAD mixed-mode simulation results. It should be noted that we have made no deliberate attempt to minimize the overall energy, except for fixing the leakage current at 1 pA/μm, for a fair comparison between the different classes of devices.

C. Voltage Scaling

As per International Technology Roadmap for Semiconductors (ITRS) [4], I_{ON} at $V_{\mathrm{DS}} = V_{\mathrm{GS}} = V_{\mathrm{DD}}$ is required to have a value of 550/350 μA/μm for low-operating power/low-standby power mode of operation for an nMOS. Fig. 3 shows the extracted ON current (I_{ON}) plot as a function of supply voltage for three different V_T values for an area scale device. Different V_T is achieved by varying doping concentration in epitaxial layer. Here, V_T is defined at a gate voltage where the device exhibits a sharp rise in the drain current. As the supply

TABLE I
DEVICE AND ELECTRICAL PARAMETERS

Device Parameters	Value
L_G (nm)	20
EOT (nm)	0.4, 0.6, 1.0
T_{BODY} (nm)	15
T_{BULK} (nm) (MOS-HP)	60
T_{EPI} (nm)	2
Source/Drain doping (cm^{-3})	10^{20}
WF (eV) (n-type)	4.1
WF (eV) (p-type)	4.9
Ge mole fraction (%)	30

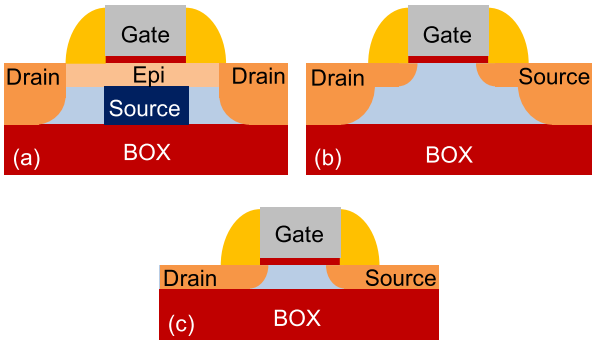

Fig. 4. Schematic representation of cross section of the devices used in this paper with LG = 20 nm. (a) STBFET. (b) High performance MOSFET (MOS-HP). (c) Low power MOSFET (MOS-LP). In STBFET devices, source is n++ (p++) in the case of N-type (P-type) operation.

voltage is reduced from a nominal value of 1.0 to 0.5 V, the I_{ON} reduces by five times from its nominal value at 1 V, for the area scaled TFET with 100 mV V_T. This reduction becomes severe in a high V_T device (300 mV) where I_{ON} reduction by an order of magnitude can be seen. An order of magnitude reduction in I_{ON} will make the circuit at least five times slower.

D. Motivation to Use SiGe: Challenges With All-Silicon STBFET

We have used SiGe as a technological option because of its CMOS compatibility to maintain a moderate level of I_{ON} with low supply voltages, which was previously investigated in [33]–[37]. However, replacing silicon with $Si_{1-x}Ge_x$ is also likely to increase the off state leakage current, hence it is required to use heterostructure-based area scaled devices [28], [38]–[40].

III. OPTIMIZED DEVICES

Fig. 4 shows various devices under investigation which include a STBFET as example of an area scaled TFET, a high performance MOSFET (MOS-HP), and a low power MOSFET (MOS-LP). We have used gate length of 20 nm (L_G) and three different equivalent oxide thicknesses (EOTs) (0.4, 0.6, and 1 nm) while other details can be seen from Table I. The present investigation is shown for a silicon-on-insulator (SOI) process but similar trends are applicable for an equivalent bulk process. In the following sections, we will discuss about optimization of these devices.

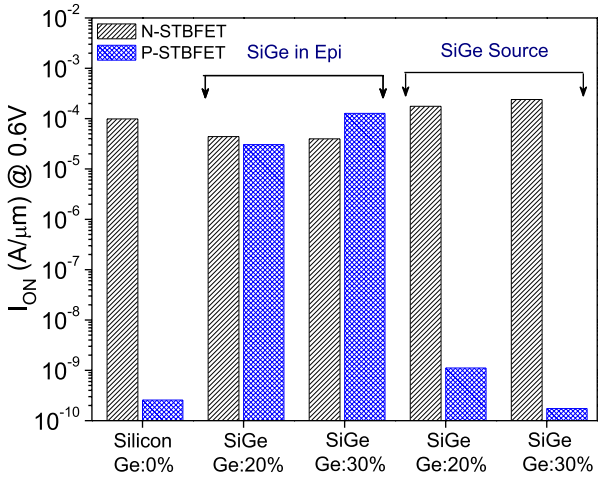

Fig. 5. Impact of introducing SiGe on the ON current at 0.6 V supply voltage for various STBFETs. For N-type STBFET, source contains SiGe while for the case of P-STBFET, SiGe is used in the Epi region. The current increases by 3× and 10^5× with 30% Ge content for N and P type STBFETs, respectively.

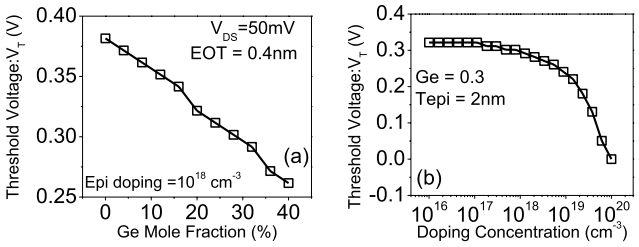

Fig. 6. Impact of (a) Germanium content and (b) epi doping on threshold voltage for N-STBFET, V_T decreases linearly with an increase in Ge mole fraction.

A. STBFET

Fig. 5 shows extracted I_{ON} at V_{DD} = 0.6 V and I_{OFF} = 1 pA/μm for various $Si_{1-x}Ge_x$ device options and the results are compared with an all silicon device. As mentioned earlier, use of an all Si device does not give CMOS comparable currents and the currents are <100 μA/μm. However, it can be seen from the figure that we need to use $Si_{1-x}Ge_x$ at source for N-type while P-type devices contain a $Si_{1-x}Ge_x$ epi for CMOS compatible currents. Therefore, for this paper we use SiGe source for N-STBFET and SiGe epitaxial layer for P-STBFET.

Justification of using other parameters is as follows.

1) Effect of Ge Mole Fraction on Threshold Voltage: if Ge concentration x is increased in $Si_{1-x}Ge_x$, its bandgap reduces, which in turn increases the carrier tunneling rate, thereby reducing the voltage to get a certain amount of carriers [Fig. 6(a)]. A similar effect of epitaxial layer doping on the V_T can be seen by Fig. 6(b). Fig. 7(a) shows the effect of varying epitaxial layer thickness on the threshold voltage for a fixed 30% Ge content. A thinner epitaxial layer/pocket depletes completely in comparison with a thicker one. In this case, a higher gate voltage is required to invert the epilayer.

Fig. 7(b) shows the effect of epi thickness on I_{ON}. As stated earlier, thinner epitaxial layer results in a higher V_T.

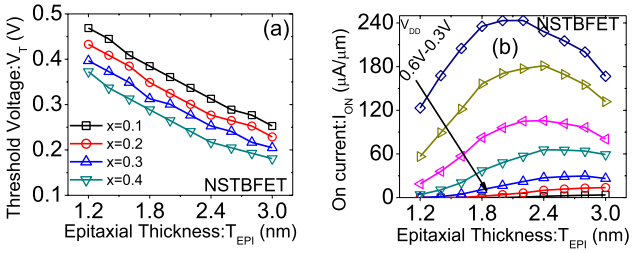

Fig. 7. Impact of epitaxial thickness on (a) V_T with different values of Ge for a constant 0.5 V supply and (b) I_{ON} with different value of supply voltage (varied from 0.6 to 0.3 V in 0.05 V step) for a fixed 30% Ge content (x).

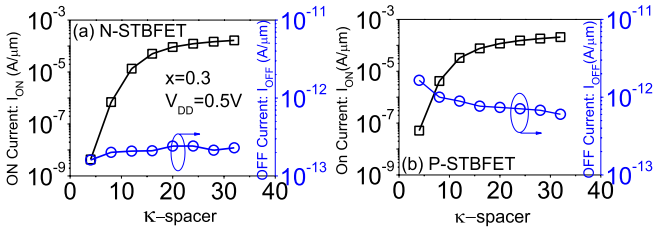

Fig. 8. Impact of κ spacer on the I_{ON} and I_{OFF}. (a) N-STBFET. (b) PSTBFET. A high-κ spacer improves ON current.

Therefore I_{ON} current in this case will be V_T limited. As epitaxial layer thickness is increased, tunnel width decreases and I_{ON} increases. A further increase in the thickness, however, degrades I_{ON} again, because the thicker epitaxial layer reduces gate control over tunnel junction. There is a window of variation in epi thickness of ± 0.2 nm which only yields $<10\%$ I_{ON} degradation from its maximum value.

2) Effect of Spacer Dielectric Constant κ: The conductivity of region beneath spacers is modulated by gate fringing field through spacer coupling after the devices turns on. In Fig. 8, the effect of varying the κ of spacer on I_{ON} is shown. At lower values of dielectric constant, such as SiO_2 ($\kappa = 3.9$), higher epi resistance limits the current. Employing a high-κ material mitigates this effect until it is again limited by tunnel junction resistance. The I_{OFF} does not have a strong dependence on spacer κ for both N- and P-type devices, which is apparent from Fig. 8.

Based on a careful examination of the dependence of electrical quantities on material parameters and device geometry, a STBFET device with a 2-nm thick epitaxial layer, a high κ ($\kappa = 21$) spacer, and 30% Ge content is used for circuit assessment.

B. MOSFET

We selected two MOSFET flavors for this paper. A high performance MOSFET (MOS-HP), which is a SOI MOS device, is selected based on the recommendations of ITRS [4] having an I_{OFF} of 100 nA/μm. A body thickness (T_{BULK}) of 60 nm, and a 1.2×10^{18} cm^{-3} channel doping is used. A low power MOSFET (MOS-LP), which is based on a fully depleted SOI technology, having a high V_T is also optimized for a leakage current 10^{-12} A/μm at different supply voltages using a 15-nm thick body (T_{BODY}). The substrate doping is

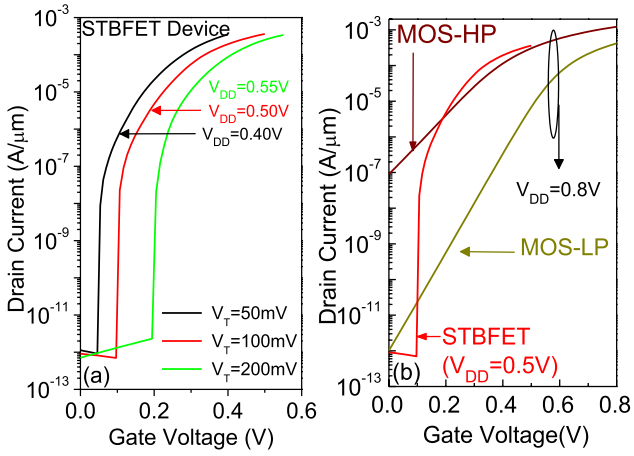

Fig. 9. Simulated transfer characteristics (a) for area scaled device with varying V_T, where V_T is defined at a gate voltage where the device exhibits a sharp rise in drain current (arrows point drain voltage used). (b) Both MOSFETs and an area scaled device ($V_T = 100$ mV).

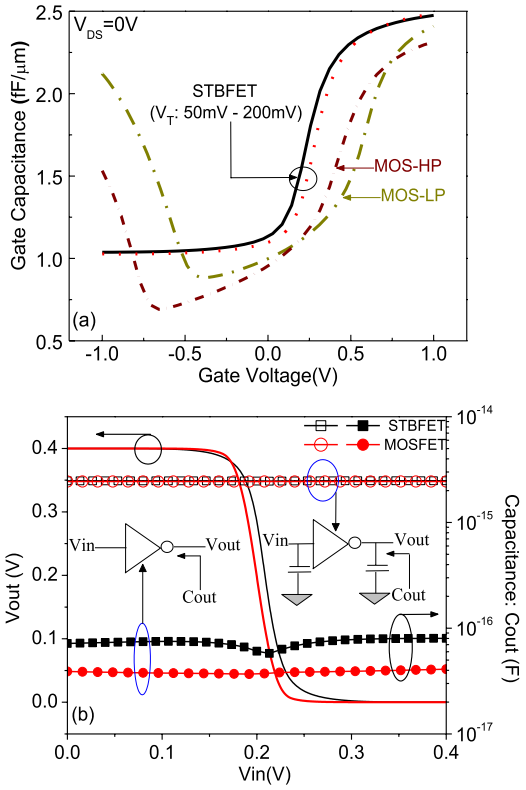

Fig. 10. (a) Simulated gate capacitance of the devices. (b) Inverter transfer characteristics and capacitance of a STBFET and a MOSFET. As maximum gate capacitance value lies 2–2.5 fF/μm for all the devices having Wp/Wn = 3 with Wn = 30 nm, absolute device capacitance ($\sim 10^{-17}$ F) is always of two orders lower compared with the load capacitance C_{INT} (2.4 fF).

used as a parameter for leakage current optimization. For both the MOSFETs we used 15-nm spacers.

IV. Logic Performance Comparison

A. Delay–Power Versus Supply Voltage

Fig. 9 shows the simulated I_{DS}–V_{GS} characteristics of the devices. In Fig. 9(a), the characteristics of STBFET for

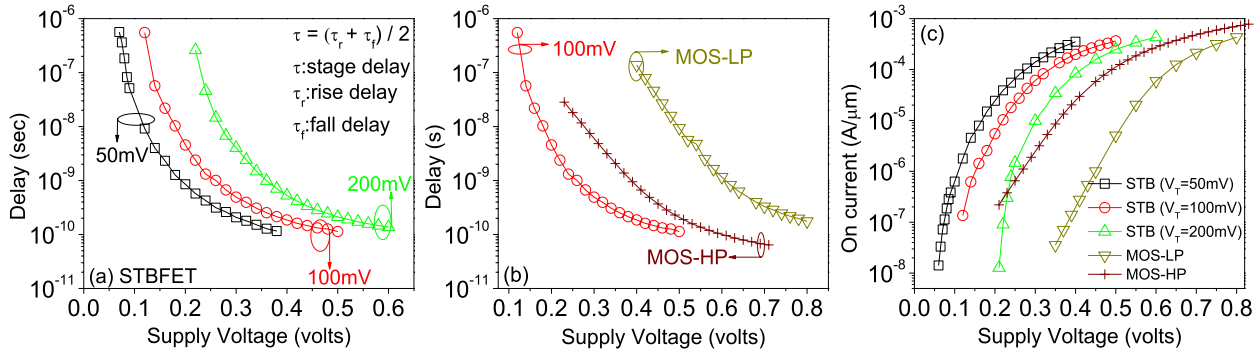

Fig. 11. Delay versus supply voltage for (a) STBFET devices, (b) for MOSFETs and TFET, and (c) I_{ON} at $V_{GS} = V_{DS} = V_{DD}$. Roughly delay is given by $C_L V_{DD}/I_{ON}$ hence for a fixed C_L (2.4 fF) device that shown in better I_{ON} for a given V_{DD} gives a better performance.

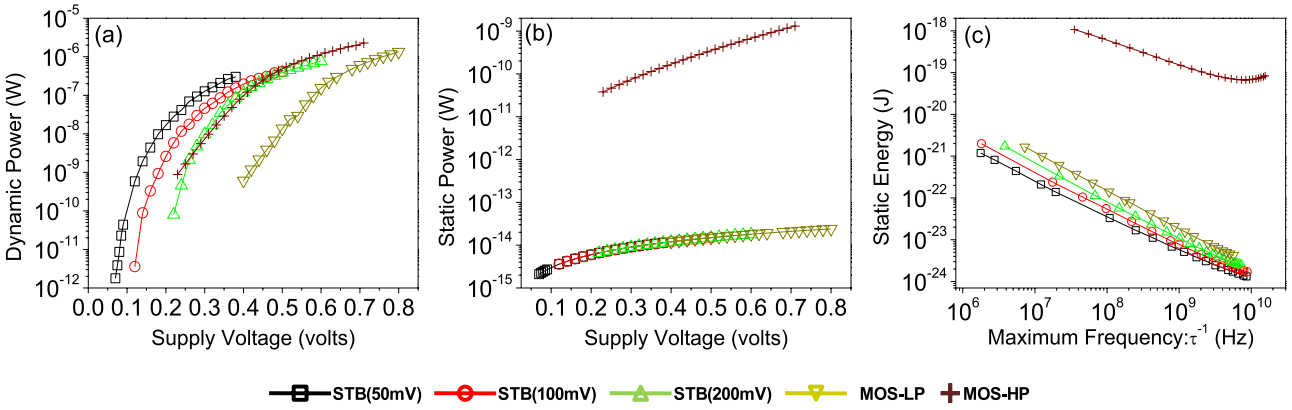

Fig. 12. (a) Dynamic power, (b) static power, and (c) static energy ($E_{st} = P_{st} \times \tau$) where τ being the stage delay. A MOS-HP dissipates more energy in idle state than the rest of the devices. This becomes worse at low operating frequencies making these devices unsuitable for applications where high battery life is required in idle state.

different V_T are shown. In Fig. 10(a), the simulated gate capacitance is shown as a function of gate voltage at a drain voltage of 0 V. For all devices, the capacitance magnitude is in the range of a few fF/μm. For a minimum sized inverter ($W = 30$ nm), the device capacitance is $\ll C_{INT}$ (2.4 fF), which is apparent from Fig. 10(b) where a minimum sized inverter output is shown for both with and without loads cases. This shows that even though output capacitance is different for a MOSFET and a STBFET for isolated devices, it remains constant for loaded case, which is solely dictated by the external capacitance.

The extracted delay is shown as a function of supply voltage in Fig. 11(a) for all the STBFET devices while Fig. 11(b) depicts the rest of the devices. For higher supply voltages (> 0.5 V), STBFET delay is comparatively larger than MOS-HP delay because of ON current reduction at higher drain current. This happens because of the resistance offered by a thinner (2 nm) epitaxial layer. Nevertheless, it can be seen clearly that a MOSFET equivalent delay is achieved at a lower supply voltage (< 0.5 V) by STBFET inverter due to its high driving capability [Fig. 11(c)]. The considered MOS-LP is a high V_T device, which operates mostly in subthreshold region in our investigation [Fig. 9(b)] leading to a lower I_{ON}. Hence, it is required to apply a larger V_{DD} to achieve a lower delay. Fig. 12(a) shows the dynamic power ($P_{dyn} = E_{dyn}/\tau$) for the devices plotted as a function of supply voltage scaling. Since the dynamic power roughly goes by CV^2/τ, obviously the devices that show lower delay at a given V_{DD} also result in larger dynamic power dissipation. Static power ($I_{OFF} \times V_{DD}$) dissipation can be seen from Fig. 12(b), where all device characteristics except MOS-HP overlap due to a constant leakage current (1 pA/μm). However, a remarkable difference between the MOS-HP device power compared with other devices is visible because of the high device leakage current ($\sim$100 nA/μm).

B. Energy Versus Performance

For handheld and mobile applications a longer battery life in idle state has always been of paramount interest, which is governed by energy consumption in the device. For this purpose, static energy ($P_{st} \times \tau$) is shown in Fig. 12(c) as a function of maximum operating frequency (τ^{-1}).

Fig. 12(c) shows the limitation of use of MOS-HP in applications where very low signal activity and longer battery life are desired. The reason for this behavior is that all devices except MOS-HP have got a very low leakage. Therefore, at a lower operating frequency and for a fixed V_{DD}, it is important to optimize the device for a lower leakage current. Fig. 13 shows the total energy per operation as a function of performance (operating frequencies) for 0.01 activity factor, where open symbols represent the extraction from transient

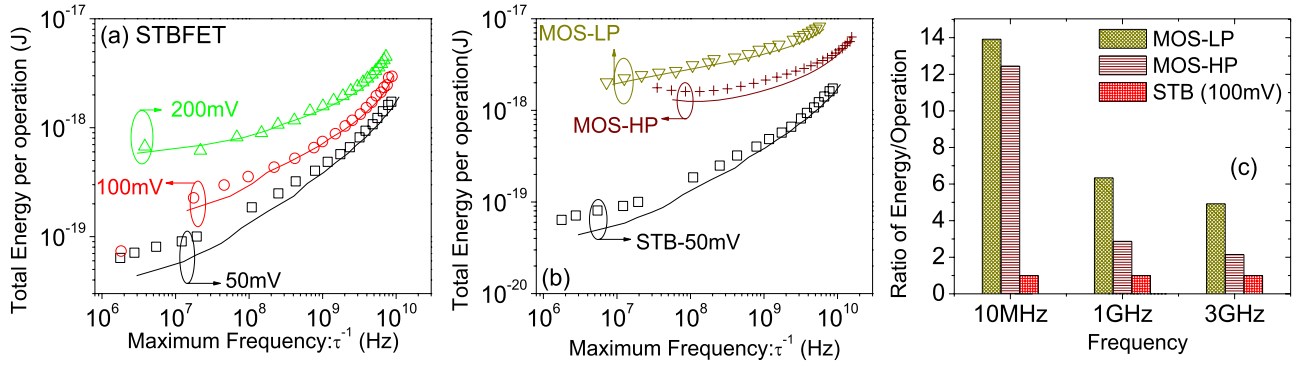

Fig. 13. Total energy per operation versus performance for 0.01 activity factor (a) for a STBFET ($V_T = 50$ mV), and MOSFETs (b) for STBFET devices. Symbol: TCAD-based extraction and line analytical [41] calculations. A low V_T STBFET can be used with a lower supply voltage resulting in low energy dissipation. A high V_T MOS-LP requires a high V_{DD} to meet the targeted performance requirements but leads to higher energy dissipation. (c) STBFET (100 mV) leads to an energy saving of ~7× (3×) in comparison with MOS-LP (MOS-HP) at 1-GHz frequency.

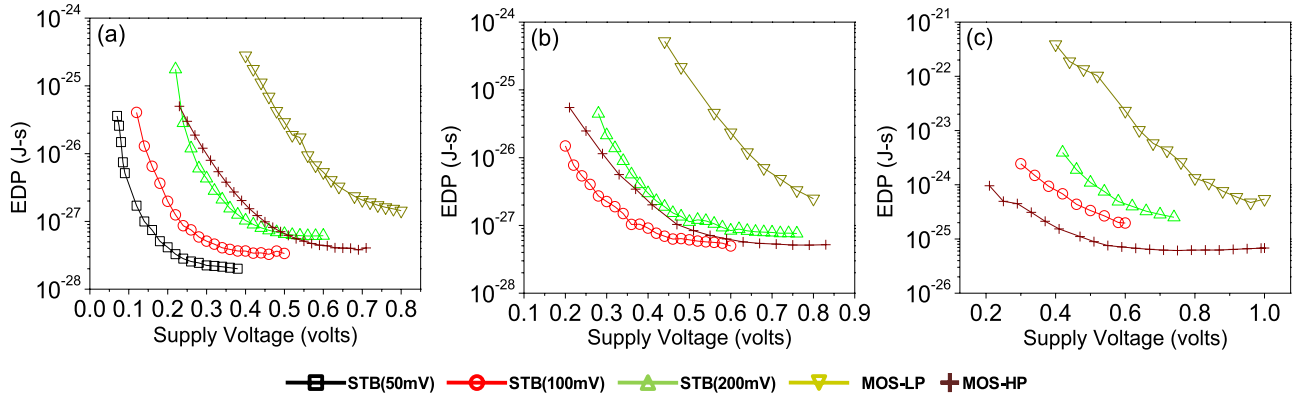

Fig. 14. EDP for (a) EOT = 0.4 nm, (b) EOT = 0.6 nm, and (c) EOT = 1 nm. It can be seen that with a STBFET, EDP can be minimized at sub 0.5 V supply voltages compared with other devices.

device simulation while the solid lines are generated using (1) [41]

$$E_a = V_{DD}^2 C L_d^2 f^2 \left(\frac{\alpha}{2 L_d f} + \frac{I_{off}}{I_{on}} \right) \quad (1)$$

where $L_d = 1$ (logic depth), $\alpha = 0.01$ (activity factor), $C =$ 2.4 fF, and $f = 1$ (fan out). I_{ON} and I_{OFF} at V_{DD} are extracted from TCAD simulations. Fig. 13(a) compares STBFET ($V_T =$ 50 mV) with MOSFET and TFET devices while Fig. 13(b) compares STBFETs having a different threshold voltage values. Because of the relatively higher ON currents at lower supply voltages and a lower leakage current, STBFET devices consume lesser energy for operating frequencies <4-GHz. MOS-LP devices require a higher V_{DD} for achieving the targeted performance [Fig. 11(b)] leading to an overall higher energy dissipation per operation. A MOS-HP although uses a similar V_{DD} as that of area scaled TFET, its higher static energy leads to an increased overall energy in the low to medium frequency region as shown in Fig. 12(c). Fig. 13(c) shows the relative energy per operation for the $V_T = 100$-mV STBFET, for MOS-HP and MOS-LP. It is evident from the figure that, with the STBFET, a ~5×, ~7×, and ~14× improvement can be obtained at 3 GHz, 1 GHz, and 10-MHz frequency, respectively, compared with the MOS-LP.

C. Energy-Delay Product Versus Supply Voltage

Some demanding applications on mobile devices require a sufficient level of performance. In all those applications, it is necessary to take the EDP into account for device assessment [41]. In Fig. 14, the different tunnel FET devices are compared. Due to higher energy and higher delay, the MOS-LP could not be used in such applications. A MOS-HP leads to a minimum EDP similar to STBFET, though the performance of the STBFET is quite superior at lower supply voltages. Shrinking of EOT enhances the performance of the STBFET further (Fig. 14). The reason for this behavior is that, at reduced EOTs, gate control over epitaxial region improves, which enhances I_{ON}. This is manifested in a lower EDP product.

V. Conclusion

This paper clearly showed that area scaled TFET structures with appropriate I_{ON} can fulfill the requirements of GHz operation at voltages below 0.5 V. Extreme low voltage operation of logic chains benefitted from high I_{ON} and super-steep subthreshold swing characteristics of area tunneling tunnel devices giving rise to a 7× (3×) saving in energy when compared with MOS-LP (MOS-HP), respectively, at 1-GHz operation. The predicted 10× reduction of EDP of area tunneling devices, such as STBFETs compared with MOSFETs (EOT = 0.4 nm)

at sub 0.4 V supply voltage operation would lead to a quantum leap for processors in mobile applications.

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