A Review on the ESD Robustness of Drain-Extended MOS Devices

Mayank Shrivastava, *Member, IEEE*, and Harald Gossner, *Senior Member, IEEE*

(Invited Paper)

***Abstract*—This paper reviews electrostatic discharge (ESD) investigations on laterally diffused MOS (LDMOS) and drain-extended MOS (DeMOS) devices. The limits of the safe operating area of LDMOS/DeMOS devices and device physics under ESD stress are discussed under various biasing conditions and layout schemes. Specifically, the root cause of early filament formation is highlighted. Differences in filamentary nature among various LDMOS/DeMOS devices are shown. Based on the physical understanding, device optimization guidelines are given. Finally, an outlook on technology scaling is presented.**

***Index Terms*—Drain engineering, drain-extended MOS (DeMOS), electrostatic discharge (ESD), filamentation, laterally diffused MOS (LDMOS) SCR, moving filament, rugged LDMOS, safe operating area (SOA), space-charge modulation.**

I. Introduction

THE most common device used in smart power technologies (SPT) is the laterally diffused MOS (LDMOS). Fig. 1(a) and (b) show two types of LDMOS devices, one with a field oxide (FOX) in the drift or laterally diffused drain region and the other without FOX inside the drift region. The primary feature of LDMOS devices is to sustain very high voltage and high currents, due to which they are widely used as motor controllers and drivers in the high-performance ASICs required for automotive applications. Beyond automotive applications, LDMOS devices are widely used in liquid-crystal display driver ICs, power amplifiers, line drivers, buck or DCDC converters and power management ICs. On one hand, these applications have seen a continuous increase in its demand due to ongoing integration of electronic features into mechanical operations or with several other electrical/electronic features. However, on the other hand, several thriving electrical requirements also come along with their operation in such applications, where they have to comply with overvoltage, reverse voltage, operation under wide temperature range and electrostatic discharge (ESD) conditions.

Use of LDMOS devices today goes beyond smart power technologies. Portable devices like smart phones, digital cameras and MP3 players demand ultrafast connections, as well as high-voltage capable interfaces, suitable for transferring large amounts of data, for example USB3.0, which combines 5-Gbit/s speed requirements and 5-V operation. ICs serving this market are often processed in sub-65-nm node CMOS processes. A cost-efficient way to implement a high-voltage compatible transistor in these technologies is to form an extended drain region by the use of existing deep wells in the standard CMOS process. This device is referred to as drain-extended MOS (DeMOS)—as depicted in Fig. 1(c) and (d)—and is discussed in detail in [1], [2]. Circuits based on DeMOS devices can be found in power management units, level shifters, high-voltage drivers and RF power amplifiers, working up to voltages of 10–20 volts.

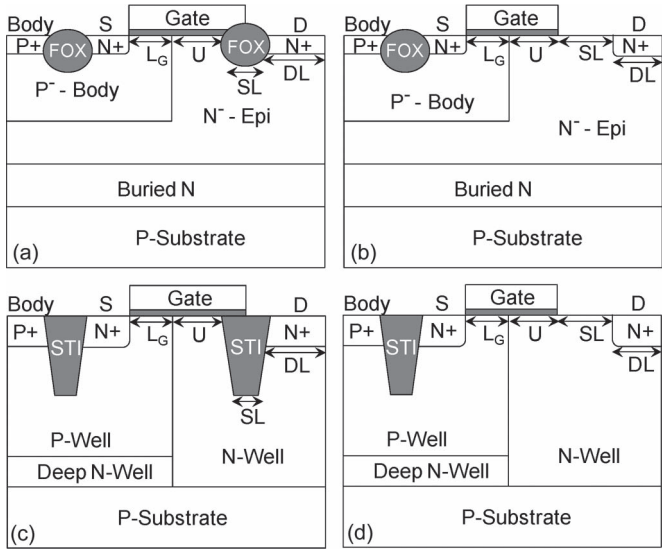

Fig. 1. Laterally diffused MOS (LDMOS) and Drain-extended MOS (DeMOS) device types implemented in different technologies: (a) and (b) shows cross section of LDMOS devices, with and without field isolation (FOX) inside the drift region; whereas (c) and (d) shows cross-sectional view of DeMOS devices, with and without shallow trench isolation (STI) inside the drift region. Parameters U and SL—shown in the device's cross section—affect the breakdown voltage (V_{BD}) and device's ON-resistance (R_{ON}), L_G affects its analog/RF characteristics and DL has an impact on device's ESD behavior.

ESD is a critical stress event for semiconductor products, which can encounter during manufacturing, packaging or assembling processes [3]. In order to protect the functional devices from ESD stress, various ESD protection methods are in use. These schemes can be divided into two categories: the self-protecting and the nonself-protecting approaches. For the self-protecting scheme, the driver transistor exposed to ESD stress,

Manuscript received May 31, 2012; revised August 24, 2012; accepted September 12, 2012. Date of publication September 24, 2012; date of current version November 30, 2012.

The authors are with Intel Mobile Communications GmbH, 85622 Munich, Germany (e-mail: mayank.shrivastava@intel.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TDMR.2012.2220358

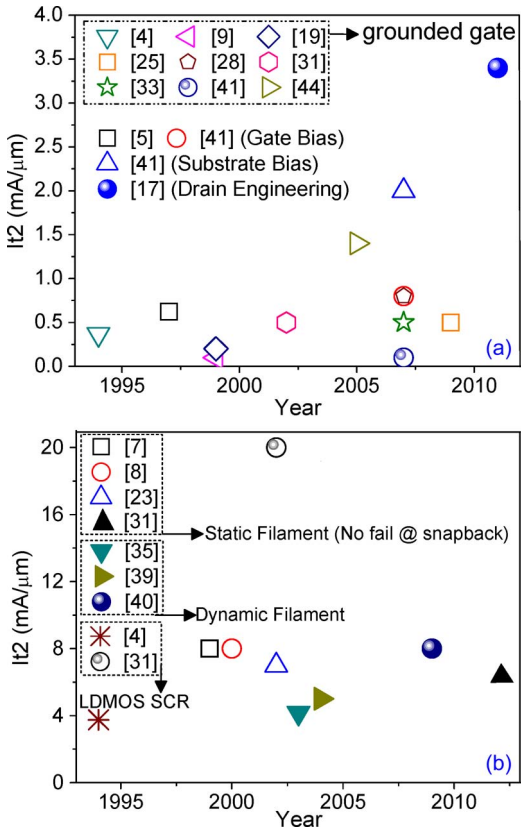

Fig. 2. It2 values reported in literature, published during last 2 decades. (a) LDMOS/DeMOS devices in grounded/biased gate and substrate pump configuration, which were failing right after the 1st snapback, (b) LDMOS/DeMOS devices in grounded gate configuration, which survived the 1st snapback and were found to have static or dynamic filaments, as well as LDMOS/DeMOS device with an embedded SCR.

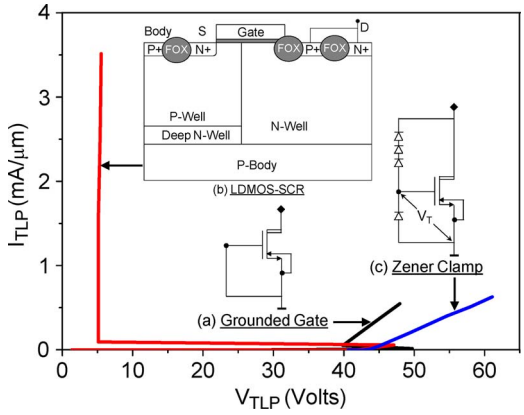

Fig. 3. 100-ns pulse I–V characteristics of LDMOS (a) under grounded gate configuration, (b) with embedded SCR (LDMOS-SCR) and (c) as gate-triggered clamp designed using Zener diodes [4], [5].

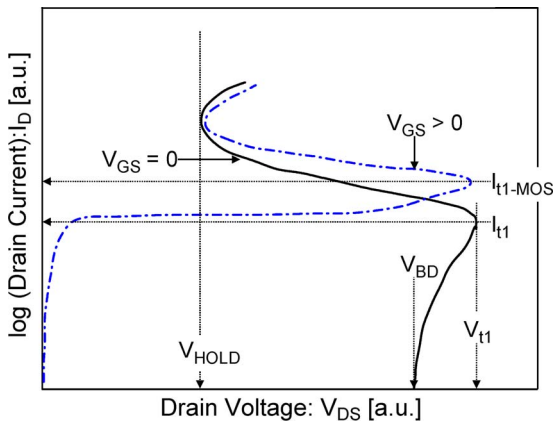

Fig. 4. Definition of characteristic quantities in a typical I–V curve of grounded gate and gate biased LDMOS devices, extracted from TLP measurements [7], [8]. Here, $V_{\rm HOLD}$ is the holding voltage of low-resistance state of the I–V characteristics, junction breakdown voltage is represented as $V_{\rm BD}$, trigger voltage or onset of snapback as V_{t1}, impact ionization trigger current as I_{t1} and MOS trigger current as $I_{t1-{\rm MOS}}$.

is designed to withstand an ESD discharge event. For example, driver devices of large gate width can be used to shunt 1–2 A of electrostatic discharge current. However, if drivers are of low or medium sizes (without dummy driver cells), nonself-protecting schemes need to be implemented; in this case specific ESD protection devices have to be added to the driver cell [3].

ESD behavior of LDMOS/DeMOS devices have been investigated over a period of more than two decades. In many cases extremely low failure current (It2) of these devices have been observed under ESD stress (Fig. 2). The very first ESD investigation on LDMOS device was reported in [4], where the ESD-related device damage was found to occur at the N+ drain (Si) and FOX interface. Moreover, the ESD behavior was found to be nonscalable in grounded gate configuration, i.e., It2 does not increase with increasing transistor width. The quasi-steady I–V behavior of grounded gate LDMOS device extracted from 100-ns transmission line pulsing method (TLP) is shown in Fig. 3 [4]. It shows an extremely low It2 value (0.5 mA/μm) of n-LDMOS devices. In order to design efficient ESD protection clamps using such devices, two approaches have been realized—i) LDMOS-SCRs [4] and ii) gate-triggered clamps [5]. The LDMOS-SCR consists of a parasitic SCR, which is implemented by inserting P^+ diffusion into the drift (N-epi/N-well) region of LDMOS device, as shown in the inset of Fig. 3. The basic principle of LDMOS-SCR is as follows: as soon as the drain-to-body potential of LDMOS device exceeds its junction breakdown threshold, the SCR path triggers and eventually avoids the catastrophic failure of the LDMOS device. It was found that ESD performance improved from less than 2 kV to greater than 6 kV just by incorporating an SCR without causing any adverse impact on the transistor or its circuit performance [4]. ESD robust nature of LDMOS-SCR was later validated by testing the same under an inductive load [6]. In [5] channel heating in LDMOS device, under sub-100-ns scale stress, was found minimal. This allows designing efficient protection clamps in MOS mode [5]. For example, a device with gate width of 2400 μm was used along with a Zener diode at gate, which turns on the MOS and provides $\sim$1.5 A ($>$ 2 KV) of MOS current under ESD stress condition (Fig. 3).

II. Device Behavior Under ESD Stress

Both DeMOS and LDMOS exhibit a similar characteristic I–V behavior. Fig. 4 shows the high breakdown voltage of the grounded gate devices, which is followed by a distinct kink in the I–V characteristic limited by the triggering voltage V_{t1}

which is, in difference to NMOS devices, largely independent[1] of a gate bias. After passing the triggering voltage, a strong snapback occurs leading to low holding voltages. Most of the devices were found to fail right after the snapback. Commonly this is attributed to nonuniform turn-on behavior [4], [7]. In some cases, gate bias influences the parasitic turn-on behavior and eventually device failure threshold. [7], [8] report that trigger current and failure threshold increase with small gate bias, while V_{t1} largely stays the same, unlike to ggNMOS devices. An empirical relation for the holding voltage of LDMOS device was formulated in [8] in order to extend the MOS I–V relation. The holding voltage was found to be proportional to breakdown voltage V_{BD} and inversely proportional to bipolar gain (β) and impact ionization multiplication factor (M) of the underlying bipolar transistor and its extended drain–body junction

$$V_{\mathrm{Hold}} \propto \frac{V_{\mathrm{BD}}}{\sqrt[n]{1+\beta/k}} \tag{1}$$

where $k = \beta \cdot (M-1) \geq 1$ and $M = 1/(1-(V_{\mathrm{DS}}/V_{\mathrm{BD}}))$.

Exponent n represents an empirical fitting factor. The physical mechanism described by this relation is a bipolar driven snapback which is relevant for devices with short drift region and higher doping herein. V_{t1} and V_{Hold} were found to be closely related [9]. As V_{t1} of LDMOS/DeMOS device increases, V_{Hold} shifts by the same factor when filament width remains unchanged. This can be achieved by increasing/decreasing drain-to-poly spacing (SL) for LDMOS or DeMOS devices without FOX or STI isolation [Fig. 1(a) and (b)]. While V_{t1} and V_{Hold} show a simultaneous increase/decrease, It2 value was not found to have any dependency on V_{t1} or V_{Hold}. Also, It2 did not scale with device width, which further validated previous predictions [4], [7].

The strong snapback to a low-holding-voltage state of structures with large and lowly doped drain extension was attributed to electric field localization at the n+/n- diffused junction [7]. Field localization is a combined effect of high avalanche generation ($M \to \infty$ or $V_{\mathrm{DS}} > V_{\mathrm{BD}}$) at the n+/n- junction and charge modulation of the lightly doped extended drain region under high-current conditions [9]. In case of n-DeMOS, free carriers modulate the lightly n-doped drain extension region. This effect shifts the peak electrical field and confines it in a small region close to n+/n- junction (Fig. 5), while the peak value of electric field increases.

The charge modulation of the lowly doped drain extension region and localization of peak electric field at the highly doped n-type collector is also referred to as "Kirk effect" [10], which was investigated in more detail by TCAD simulations [11]. The onset of Kirk effect can approximately be described by

$$J_{\mathrm{KIRK}} = q \cdot N_{\mathrm{DRIFT}} \cdot v_{\mathrm{SAT}} \tag{2}$$

where J_{KIRK} is the majority carrier current density required for the onset of charge modulation, q is charge, N_{DRIFT} is the net doping density inside the lowly doped drift region (N-epi/N-well) and v_{SAT} is the majority carrier saturation velocity.

[1]Only valid when $I_{\mathrm{KIRK}} > I_{D-\mathrm{sat}}$, where I_{KIRK} is the current required for the onset of space charge modulation and $I_{D-\mathrm{sat}}$ is the saturation drain current. A detailed discussion on the influence of gate bias is presented in Section IV.

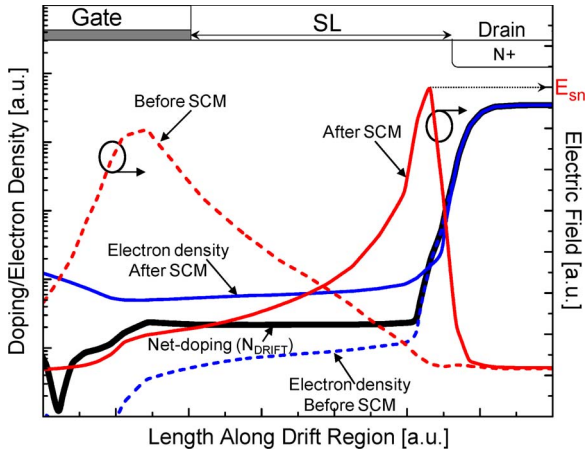

Fig. 5. Electron density (blue) and electric field (red) at the drain extension along cut line close to silicon surface. Shift in the electric field profile from well junction under the gate toward N^+ drain occurs during space-charge modulation (SCM). Space-charge modulation is attributed to high majority carrier density exceeding the net doping density (black).

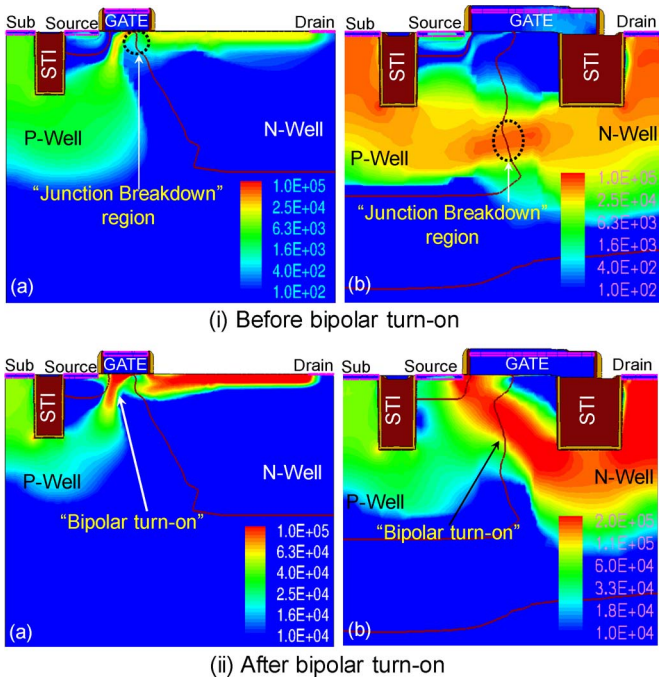

Fig. 6. Total current density [A/cm^2] contours inside the device (a) without and (b) with STI isolation in the drift region, representing the nature of current flow (i) before and (ii) after onset of parasitic bipolar turn-on. Shift of maximum current from substrate to source contact of device proves the change in nature of current flow from junction breakdown (i) to bipolar (ii). Note that the onset of parasitic bipolar in both the cases was before filament formation or fail.

The three relevant physical mechanisms, which determine the behavior of LDMOS or DeMOS under ESD conditions, i.e., bipolar turn-on, impact ionization and charge modulation, are investigated in more detail in the following sections using 2-D and 3-D TCAD simulation.

III. Device Physics and Filament Formation

In order to unify the physical picture, demonstration of different physical effects in the DeMOS device is shown for both types of devices, i.e., device without [Fig. 6(a)] and with [Fig. 6(b)] oxide isolation in the drift region [12]–[15].

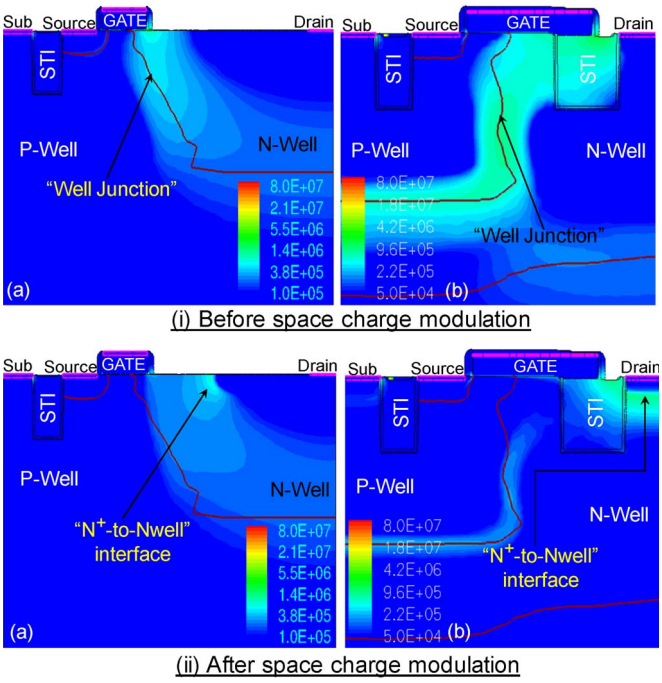

Fig. 7. Electric field [V/cm] contours inside the device (a) without and (b) with STI isolation in the drift region, representing the nature of electric field distribution and its localization (i) before and (ii) after space-charge modulation. The figures show that before space-charge modulation, peak electric field was localized at N-well-to-P-well junction, which shifts next to N^+ drain-to-N-well interface after space-charge modulation.

A. Junction Breakdown

Fig. 6(i) depicts current density contours at a low drain current (10 μA/μm), which shows that the initial flow of current through DeMOS devices (both without and with isolation in the drift region) is due to P-well-to-N-well junction breakdown. Similar current levels are seen at drain (collector of NPN) terminal and substrate (base of NPN) contact, which indeed proves the dominance of junction breakdown for conduction at small drain currents. An order of magnitude lower current through source (emitter of NPN) terminal in these contours show that the parasitic bipolar was not triggered yet.

B. Bipolar Turn-on

Fig. 6(ii) shows turn-on of parasitic bipolar at moderate currents (0.1–0.2 mA/μm) where most of the current was collected at the source contact (emitter of parasitic NPN). Note the difference among the two devices, i.e., a) without and b) with oxide isolation. In the structure without STI inside the drift region (a), current or majority carriers were mostly confined close to the silicon surface; while the current path bends deeply into the drift region when STI is present (b). The difference in the respective majority carrier paths leads to smaller width of current tube in (a) as compared to (b) within the cross-sectional plane of the respective devices, which eventually gives rise to a higher carrier density in (a) as compared to (b), for a given drain current.

C. Space-Charge Modulation and Kirk Effect

Fig. 7 shows the electric field distribution across the device i) before and ii) after space-charge modulation, respectively.

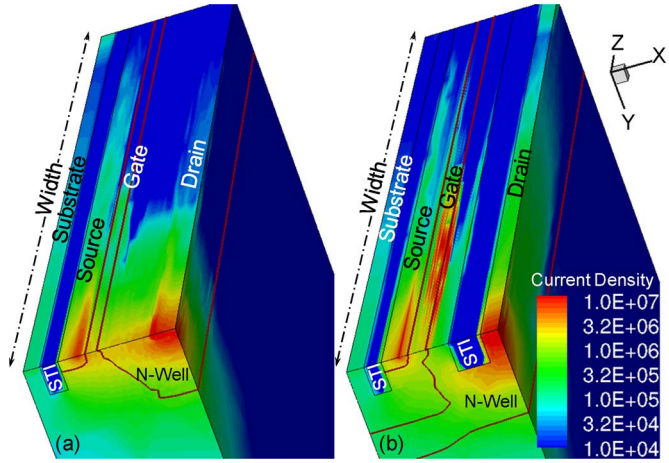

Fig. 8. Three-dimensional current density [A/cm^2] contours representing the formation of current filament after space-charge modulation.

Fig. 7(i) shows peak electric field located at well junction, which shifts at N+ drain-to-N-well junction after space-charge modulation, which is evident from Fig. 7(ii). Due to the fact presented above, device without isolation (having higher carrier density) exhibits an earlier space-charge modulation when compared to the same device with STI isolation and the same drift region doping (N-well/N-epi). While the peak electric field is located near surface for structure (a), it peaks right underneath the n+ diffusion region in structure (b), which is again related to the presence or absence of STI isolation.

D. Filament Formation and Fail

Filament formation right at snapback is widely reported. This can be destructive or nondestructive. Destructive filament formation results in very strong localization of current, which leads to extremely high current densities and local heating. Thus, one of the critical issues with filamentation is to build a qualitative understanding of its formation. The mechanism of filament formation heavily depends on the device structure and doping profiles. For DeMOS with large drain extension it has been proven that the filament formation is driven by the fall of majority carrier mobility under high electric fields at N+ drain-to-N-well junction, which occurs after space-charge modulation [16]. Probing the physical parameters like current density and lattice temperature in the zy plane an abrupt change to a localized current path (i.e., filament) can be seen when taking into account high field mobility degradation (Fig. 8). This, however, was not visible when high field mobility degradation was not considered in 3-D TCAD simulation models [17]. The physical picture of the formation of a current filament or an electrical instability can be described as follows: the rise in electric field (E) to extremely high ($E \gg 1 \times 10^5$ V/cm) values next to N+ drain diffusion after the space-charge modulation in the drain extension region leads to a strong decrease in carrier mobility μ ($E \uparrow \rightarrow \mu \downarrow$). The extremely degraded carrier mobility restricts the flow of current through the device. To overcome this problem, the system forms a current filament of very high charge carrier density. A rise in carrier density n screens the rising electrical field inside the filament, which improves mobility [17], [18]. These factors together make the formation

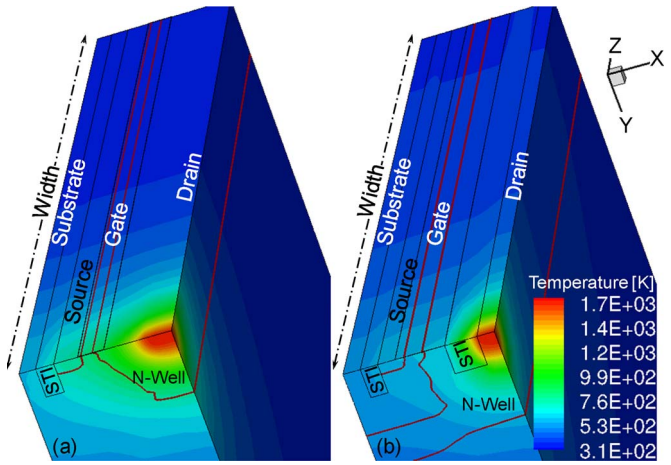

Fig. 9. Lattice temperature distribution across the 3-D device structure for both the devices (a) without and (b) with oxide isolation inside the drift region. In both the cases the hot spot was located next to N^+ drain-to-N-well interface.

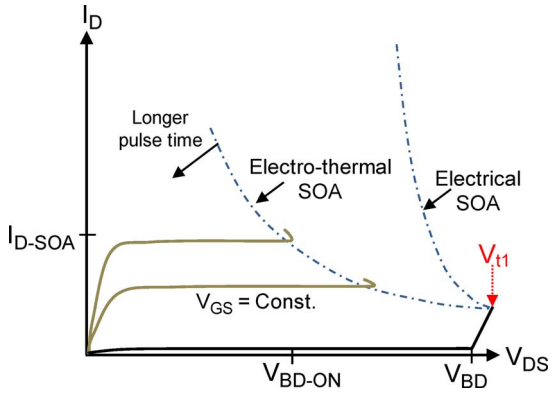

Fig. 10. Boundaries defining the electrical and electrothermal safe operating areas. $\mathrm{V_{BD}}$ and $\mathrm{V_{BD-ON}}$ is the drain-to-body junction breakdown voltage in off state and on state, respectively, V_{t1} represents onset of snapback, $\mathrm{I}_{D-\mathrm{SOA}}$ is the maximum allowed drain current defined by electrothermal SOA, i.e., under functional or operating conditions.

of a filament favorable. The process can be summarized as: $\mathrm{E}\uparrow\rightarrow \mu\downarrow\rightarrow$ filament formation $\rightarrow \mathrm{n}\uparrow\rightarrow \mathrm{E}\downarrow\rightarrow \mu$ recovers.

Soon after this localization or filamentation, an instant rise of temperature to a very high value can be detected, as shown in Fig. 9, which finally cause the fail [17]. It is worth to emphasize that the bipolar turn-on does not drive any strong filament formation in DeMOS devices. Also, a bipolar driven snapback is hardly seen in this state. In contrary, subsequent space modulation and related filament formation leads to the very sharp and deep snapback seen in LDMOS/DeMOS TLP I–V characteristics.

IV. Safe Operating Area

For device optimization the concept of Safe Operating Area (SOA) under pulsed stress conditions is important, which describes the acceptable region for safe and reliable operation as a function of pulse voltage, current and width. Normal operation defines the minimum form of SOA required for the qualification of LDMOS/DeMOS devices. Fig. 10 shows the boundaries defining the electrical and electrothermal safe operating areas for a LDMOS/DeMOS device [19], [20] and demonstrates the general features of an electrical and electrothermal SOA.

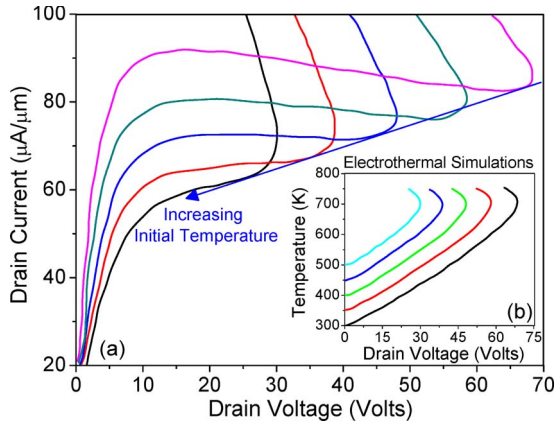

Fig. 11. (a) Snapback characteristics and (b) temperature rise of LDMOS device for various ambient temperatures. As the starting junction temperature increases the snapback voltage decreases systematically by a rate of 0.18 V/K [21].

Constant $\mathrm{V_{GS}}$ curve shows onset of snapback due to electrothermal instability which occurs at a high drain potential (electric field) and a high channel current. The regime below the snapback is referred to as safe operating area under normal operating conditions. The maximum achievable current and voltage compliant with electrical and electrothermal SOA decrease with increasing ambient temperature, which is attributed to an accelerated instability at higher temperatures. This behavior is also described in Fig. 11 as a shift of electrical SOA boundary with increasing temperature [21]. Fig. 11 shows that snapback always takes place as soon as the device reaches a certain lattice temperature, which was indeed defined as the limit for electrothermal SOA. Note that electrothermal SOA become relevant for longer pulse widths only.

On the other hand, electrical SOA is relevant for very short pulse widths, which do not lead to significant joule heating before reaching extremely high current densities. The electrical SOA boundary corresponds to the onset of instability when device is stressed beyond avalanche breakdown. A method to estimate the electrical SOA limit of any LDMOS transistor was described in [19]. It was reported that the base widening at the onset of space-charge modulation limits the safe operating area of LDMOS devices. Space-charge modulation leads to a triangular-shaped electric field profile (Fig. 5), which means that, in addition to the "limiting current density" $q \cdot N_{\mathrm{DRIFT}} \cdot v_{\mathrm{SAT}}$, as described in (2), there is also a space-charge-limited current component. This increases as the length of the space-charge region decreases. The critical current density J_{sn} is described more precisely in (3), where $\mathrm{E_{sn}}$ is the peak electric field inside the space-charge region (see Fig. 5) and V_{t1} is the drain potential at the onset of snapback for each I–V curve at given $\mathrm{V_{GS}}$ value [19]

$$J_{\mathrm{sn}} = \frac{E_{\mathrm{sn}}^2 \cdot \varepsilon \cdot v_{\mathrm{SAT}}}{2 \cdot V_{t1}} + q \cdot V_{\mathrm{DRIFT}} \cdot v_{\mathrm{SAT}}. \tag{3}$$

Investigations presented in [22] have shown improvement of electrical SOA by means of layout and doping optimization in the source/body region of LDMOS transistor. Circular cell/devices were found to have improved electrical SOA

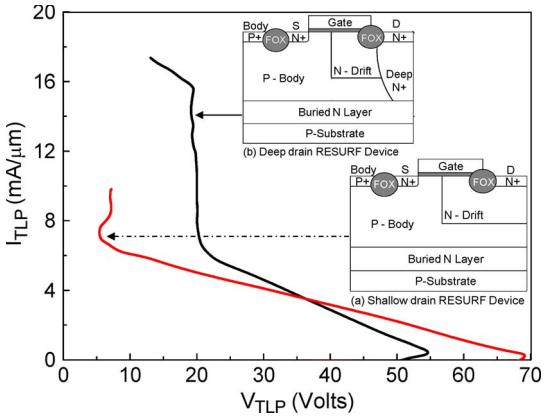

Fig. 12. 100-ns TLP characteristics of (a) shallow and (b) deep drain LDMOS device [23], [24].

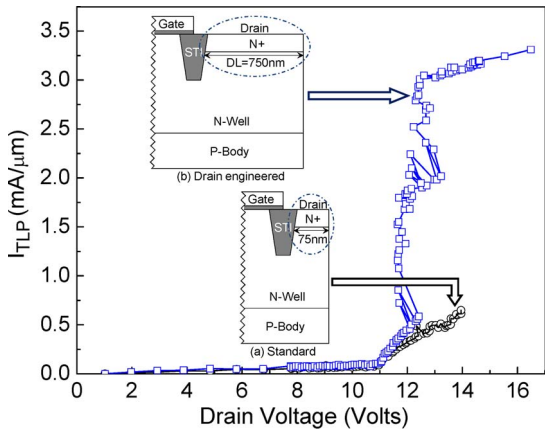

Fig. 13. 100-ns TLP characteristics of drain-extended MOS device with (a) DL = 75 nm and (b) DL = 750 nm [17].

boundaries when compared with a stripe like cell/device geometry. However, this was achieved with a slight penalty of R_{ON}, when compared for MOS performance.

V. Optimization Schemes

This section summarizes various optimization techniques, which are capable to improve ESD robustness of LDMOS/DeMOS devices.

A. Drain Engineering

Engineering of N^+ drain–N^- drift region plays an essential role in the ESD behavior of LDMOS/DeMOS devices. Fig. 12 shows a conventional shallow drain LDMOS device with large snapback and low It2. TLP characteristic improves when a deep drain diffusion profile in the drift region of LDMOS device is used. Incorporating a deep drain diffusion profile improved the It2 value of shallow drain LDMOS device from 8 mA/μm ($V_H = 7$ V) to 16 mA/μm ($V_H = 20$ V) [23], [24]. The gain, however, was at the cost of lower V_{t1} as well as lower V_{BD}. The improvement is attributed to reduced electric field at the drain diffusion after space-charge modulation, which eventually reduces the overall power dissipation ($J \cdot E$) [23]. Such a profile also helped in reducing any leakage degradation before the hard fail of the device. A similar proposal was made in [12], which had an N-Well sinker in order to avoid early charge modulation and a STI region near the drain diffusion. This caused a bend of the current path deep into the drift region, which improved the ESD failure voltage (V_{t2}) by a factor of $\sim 2\times$ and the failure current threshold (It2) by a factor of $\sim 5\times$. The proposed modification has been shown not to degrade the R_{ON} v/s V_{BD} performance and does not lead to extra processing cost. Investigations presented in [12] show that the critical current density for the onset of space-charge modulation was increased when using a deep N-sinker, which is due to a $\sim 5\times$ higher net doping of N-sinker near N^+ drain. This indeed shifted the onset of destructive filament formation to a $\sim 5\times$ higher drain current.

In other investigations on DeMOS device with STI in the drift region, an improvement in failure threshold was found by

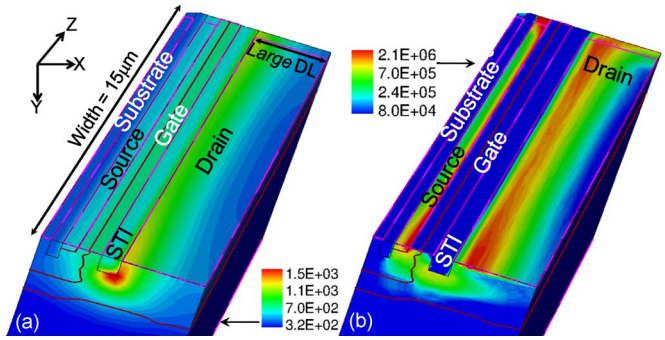

Fig. 14. Three-dimensional distribution of (a) current density [A/cm^2] and (b) lattice temperature [K] in the drain-extended MOS device with increased DL (750 nm) at a $\sim 5\times$ higher TLP current (=50 mA) compared to the It2 value of standard device (DL = 75 nm) [17], [26].

increasing the N^+ drain diffusion length DL [13], [25], [26]. Increasing the drain diffusion area leads to a lower current density in the N-well (or N-drift) region underneath the drain diffusion. This also shifts the onset of space-charge modulation to higher current. Fig. 13 shows that the device with larger DL (DL = 750 nm) exhibits $\sim$5 X improvement in the failure current compared to a device with smaller DL (DL = 75 nm). The It2 value amounts to 3.3 mA/μm which is the highest reported It2 value for grounded gate DeMOS devices (Fig. 2). Moreover, triggering of second finger of the double-finger structure is clearly observed at $I_{TLP} = 1.6$ mA/μm, which shows that this modification will lead to a linear rise in It2 value with increasing number of fingers. Fig. 14 shows significantly widened current filament in case of a higher DL. The filament is extending over the full finger width and has a uniform heating up to very high temperature levels. This indicates full exploitation of intrinsic thermal failure threshold of device [27]. Moreover, by the increase in DL ON-resistance of the STI-type drain-extended MOS device was found to be reduced [17]. It is worth pointing out that the extended drain diffusion region with increased DL is fully silicided and a maximum number of contacts were used. This also indicates that suppression of current filamentation is not due to so-called ballasting resistance—unlike in the silicide blocked drain diffusion of ggNMOS devices.

In another work [28], it was reported that increasing the background doping of the extended drain region (i.e., drift region) can improve the ESD robustness of drain-extended MOS device. However, increasing the drain extension doping reduces the breakdown voltage. The underlying physics of the reported improvement was given in [29]. The increase of the background doping shifts the onset of space-charge modulation toward higher current densities, which improves the onset of snapback and eventually leads to higher It2. [29] also shows that use of graded drain-to-drift region doping profile improves ESD robustness of DeMOS devices without affecting the device's breakdown voltage and ON-resistance.

Another approach of drain engineering was proposed in [30], where local drain diffusion islands (along the width) were used inside the N-well/N-Epi, instead of stripe like drain diffusion. This approach was found to increase the It2 value of DeMOS device, however at the cost of slightly increased $\mathrm{R_{ON}}$. Recently, a dramatic improvement in the ESD behavior of DeMOS/LDMOS was achieved using selective silicide blocking of the drain diffusion region [31]. An improved ESD robustness was achieved with a minimal impact on $\mathrm{R_{ON}}$, however, at a cost of 10% drop in $\mathrm{I}_{D-\mathrm{sat}}$.

B. Embedded SCR

Beyond early implementations of parasitic SCR inside the LDMOS device [4]–[6], there have been several recent investigations on SCR-LDMOS device. E.g. a 40-V LDMOS device, which was found to be seriously prone to ESD fail, was improved by inserting a P+ strap in N+/N-well drain region, modifying this to a SCR-LDMOS [32]. However, this SCR-LDMOS device was seen to have a nonuniform current distribution in multifingers configuration due to a varying substrate resistance with respect to finger position. In order to improve the current uniformity, a modified ESCR-LDMOS structure was proposed, which consisted of local $\mathrm{P^+}$ strap between $\mathrm{N^+}$ source regions and achieved $2\times$ improvements in It2 compared to the base SCR-LDMOS device. Fig. 15 compares the TLP characteristics of SCR-LDMOS and ESCR-LDMOS showing that the $\mathrm{P^+}$ strap between $\mathrm{N^+}$ source region improves the It2 values by a factor of 2 [32].

Further work published in [33] has proposed several different approaches for a robust design of an ESD clamp required for LDMOS/DeMOS drivers. In the first approach N-well region of LDMOS device includes a P+ region, which forms a parasitic SCR in conjunction with LDMOS device, as shown in Fig. 16(a). In Fig. 16(b) a LDMOS device is placed in next to a SCR device with slightly smaller trigger voltage. The second approach resulted in a more than $2\times$ ESD robustness increase compared to the first. However, additional area was needed. Moreover, it was found that when $\mathrm{N^+}$ in N-well (drain diffusion) was placed next to the FOX/STI isolation (between $\mathrm{P^+}$ in N-well and STI), device was highly prone to increased leakage and reduced V_{t1} in case of multizapping [34]. This degradation was reduced when the $\mathrm{P^+}$ in N-well (Anode terminal of SCR connected to the pad) was placed between FOX/STI isolation and $\mathrm{N^+}$ diffusion in N-well.

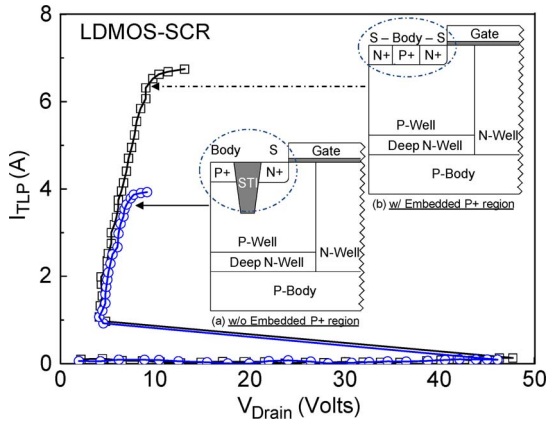

Fig. 15. 100-ns TLP characteristics of SCR-LDMOS device (a) without P+ embedded region (SCR-LDMOS) and (b) with P+ embedded region inside N+ source (ESCR-LDMOS). Both the devices had same gate width [32].

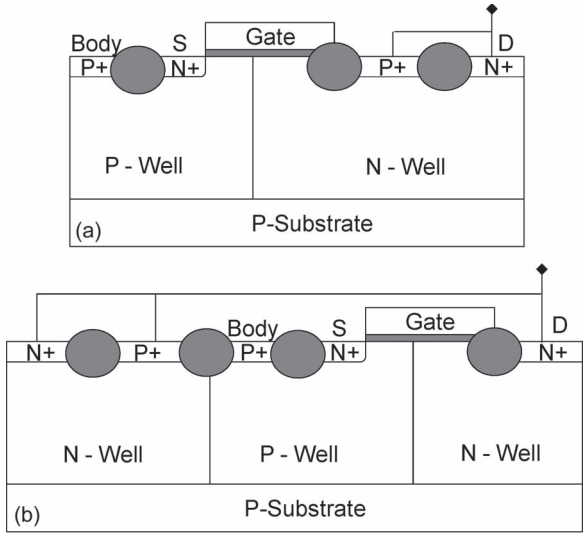

Fig. 16. (a) LDMOS device with $\mathrm{P^+}$ diffusion within the N-well drift region electrically connected to $\mathrm{N^+}$ drain contact and forms a parasitic SCR. (b) LDMOS device with a SCR device next to it, which protects the LDMOS device from ESD fail [33].

C. Dynamic Filaments

Most of LDMOS/DeMOS device fails are due to an early filament formation and associated self-heating inside the static filament. Changing the nature of filament from static to dynamic (i.e., moving/spreading along the width) will mitigate this effect. This has been proposed for the first time in [35]. Dynamic filaments were predicted to improve It2 value of LDMOS device by impeding the significant self-heating right after filament formation. An analytic model for the speed of filament motion was derived in [35], where filament velocity (v) was found to be proportional to mobility of majority carriers in the base of parasitic bipolar (μ) and inversely proportional to length of the base region of parasitic bipolar (t_b)

$$v \propto \frac{\mu}{t_b}. \tag{4}$$

Movement of current filaments was first demonstrated through experiments in [36], [37], for a vertical DMOS device in a 90-V SPT. This was studied under snapback conditions

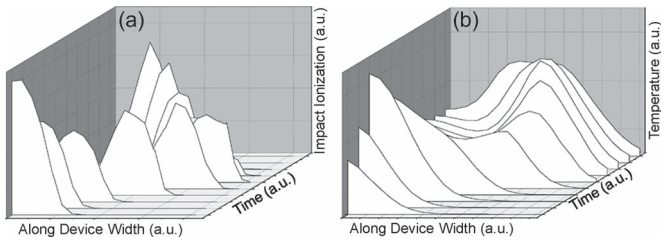

Fig. 17. (a) Impact ionization and (b) temperature profile along the width of device at different times during a single stress pulse [36], [37].

using transient interferometric mapping tool [38]. The study reports that the hot spot region at the drain diffusion or buried layer associated with the filament can move along the width of the device. Movement of current filament was attributed to reduced avalanche generation rate inside the filament (hot region) compared to its surrounding at lower temperature, which favors the shift of the filament to cooler regions nearby. This behavior is depicted in Fig. 17, which shows filament motion across the device width.

Depending on the DMOS topology, two types of motion were seen—(a) motion along the body diffusion of vertical DMOS device and (b) motion from one cell to a neighboring one in a multicell device configuration.

Detailed electrical and optical investigations of these moving filaments were performed and a motion of hot spots along the N-buried layer was found [39]. It2 value was found to be dependent on the drift region doping, which influences the length of vertical current flux tube close to source region. It was found that a larger substrate current enhances filament motion. Recently the filament movement was investigated in detail for a lateral DeMOS structure with STI inside the drift region as well [Fig. 1(c)] in [40]. While in previous works [36]–[39], filament motion was attributed to reduced avalanche generation due to heating inside the filament, this recent study has found additional requirements, which are essential for filament motion: i.e., i) occurrence of space-charge modulation leading to filament formation and ii) fast bipolar turn-on compared to the rate of increase in lattice temperature during the filament formation. Furthermore, it was indicated that filament remains in continuous motion if the device width is sufficiently large. The time for a back and forth motion is directly proportional to the width of the device. The underlying physics of filament motion is the same for vertical and lateral LDMOS/DeMOS device topologies.

D. Biasing Schemes and Source Engineering

To overcome the weakness of the grounded gate DeMOS device various biasing schemes have been evaluated in literature. Fig. 18 shows TLP characteristics and respective It2 values of DeNMOS device investigated under various configurations, i.e., gate-grounded, butted substrate, gate bias and substrate bias [41]. A maximum It2 of 1.9 mA/μm was achieved under substrate biasing scheme of a so-called DI-DeNMOS, which is based on an N-well diode in series with DeNMOS, pumping holes into the base of the DeNMOS. Impact of body injection (substrate pump) and gate biasing technique for LDMOS device

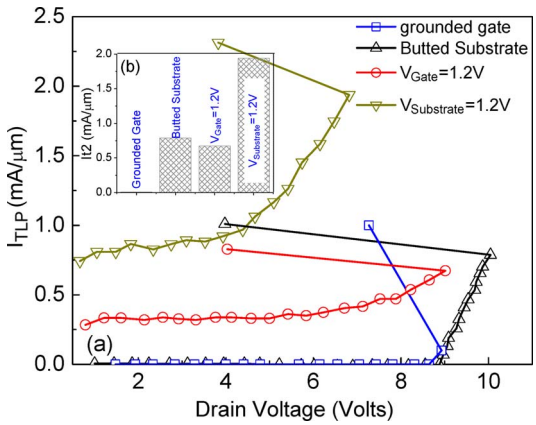

Fig. 18. (a) 100-ns TLP characteristics of DeMOS device (without STI isolation in the drift region) under various bias schemes and with source engineering (butted substrate), (b) Comparison of It2 values extracted from TLP measurements under various biasing schemes [41].

concerning V_{t1} reduction and It2 improvement is discussed in [42], [43]. The area overhead associated with the pump or trigger circuit actually leads to no improvement in terms of It2/area. However, when holding voltage is a concern (low holding voltage using high-voltage device for high-voltage application), a combination of gate and substrate biasing technique will be useful.

In literature no impact of gate biasing on the It2 value is shown for devices with isolation oxide in the drift region [44], while improvement from gate biasing on the It2 value is reported for devices without isolation oxide inside the drift region. This initially unexpected behavior can be explained as follows. In the case of device without isolation oxide, majority or drift carriers are confined close to the Si surface. However, if an isolation oxide trench is used current conduction takes place deeper inside the device. This behavior is evident from Fig. 8. Due to the fact that gate electric fields can only control the Si surface (gate oxide-to-Si interface) and have no influence on carriers flowing deep in the body and drain extension region, gate biasing scheme has no impact on these devices.

Another approach of source engineering was proposed in [30], where P+ substrate islands were embedded into the source N+ strap (along the width direction). In addition to the P+ islands, work in [45] recently presented additional improvements by silicide blocking of source N+ diffusion. These approaches were found to increase the It2 value of DeMOS device explained by a weaker bipolar gain, however with slightly increased R_{ON}.

VI. CDM Behavior

Unlike to HBM event ($\sim$100 ns), CDM is a very fast ($\leq$ 1 ns) event, which is often modeled by using very fast TLP (VF-TLP) test. So far there have been very few investigations on the CDM/VF-TLP behavior of LDMOS or DeMOS devices [26], [46], [47]. On one hand [26], [46] report higher It2 values (compared to 100-ns TLP) in CDM domain; however, on the other hand, work presented in [47] shows that CDM/VF-TLP leads to an early fail when compared to longer pulse widths.

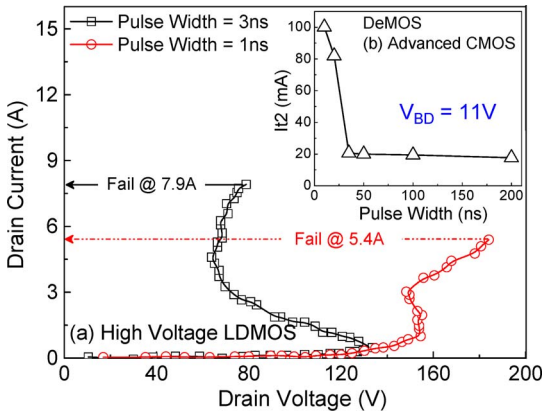

Fig. 19. CDM evaluation of LDMOS and DeMOS devices by short-pulse TLP experiments (a) VF-TLP behavior of an 80-V LDMOS device [47] and (b) It2 of a DeMOS device (with STI isolation) as a function of pulse width [17].

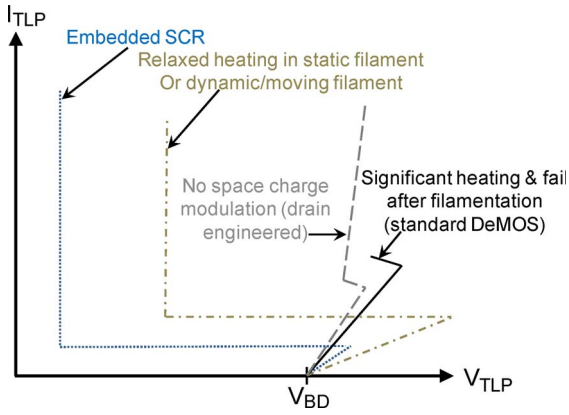

Fig. 20. Overview of I–V characteristics of different ESD optimized LDMOS/DeMOS device type including the underlying physical effect.

For understanding the VF-TLP behavior of LDMOS/DeMOS devices, one should note that the correlation between It2 value and TLP pulse width is only valid for devices which follow power law [3], for example: ggNMOS, SCRs and diodes. Whereas, the power law (and short time pulse) behavior of LDMOS/DeMOS devices is rather complex due to nonuniform conduction and early filament formation.

Fig. 19(a) depicts TLP behavior of a HV LDMOS device with 3-ns and 1-ns pulse width [47]. Figure shows that 3-ns pulse leads to a snapback attributed to the filament formation. A higher It2 value is detected compared 1-ns pulse, which does not show any snapback (attributed to lack of filament formation). This contradicts the usual power law considerations. This behavior can be explained as follows: LDMOS device under 3-ns stress forms a filament, as sufficient time is available for filament formation. It gets into a low-holding-voltage state, which protects the device from early gate oxide fail. On the other hand, at 1-ns pulse the device does not show any snapback/filamentary state (due to insufficient time available for filament formation). A high-holding-voltage state is sustained, which eventually leads to an early gate oxide breakdown.

Fig. 19(b) depicts It2 value (extracted for DeMOS device in an advanced CMOS node) as a function of pulse width [17]. The It2 value initially remains unchanged for decreasing pulse width; however, at 40-ns pulse width it suddenly improves. As in these structures the fail was of electrothermal nature, the suppression of filament formation at lower pulse width improved the failure threshold.

It is evident from these two cases that CDM like fails are determined by gate oxide failure level and holding voltage as a function of pulse time and drain current threshold required for filament formation. Thus, CDM behavior of LDMOS/DeMOS will strongly depend on the technology, device topology and design parameters.

VII. Outlook on Technology Scaling

Technology parameters like well doping, well depth isolation type (STI/FOX), isolation depths, presence/absence of N-buried layer, drain/source implant (or junction) depths and device design parameters like U, L_G, SL and DL (as shown in Fig. 1) have serious impact on the filamentary behavior and eventual ESD robustness of LDMOS/DeMOS devices. Since these parameters have a predefined trend with the technology scaling, advancement of semiconductor process will strongly affect the characteristics of these devices under an ESD stress. While DL is an adjustable layout parameter, it might become restricted to minimum values in very advanced CMOS technologies beyond sub-28-nm nodes, which will degrade It2 to very low values and make self-protection of drivers extremely difficult. A similar trend can be seen for gate overlap (U), while DeMOS devices are found to be rather insensitive against L_G and SL scaling.

The well implantation details can vary significantly from technology to technology with major impact on ESD performance of DEMOS and LDMOS devices. A lower drift region (N-well for DeNMOS in advanced CMOS) doping leads to a higher junction breakdown voltage. However, it will reduce onset of space-charge modulation and filamentary snapback. Such an early filament formation in LDMOS/DeMOS devices—in most of the cases—leads to an immediate fail, which is due to excess heating inside the narrow filament. On the other hand, a device with lower drift region doping becomes ESD robust by incorporating drain diffusion (N+ implant for DeNMOS) with a higher implant depth, which gives rise to a graded drain-to-drift doping profile. A graded profile suppresses the formation of filament, which mitigates excess self-heating. This eventually protects device from a catastrophic fail at higher currents under snapback (space-charge modulation) conditions, as shown in Fig. 20. In addition to this, lower substrate/channel doping helps further by changing the filamentary nature from static (excess heating) to dynamic/moving (relaxed/balanced heating). Furthermore, increasing the drift region junction depth improves breakdown as well as trigger voltage and ESD robustness of these devices by spreading majority carriers deep into the drift region, which delays the onset of space-charge modulation. Since these trends are opposite to the technology scaling, ESD robustness of these device will be a challenge in sub-28-nm node technologies.

Finally, moving toward FinFET technologies will bring even more restrictions in the design of drain-extended devices due to the narrow fins and the weak coupling from fin-to-fin via the substrate.

VIII. Summary

This paper provides an overview on the state-of-art of ESD robust DeMOS/LDMOS devices and the underlying physical mechanisms often leading to early fails. Extremely low failure current (It2) and missing width scaling of these devices has consistently been reported during the last two decades, which has challenged the design of ESD robust I/O drivers and other SoC modules requiring high-voltage handling capabilities. Previously a number of investigations explain this early failure and limitation of the safe operating area by bipolar driven instability. However, it was discovered recently that LDMOS devices fail due to an excess heating right after filament formation, where the filament formation was attributed to an electrical instability. This electrical instability is a consequence of high field mobility degradation after space-charge modulation. However, devices can be prevented from failing right after space-charge modulation by spreading out the filament, using appropriate design and technology measures like careful source/drain engineering. Finally, avoiding space-charge modulation by drain engineering was discovered to be the most promising measure toward improved ESD robustness and safe operating area of DeMOS devices (i.e., rugged LDMOS/DeMOS) without sacrificing its intrinsic MOS performance or R_{ON}.

Acknowledgment

Authors would like to thank C. Duvvury, Texas Instruments, Dallas, TX for very helpful discussions on this topic.

References

[1] J. C. Mitros, C. Tsai, H. Shichijo, K. Kunz, A. Morton, D. Goodpaster, D. Mosher, and T. R. Efland, "High-voltage drain extended MOS transistors for 0.18-μm logic CMOS process," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1751–1755, Aug. 2001.

[2] P. Hower, S. Pendharkar, and J. Smith, "Integrating power devices into silicon roadmaps," *Proc. Inst. Elect. Eng.—Circuits, Devices Syst.*, vol. 153, no. 1, pp. 73–78, Feb. 2006.

[3] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, 2nd ed. Hoboken, NJ: Wiley, 2002.

[4] C. Duvvury, J. Rodriguez, C. Jones, and M. Smayling, "Device integration for ESD robustness of high voltage power MOSFETs," in *IEDM Tech. Dig.*, 1994, pp. 407–410.

[5] C. Duvvury, F. Carvajal, C. Jones, and D. Briggs, "Lateral DMOS design for ESD robustness," in *IEDM Tech. Dig.*, 1997, pp. 375–378.

[6] S. Pendharkar, R. Teggatz, J. Devore, J. Carpenter, T. Efland, and C. Tsai, "SCR-LDMOS—A novel LDMOS device with ESD robustness," in *Proc. ISPSD*, 2000, pp. 341–344.

[7] M. Mergens, W. Wilkening, S. Mettler, H. Wolf, A. Stricker, and W. Fichtner, "Analysis and compact modeling of lateral DMOS power devices under ESD stress conditions," in *Proc. EOSESD Symp.*, 1999, pp. 1–10.

[8] M. Mergens, W. Wilkening, S. Mettler, H. Wolf, A. Stricker, and W. Fichtner, "Analysis of lateral DMOS power devices under ESD stress conditions," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2128–2137, Nov. 2000.

[9] G. Boselli, S. Meeuwsen, T. Mouthaan, and F. Kuper, "Investigations on double-diffused MOS (DMOS) transistors under ESD zap conditions," in *Proc. Elect. Overstress/Electrostat. Discharge Symp.*, 1999, pp. 11–18.

[10] C. T. Kirk, "A theory of transistor cutoff frequency (f_T) falloff at high current densities," *IEEE Trans. Electron Devices*, vol. ED-9, no. 2, pp. 164–174, Mar. 1962.

[11] S. Pendharkar, P. Hower, R. Steinhoff, J. Brodsky, J. Devore, and B. Grose, "Using two-dimensional filament modeling to predict LDMOS and SCR-LDMOS behavior under high current ESD conditions," in *Proc. ISPSD*, 2001, pp. 161–164.

[12] M. Shrivastava, J. Schneider, M. S. Baghini, H. Gossner, and V. R. Rao, "On the failure mechanism and current instabilities in RESURF type DeNMOS device under ESD conditions," in *Proc. IEEE IRPS*, 2010, pp. 841–845.

[13] M. Shrivastava, H. Gossner, M. S. Baghini, and V. R. Rao, "Part I: On the low current parasitic bipolar and base push-out behavior of STI type DeNMOS device under ESD Conditions," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2235–2242, Sep. 2010.

[14] A. Chatterjee, M. Shrivastava, H. Gossner, S. Pendharkar, F. Brewer, and C. Duvvury, "An insight into the ESD behavior of the nanometer scale drain extended NMOS device—Part I: Turn-on behavior of the parasitic bipolar," *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 309–317, Feb. 2011.

[15] A. Chatterjee, M. Shrivastava, H. Gossner, S. Pendharkar, F. Brewer, and C. Duvvury, "An insight into ESD behavior of nanometer-scale drain extended NMOS (DENMOS) devices: Part II: (2D study-biasing and comparison with NMOS)," *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 318–326, Feb. 2011.

[16] M. Shrivastava, S. Bychikhin, D. Pogany, J. Schneider, M. S. Baghini, H. Gossner, E. Gornik, and V. R. Rao, "Filament study of STI type drain extended NMOS device using transient interferometric mapping," in *Proc. IEEE IEDM*, 2009, pp. 417–420.

[17] M. Shrivastava, C. Russ, H. Gossner, S. Bychikhin, D. Pogany, and E. Gornik, "ESD robust DeMOS devices in advanced CMOS technologies," in *Proc. EOS/ESD Symp.*, 2011, pp. 1–10.

[18] E. J. Yoffa, "Screening of hot-carrier relaxation in highly photo excited semiconductors," *Phys. Rev. B, Condens. Matter*, vol. 23, no. 4, pp. 1909–1919, Feb. 15, 1981.

[19] P. L. Hower, J. Lin, and S. Merchant, "Snapback and safe operating area of LDMOS transistors," in *IEDM Tech. Dig.*, 1999, pp. 193–196.

[20] P. Hower, C.-Y. Tsai, S. Merchant, T. Efland, S. Pendharkar, R. Steinhoff, and J. Brodsky, "Avalanche-induced thermal instability in LDMOS transistors," in *Proc. ISPSD*, 2001, pp. 153–156.

[21] Y. S. Chung and B. Baird, "Electrical-thermal coupling mechanism on operating limit of LDMOS transistor," in *IEDM Tech. Dig.*, 2000, pp. 83–86.

[22] A. Podgaynaya, D. Pogany, E. Gornik, and M. Stecher, "Improvement of the electrical safe operating area of a DMOS transistor during ESD events," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2009, pp. 437–442.

[23] V. Parthasarathy, V. Khemka, R. Zhu, J. Whitfield, A. Bose, and R. Ida, "A double RESURF LDMOS with drain profile engineering for improved ESD robustness," *IEEE Electron Device Lett.*, vol. 23, no. 4, pp. 212–214, Apr. 2002.

[24] V. Parthasarathy, V. Khemka, R. Zhu, J. Whitfield, R. Ida, and A. Bose, "Drain profile engineering of RESURF LDMOS devices for ESD ruggedness," in *Proc. IDPSD*, 2002, pp. 265–268.

[25] M. Shrivastava, J. Schneider, M. S. Baghini, H. Gossner, and V. R. Rao, "A new physical insight and 3D device modeling of STI type DENMOS device failure under ESD conditions," in *Proc. IEEE IRPS*, 2009, pp. 669–675.

[26] M. Shrivastava, H. Gossner, M. Shojaei Baghini, and V. Ramgopal Rao, "Part II: On the 3D filamentation and failure modeling of STI type DENMOS device under ESD conditions," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2243–2250, Sep. 2010.

[27] M. Shrivastava, H. Gossner, M. S. Baghini, and V. R. Rao, "On the transient behavior of various drain extended MOS devices under the ESD stress conditions," in *Proc. ISOCC*, 2010, pp. 264–267.

[28] K.-H. Kim, W.-J. Choi, and Y.-J. Seo, "Effects of background doping concentration on ESD protection properties of high voltage operation extended drain N-type MOSFET device," in *Proc. Int. Rel. Phys. Symp.*, 2007, pp. 334–341.

[29] M. Shrivastava, S. Bychikhin, D. Pogany, J. Schneider, M. S. Baghini, H. Gossner, E. Gornik, and V. R. Rao, "On the differences between 3D filamentation and failure of N and P type drain extended MOS devices under ESD condition," in *Proc. IEEE IRPS*, 2010, pp. 480–484.

[30] J.-H. Lee, H.-D. Su, C.-L. Chan, D. H. Yang, J. F. Chen, and K. M. Wu, "The influence of the layout on the ESD performance Of HV-LDMOS," in *Proc. ISPSD*, 2010, pp. 303–306.

[31] A. A. Salman, F. Farbiz, A. Appaswamy, H. Kunz, G. Boselli, and M. Dissegna, "Engineering optimal high current characteristics of high voltage DENMOS," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2012, pp. 3E.1.1–3E.1.6.

[32] J. H. Lee, J. R. Shih, C. S. Tang, K. C. Liu, Y. H. Wu, R. Y. Shiue, T. C. Ong, Y. K. Peng, and J. T. Yue, "Novel ESD protection structure with embedded SCR LDMOS for smart power technology," in *Proc. Int. Rel. Phys. Symp.*, 2002, pp. 156–161.

[33] A. J. Walker, S. T. Ward, and H. Puchner, "Novel robust high voltage ESD clamps for LDMOS protection," in *Proc. Int. Rel. Phys. Symp.*, 2007, pp. 596–597.
[34] A. J. Walker, H. Puchner, and S. P. Dhanraj, "High-voltage CMOS ESD and the safe operating area," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1753–1760, Aug. 2009.
[35] R. M. Steinhoff, J.-B. Huang, P. L. Hower, and J. S. Brodsky, "Current filament movement and silicon melting in an ESD-robust DENMOS transistor," in *Proc. EOSESD Symp.*, 2003, pp. 1–10.
[36] M. Denison, M. Blaho, D. Silber, J. Joos, N. Jensen, M. Stecher, V. Dubec, D. Pogony, and E. Gornik, "Hot spot dynamics in quasivertical DMOS under ESD stress," in *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, 2003, pp. 80–83.
[37] M. Denison, M. Blaho, P. Rodin, V. Dubec, D. Pogany, D. Silber, E. Gornik, and M. Stecher, "Moving current filaments in integrated DMOS transistors under short-duration current stress," *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1695–1703, Oct. 2004.
[38] M. Litzenberger, C. Fürböck, S. Bychikhin, D. Pogany, and E. Gornik, "Scanning heterodyne interferometer setup for the time resolved thermal and free carrier mapping in semiconductor devices," *IEEE Trans Instrum. Meas.*, vol. 54, no. 6, pp. 2438–2445, Dec. 2005.
[39] P. Moens, K. Reynders, S. Bychikhin, D. Pogony, and M. Zubeidat, "Optimization of integrated vertical DMOS transistors for ESD robustness," in *Proc. ISPSD*, 2004, pp. 221–224.
[40] M. Shrivastava, J. Schneider, M. S. Baghini, H. Gossner, and V. R. Rao, "Highly resistive body STI NDEMOS: An optimized DEMOS device to achieve moving current filaments for robust ESD protection," in *Proc. IEEE IRPS*, 2009, pp. 754–759.
[41] G. Boselli, V. Vassilev, and C. Duvvury, "Drain extended NMOS high current behavior and ESD protection strategy for HV applications in sub-100 nm CMOS technologies," in *Proc. Int. Rel. Phys. Symp.*, 2007, pp. 342–347.
[42] W. Y. Chen, M. D. Ker, Y. N. Jou, Y. J. Huang, and G. L. Lin, "Improvement on ESD robustness of lateral DMOS in high-voltage CMOS ICs by body current injection," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2009, pp. 385–388.
[43] C.-T. Wang and M. D. Ker, "ESD protection design with lateral DMOS transistor in 40-V BCD technology," *IEEE Trans. Electron Devices*, vol. 57, no. 12, pp. 3395–3404, Dec. 2010.
[44] Y. Chung, H. Xu, R. Ida, W.-G. Min, and B. Baird, "ESD scalability of LDMOS devices for self-protected output drivers," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2005, pp. 351–354.
[45] S. Fujiwara, K. Nakaya, T. Hirano, T. Okuda, and Y. Watanabe, "Source engineering for ESD robust NLDMOS," in *Proc. EOS/ESD Symp.*, 2011, pp. 1–6.
[46] A. Goyal, J. Whitfield, C. Gill, C. Rouying Zhan, V. Kushner, A. Gendron, and S. Contractor, "Unique ESD failure mechanism of high voltage LDMOS transistors for very fast transients," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2008, pp. 673–674.
[47] P. Hower, G. Collins, and P. Chakraborty, "Modeling CDM failures in high-voltage drain-extended ESD cells," in *Proc. EOS/ESD Symp.*, 2007, pp. 1B.4-1–1B.4-7.

Mayank Shrivastava (S'09–M'10) received the B.S. degree in engineering from Rajiv Gandhi Technical University, Bhopal, India, in 2006 and the Ph.D. degree from the Indian Institute of Technology (IIT) Bombay, Mumbai, India, in 2010.

From April 2008 to October 2008 and again in May 2010 to July 2010, he was a Visiting Research Scholar with Infineon Technologies AG, Munich, Germany. From 2010 to 2011, he was with Infineon Technologies, East Fishkill, NY, and with Intel Mobile Communications, Hopewell Junction, NY, as a Senior Electrostatic Discharge (ESD) Engineer for the International Semiconductor Development Alliance. He is currently with Intel Mobile Communications, Munich, Germany. He has more than 35 publications in international journals/conferences and has 15 patents issued or pending in the field of ESD protection, drain-extended MOS devices, Fin-shaped field-effect transistors, tunnel field-effect transistors, electrothermal modeling, RF power amplifiers, and nonvolatile memory.

Dr. Shrivastava has served as a Subcommittee Member of the 2012 EOS/ESD Symposium and as a Reviewer for various international journals, which include the IEEE TRANSACTIONS ON ELECTRON DEVICES, the IEEE Electron Device Letters, the IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, Japanese Journal of Applied Physics, and the Journal of Microelectronics Reliability. He was a recipient of the India TR35 Award for the year 2010 (Young Innovator Award from MIT Technology Review 35); the 2008 Best Research Paper Award in circuit design category from Intel Corporation Asia Academic Forum; the 2010 Industrial Impact Award from IIT Bombay; the biography publication by the International Biographical Centre, Cambridge, U.K., in the 2000 Outstanding Intellectuals of the 21st Century in 2010; the Excellence in Thesis Work for his Ph.D. thesis from IIT Bombay in 2010; and Infineon fellowship from 2008 to 2010.

Harald Gossner (M'06–SM'11) received the degree in physics (Dipl. Phys.) from Ludwig Maximilians University of Munich, Munich, Germany, in 1990 and the Ph.D. degree in electrical engineering from the Universität der Bundeswehr, Munich, in 1995.

For 15 years, he has worked on the development of electrostatic discharge (ESD) protection concepts for bipolar, BiCMOS, and CMOS technologies with Siemens and Infineon Technologies. Recently, he has joined Intel Mobile Communications, Munich, where he is currently a Senior Principal Engineer for ESD overseeing the development of robust mobile systems. He has authored and coauthored more than 80 technical papers and 1 book in the field of ESD and device physics. He holds 30 patents on the same topic.

Dr. Gossner is a member of ESDA and EDS. Regularly, he is lecturing tutorials at ESREF, IRPS, and EOSESD symposiums. He has served in the technical program committees of IEDM, EOSESD Symposium, and International ESD Workshop. He currently belongs to the management teams of IEW and EOSESD. In 2006, he became a Cofounder of the Industry Council on ESD Target Levels. Since then, he has been cochairing this committee of 50 leading electronics and IC companies.