A Novel Drain-Extended FinFET Device for High-Voltage High-Speed Applications

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***Abstract*—A novel drain-extended FinFET device is proposed in this letter for high-voltage and high-speed applications. A $2\times$ better $R_{\rm ON}$ versus $V_{\rm BD}$ tradeoff is shown from technology computer-aided design simulations for the proposed device, when compared with a conventional device option. Moreover, a device design and optimization guideline has been provided for the proposed device.**

***Index Terms*—Drain extended, FinFET, high voltage (HV), system-on-a-chip (SoC).**

I. Introduction

AS THE planar bulk MOS device reaches its scaling limits [1], FinFETs [2] or trigate FETs have become popular in the recent days as the technology option for sub-20-nm gate lengths [3]. Moreover, FinFET-like devices are found to be a suitable option for system-on-a-chip (SoC) application [4], which is indeed reported as the key requirement for reduced cost, size, and power while enjoying a better performance in the technologies below the 20-nm node [5]–[7]. A SoC chip in advance CMOS consists of various functional blocks, which fall into two major voltage classes: 1) low voltage (0.8–1.2 V) and 2) high voltage (HV) (2.5–5 V). In conventional/planar bulk CMOS technology, low-voltage blocks are traditionally implemented by the use of thin gate-oxide and small-channel-length devices; however, HV functionalities can be designed by using drain-extended MOS devices [8]. Due to cost-efficient availability of devices in planar CMOS, i.e., lying in various voltage classes, SoC implementation is not an impossible goal. However, the same is not true for FinFET technology, which is due to the challenge to implement HV devices in FinFET technologies.

Keeping HV device requirements for SoC implementation and technological limitations associated with nonplanar process flow in mind, this letter reports a novel drain-extended MOS device for FinFET technology, which we found to be $2\times$ better in terms of on-resistance $(R_{\rm ON})$ versus junction breakdown voltage $(V_{\rm BD})$ tradeoff, when compared with a conventional drain-extended FinFET device.

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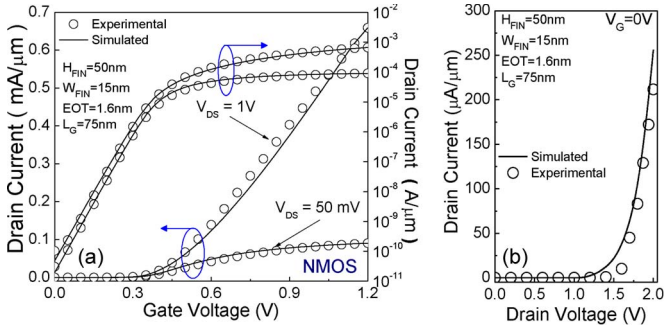

Fig. 1. Calibration of TCAD models for (a) drift–diffusion transport (with quantum corrections) and (b) p-n junction breakdown with experimental data.

II. TCAD Calibration and Framework

An undoped trigate FinFET device, which was fabricated with a midgap metal (TiN) gate; a SiON dielectric (effective oxide thickness (EOT) = 1.6 nm); a channel length L_G of 75 nm; and a target fin width $W_{\rm FIN}$ of 15 nm were used for TCAD calibration. Fig. 1(a) shows the calibration of TCAD model parameters for drift–diffusion transport considering quantum corrections at the oxide–silicon channel interface, which are carefully matched with the experiments. Moreover, mobility degradation due to thin body/fin was accounted into simulations. Furthermore, we used the *New University of Bologna* (UniBo2) model for p-n junction breakdown, which was calibrated with experimental data, as shown in Fig. 1(b).

For the investigation of proposed and conventional devices, we further reduced $W_{\rm FIN}$ and EOT down to 10 and 1 nm, respectively, which were predicted as the target $W_{\rm FIN}$ and EOT for sub-20-nm-node FinFET technologies [1], [2].

III. Novel Drain-Extended FinFET Device

Before we explore a new device concept, it is worth discussing the possible HV device options for FinFET technology by using the conventional understanding of a RESURF LDMOS device for planar fully depleted SOI technology [9], [10]. Fig. 2(a) shows the top view of a conventional HV FinFET SOI device with a lightly doped extended fin region, which allows to increase its breakdown voltage but with the following limitations: 1) Width of the extended drain region is the same as $W_{\rm FIN}$, which is not a design parameter for a *spacer-defined fin* process [11]; 2) increasing L_G does not help much for $V_{\rm BD}$ improvement; and 3) the only method to increase $V_{\rm BD}$ is to reduce extension region doping $N_{\rm EXT}$ and increase extension region length $L_{\rm EXT}$, which however leads to a severe increase in $R_{\rm ON}$.

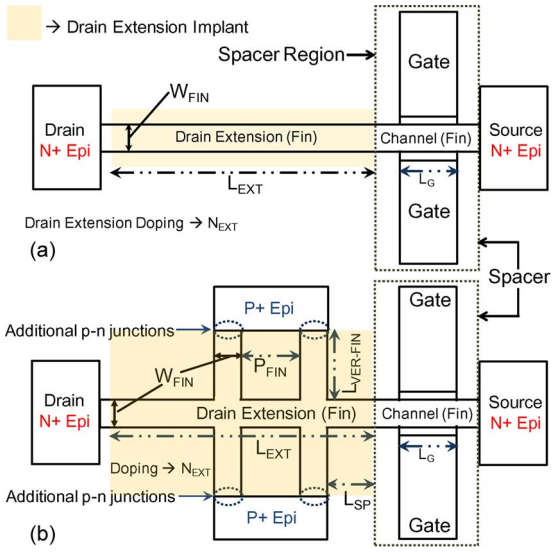

Fig. 2. Top view of (a) conventional and (b) proposed devices. p+ epitaxy was connected to the same potential as the source, i.e., ground. $P_{\mathrm{FIN}} = 40$ nm and $L_{\mathrm{SP}} = 40$ nm were used. The additional p-n junctions are formed at p+ epitaxy and longitudinal fin interface.

Fig. 2(b) shows the top view of the proposed drain-extended FinFET (SOI) device, which, in addition to the conventional drain-extended FinFET architecture [see Fig. 2(a)], i.e., a transverse drain-extended region, consists of longitudinal fins (The number of longitudinal fins is represented as $N_{\mathrm{LONG-FIN}}$.) The longitudinal fins start with a p^+ epitaxial contact (connected to the same potential as the source terminal, i.e., ground or 0 V for nMOS), which then extends into the n^- region (with length $= L_{\mathrm{LONG-FIN}}$) attached with the transverse n^- region.

Note that the transverse and longitudinal n^- regions have identical n^- doping concentration N_{EXT}, that they form additional p-n junctions, and that longitudinal fins are not along the direction of MOS current. Additional p-n junctions reduce space-charge density for an applied potential at the drain. This is attributed to the extension of the space-charge region along the additional p-n junctions, which eventually relaxes the electric field at the n^- drain–channel junction. This is already evident from Poisson's equation as follows:

$$\frac{\partial^2 V}{\partial x^2} = -\frac{\partial E}{\partial x} = -\frac{q \cdot \rho}{\epsilon}$$

where V is the applied potential, E is the electric field, q is the charge, and ρ is the space-charge density. Fig. 3(a) shows that the proposed device has a 3× reduced-peak electric field compared with a conventional device, when 5 V was applied at the drain (gate, source, and body grounded). Additional space-charge regions are formed along the p-n junctions of the longitudinal fin regions. Thus, as shown in the inset in Fig. 3(b) and (c), the proposed device has a significantly relaxed potential distribution near the gate edge, as compared with a conventional device.

IV. Device Design Guidelines and Discussion

Since longitudinal fins do not influence intrinsic MOS operation, as pointed out in Section III, and the proposed device has a 3× reduced electric field, one can predict that the proposed device will have a similar R_{ON} with improved V_{BD}, as compared

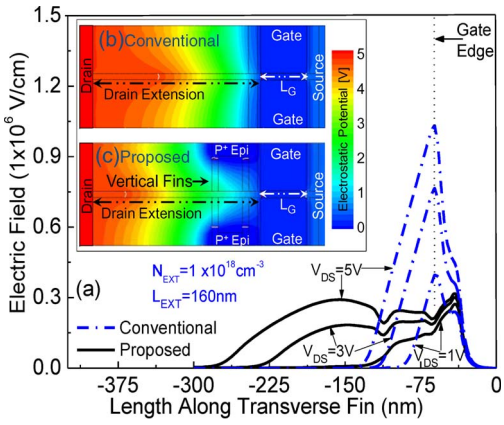

Fig. 3. Physical insight behind the $V_{\mathrm{BD}}/R_{\mathrm{ON}}$ performance tradeoff improvement. (a) Comparison of electric field distribution along the transverse fin in conventional and proposed devices. (b)–(c) Two-dimensional electrostatic potential contour across conventional and proposed devices.

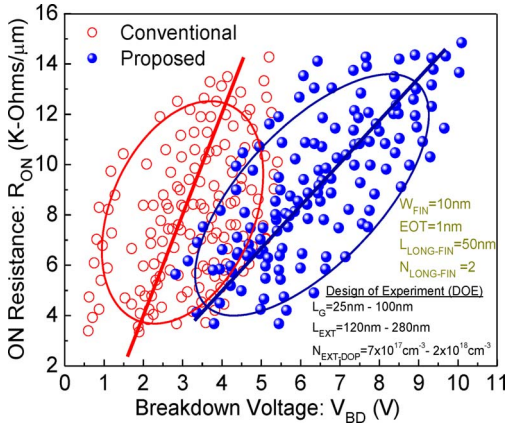

Fig. 4. DOE simulated for conventional and proposed devices.

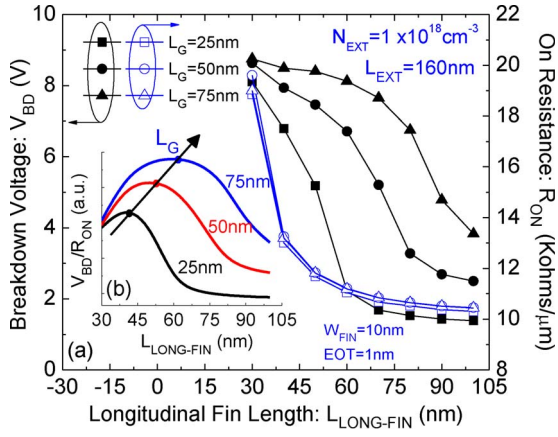

Fig. 5. Optimization of longitudinal fin length as a function of gate length ($N_{\mathrm{LONG-FIN}} = 2$ was used).

with a conventional device. The design-of-experiment results obtained through simulations for conventional and proposed devices in Fig. 4 validate our prediction furthermore and show that the proposed device achieved a ∼2× better R_{ON} versus V_{BD} tradeoff.

Figs. 5 and 6 derive the optimization criterion for $L_{\mathrm{LONG-FIN}}$ and its relation with L_G and N_{EXT}, respectively, while keeping L_{EXT} fixed. Figs. 5(a) and 6(a) show that V_{BD} and R_{ON} increase with different rates when $L_{\mathrm{LONG-FIN}}$ was

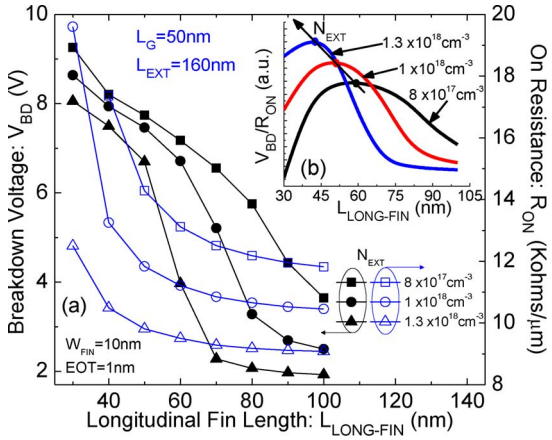

Fig. 6. Optimization of longitudinal fin length as a function of drain extension doping ($N_{\mathrm{LONG-FIN}} = 2$ was used).

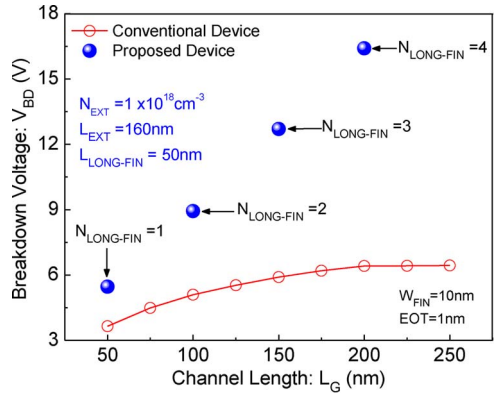

Fig. 7. Impact of channel length on the breakdown voltage of conventional and proposed devices and its relation with the number of longitudinal fins in the proposed device. Note that the symbol representing the proposed device shows only the optimum $V_{\mathrm{BD}}/R_{\mathrm{ON}}$ points corresponding to different $N_{\mathrm{LONG-FIN}}$. Note that the proposed device can achieve significantly higher breakdown voltages without increasing the gate-oxide thickness.

reduced below a certain value depending on the respective L_G and N_{EXT} values. In addition to this, Figs. 5(b) and 6(b) show the optimum value of $L_{\mathrm{LONG-FIN}}$, i.e., V_{BD} should be much higher than the R_{ON} cost adder (maximum $V_{\mathrm{BD}}/R_{\mathrm{ON}}$), as a function of L_G and N_{EXT}. Overall, Figs. 5 and 6 show how the $V_{\mathrm{BD}}/R_{\mathrm{ON}}$ tradeoff can be improved by keeping $L_{\mathrm{LONG-FIN}}$ approximately equal to 50 nm. It is worth pointing out that such an optimization is not possible for a conventional device option. Note that P_{FIN} and L_{SP} have no impact on V_{BD}.

So far, the optimization of $L_{\mathrm{LONG-FIN}}$ and its relation with L_G, L_{EXT}, and N_{EXT} are well understood, and the only unrevealed parameter remaining is the number of longitudinal fins $N_{\mathrm{LONG-FIN}}$. Fig. 7 shows that V_{BD} increases with channel length but saturates after a certain value of L_G, which depends on N_{EXT} and L_{EXT}. However, the proposed device behaves differently when $N_{\mathrm{LONG-FIN}}$ and L_G are increased at the same time. Increasing $N_{\mathrm{LONG-FIN}}$ and L_G simultaneously leads to a much higher breakdown voltage for fixed N_{EXT} and L_{EXT}. This is due to the fact that increasing $N_{\mathrm{LONG-FIN}}$ increases the region of the fin that is affected by the reverse p-n junction area and eventually relaxes the space-charge density (and electric field) for an applied voltage at the drain. Higher $N_{\mathrm{LONG-FIN}}$ for smaller L_G does not improve V_{BD} because, for smaller L_G, channel-to-"drain extension" junction electric field dominates V_{BD}. This can be attributed to the insufficient amount of space-charge contribution by longitudinal fins lying far away from the gate edge.

V. Conclusion

Additional longitudinal fins in the proposed drain-extended FinFET device have improved the breakdown voltage of the device without influencing the MOS behavior. Because of this, the proposed drain-extended FinFET device shows a 2× better R_{ON} versus V_{BD} tradeoff. Further optimization of V_{BD} versus R_{ON} tradeoff in terms of device design parameters such as L_G and $N_{\mathrm{LONG-FIN}}$ for a given N_{EXT} is presented. Such an optimization cannot be achieved for a conventional drain-extended FinFET device. It is worth pointing out that the proposed device can achieve a significantly higher breakdown voltage at a lower gate-oxide thickness, opening up new opportunities for HV high-speed (or RF) applications. The proposed device is also expected to show improved gate-oxide reliability and electrostatic discharge hardness because of the relaxed electric fields and an increased silicon volume.

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