

# Unique Gate Bias Dependence of Dynamic $R_{ON}$ -Resistance in MIS-Gated AlGaIn/GaN HEMTs and Its Dependence on Gate Control Over the 2-DEG

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**Abstract**—This work reports a unique gate bias dependence of dynamic  $R_{ON}$ -resistance in metal–insulator–semiconductor (MIS)-gated AlGaIn/GaN high-electron-mobility transistors (HEMTs). The absence of such dependence in Schottky HEMTs confirms that the phenomenon is unique to MISHEMTs. Based on the observations, the weakening of gate control over GaN channel by the insertion of the gate insulator is proposed as the phenomenon responsible for the observed behavior. The proposal is verified by incorporating high- $\kappa$  (25)  $Al_{0.5}Ti_{0.5}O_y$  as the gate oxide, which successfully mitigated the gate bias dependence of dynamic  $R_{ON}$ -resistance by improving the gate control.

**Index Terms**—AlGaIn/GaN high-electron-mobility transistors (HEMTs), AlTiO, dynamic  $R_{ON}$ -resistance, high- $\kappa$  oxide, metal–insulator–semiconductor HEMTs (MISHEMTs).

## I. INTRODUCTION

**D**YNAMIC  $R_{ON}$ -resistance (dynamic  $R_{ON}$ ) is one of the major challenges encountered by the promising AlGaIn/GaN high-electron-mobility transistor (HEMT) technology for power applications [1]–[22]. The increase in HEMT's  $R_{ON}$  after HEMT either experiencing a high drain voltage stress (in OFF-state) or after undergoing switching cycles is referred to as dynamic  $R_{ON}$ . This OFF-state stressing-induced increase in  $R_{ON}$  has been attributed to charge trapping at the surface [1]–[7] as well as GaN buffer [8]–[20]. Development of novel surface passivation techniques, such as AlN [1], [2],  $SiN_x$  [3], GaN cap [4],  $NH_3$  plasma pretreatment [5], has been able to mitigate any impact of surface traps on the device performance. On the other hand, buffer design to resolve

dynamic  $R_{ON}$  degradation in GaN HEMTs is still a major design challenge [8]–[14]. Furthermore, the requirement of carbon-doping (C-doping) in GaN buffer, which is to enhance the buffer breakdown voltage [23], makes the device engineering rather complex due to introduced traps in the C-doped GaN buffer [24]. This further affects the dynamic performance of HEMTs by participating in electron capture [15], [16] or hole emission processes [17], [18]. Physical insights into different processes affecting dynamic  $R_{ON}$  is therefore necessary to address this device design challenge.

In this context, our recent work revealed an OFF-state stress time and device design-dependent critical drain voltage ( $V_{DS-Stress} = V_{cr}$ ), beyond which dynamic  $R_{ON}$  of the devices increased considerably [15], [16]. Observed  $V_{cr}$  was found to be dependent on carrier trapping in the C-doped GaN buffer [15], [16]. While the impact of OFF-state drain stress voltage was discussed in detail in these works, any impact of gate bias conditions was not discussed. Previous studies on gate bias dependence of dynamic  $R_{ON}$  were limited to lower stress voltages ( $\sim 50$  V) and shorter stress times (few  $\mu s$ ) [20]–[22]. Given our recent studies showing peculiar dynamic  $R_{ON}$  behavior under higher voltage and longer stress times [15], [16], it is imperative to extend it to study the influence of gate bias. In this work, we report a unique OFF-state gate bias ( $V_{GS-Stress}$ ) dependence of dynamic  $R_{ON}$  and  $V_{cr}$  in AlGaIn/GaN metal–insulator–semiconductor (MIS) HEMTs. The observed phenomenon is absent in Schottky-gated devices, indicating it to be unique to MISHEMTs. This study thus presents an additional design challenge for developing reliable AlGaIn/GaN MISHEMTs, which have gained significant prominence due to lower gate leakage offered by these devices. Through detailed experiments and simulations, the observed  $V_{GS-Stress}$  dependence is proposed to be related to gate control over 2-D electron gas (2-DEG), which is validated by demonstrating mitigation of the observed phenomenon by using high- $\kappa$   $Al_{0.5}Ti_{0.5}O_y$  as gate oxide.

## II. DEVICE FABRICATION AND EXPERIMENTATION

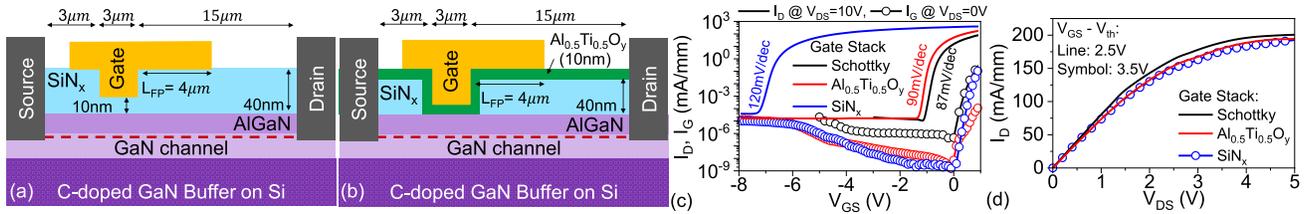
AlGaIn/GaN HEMTs, as seen in Fig. 1(a) and (b), were fabricated on a 6'' commercial-grade C-doped GaN

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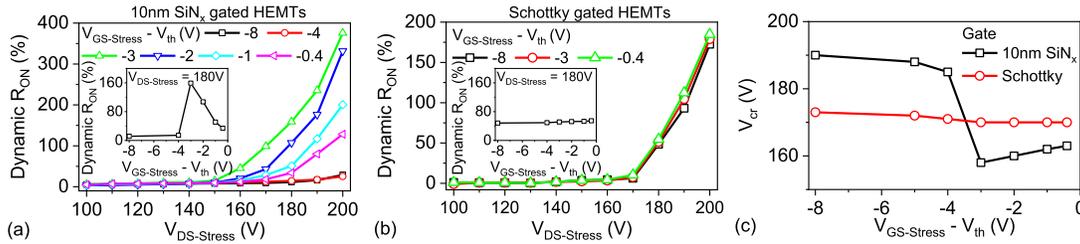
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**Fig. 1.** Schematic of (a)  $\text{SiN}_x$ -gated and (b)  $\text{Al}_{0.5}\text{Ti}_{0.5}\text{O}_y$ -gated AlGaN/GaN MISHEMTs on carbon-doped GaN buffer, fabricated for this work. (c) Transfer ( $I_D - V_{GS}$ ), gate leakage ( $I_G - V_{GS}$ ), and (d) output ( $I_D - V_{DS}$ ) characteristics of the fabricated HEMTs. A higher gate overdrive was provided for the  $I_D - V_{DS}$  characteristics of the  $\text{SiN}_x$ -gated MISHEMTs to ensure similar ON-resistance, despite their weaker gate control.



**Fig. 2.** Dependence of dynamic  $R_{ON}$  on  $V_{DS-Stress}$  for GaN HEMTs with (a)  $\text{SiN}_x$  and (b) Schottky gate, as a function of  $V_{GS-Stress}$ . Inset in the figures shows the dependence of dynamic  $R_{ON}$  on  $V_{GS-Stress}$  for a constant  $V_{DS-Stress}$  of 180 V. (c) Impact of OFF-state gate bias condition ( $V_{GS-Stress}$ ) on critical voltage ( $V_{DS-Stress} = V_{Cr}$ ) for  $\text{SiN}_x$ - and Schottky-gated GaN HEMTs.

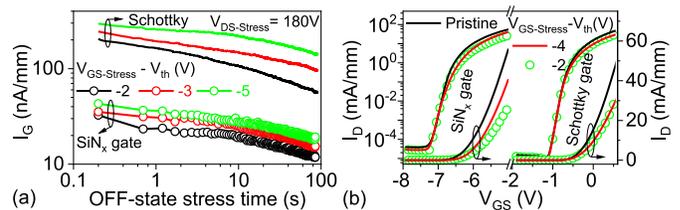
on Si epi-stack (650 V Class) using a well-optimized process [15], [16], [25]. Three device variants were fabricated on the same epi-stack, viz. (a) Schottky-gated HEMTs, (b) MISHEMTs with 10-nm  $\text{SiN}_x$  gate [see Fig. 1(a)], and Fig. 1(c) MISHEMTs with 10-nm  $\text{Al}_{0.5}\text{Ti}_{0.5}\text{O}_y$  (AlTiO) gate [see Fig. 1(b)]. The well-optimized processes [15], [16], [25] ensured superior surface quality of the HEMTs. The transfer, gate leakage, and output characteristics of the fabricated devices are shown in Fig. 1(c) and (d), respectively. The HEMTs show high ON-current, low  $R_{ON}$ , and high ON to OFF ratio, irrespective of the gate-stack. The threshold voltage ( $V_{th}$ ) of the Schottky-,  $\text{SiN}_x$ -, and AlTiO-gated HEMTs were  $-0.9$ ,  $-7$ , and  $-1.1$  V, respectively,  $V_{th}$  being defined as the  $V_{GS}$  for  $I_D$  of  $1 \mu\text{A}/\text{mm}$ . While proper surface cleaning before deposition of the Schottky gate resulted in the low  $V_{th}$  of the Schottky HEMTs [15], use of high- $\kappa$  ( $\kappa \sim 25$ ), and p-type AlTiO as gate oxide led to  $V_{th}$  of  $-1.1$  V for these devices [16], [25], [26]. Moreover, the significantly negative  $V_{th}$  of  $-7$  V for the  $\text{SiN}_x$ -gated HEMTs can be attributed to reduced channel control due to the use of 10-nm-thick low- $\kappa$  ( $\kappa \sim 5$ )  $\text{SiN}_x$  as the gate dielectric [16].

The HEMTs were subjected to a measure-stress-measure-relax cycle, with substrate grounded, to evaluate dynamic  $R_{ON}$  [14]–[16]. After pristine  $R_{ON}$  ( $R_{Pristine}$ ) measurement, devices were subjected to an OFF-state stress for 100  $\mu\text{s}$ . Immediately after the stress, post-stress  $R_{ON}$  ( $R_{Post-Stress}$ ) was measured to evaluate dynamic  $R_{ON}$  of the device as:  $\text{Dynamic } R_{ON} = (R_{Post-Stress} - R_{Pristine})/R_{Pristine} \times 100\%$ . Here,  $R_{ON}$  is calculated from the inverse slope of the output characteristics for  $V_{DS}$  ranging from 0.25 to 0.5 V. Devices were also allowed to relax for  $\sim 180$  s in between two stress cycles, to completely recover to the pristine condition.

### III. EXPERIMENTAL OBSERVATIONS AND DISCUSSION

#### A. Impact of OFF-State Stress Conditions on Dynamic $R_{ON}$

Fig. 2(a) depicts the impact of  $V_{DS-Stress}$  and  $V_{GS-Stress}$  on the dynamic  $R_{ON}$  performance of the  $\text{SiN}_x$ -gated HEMTs.



**Fig. 3.** (a) Gate leakage with OFF-state stress time of the  $\text{SiN}_x$ -gated and Schottky HEMTs, as a function of  $V_{GS-Stress}$ . (b)  $I_D - V_{GS}$  sweeps at  $V_{DS} = 10$  V, of  $\text{SiN}_x$ -gated and Schottky HEMTs, measured immediately after  $V_{DS-Stress}$  of 180 V, as a function of  $V_{GS-Stress}$ . The measurements were done under dark conditions with  $V_{GS}$  swept from positive to negative.

Devices show a  $V_{Cr}$  beyond which dynamic  $R_{ON}$  degrades significantly. Moreover, the value of dynamic  $R_{ON}$  [depicted in the inset of Fig. 2(a)] and  $V_{Cr}$  are observed to be significantly dependent on the value of  $V_{GS-Stress}$ . On the other hand,  $V_{Cr}$  and dynamic  $R_{ON}$  are found to be independent of  $V_{GS-Stress}$  for Schottky HEMTs, as seen in Fig. 2(b). This dependence of  $V_{Cr}$  on  $V_{GS-Stress}$  is further highlighted in Fig. 2(c). Unlike the Schottky HEMT,  $V_{Cr}$  of the  $\text{SiN}_x$ -gated HEMT reduced from  $\sim 190$  to  $\sim 150$  V, when  $V_{GS-Stress}$  was marginally reduced from  $V_{th} - 4$  V to  $V_{th} - 3$  V. Any increase or decrease in  $V_{GS-Stress}$  from these bias points results in a marginal increase in  $V_{Cr}$ . It is worth highlighting here that though the gate bias was varied, it was ensured that the device remained in OFF-state by keeping  $V_{GS-Stress} < V_{th}$ . Above observations make determining operating conditions and performance of MISHEMTs a strong function of gate bias conditions.

#### B. Source of $V_{GS-Stress}$ Dependence

The  $\text{SiN}_x$  and Schottky-gated devices, discussed in Fig. 2, were processed simultaneously on the same GaN buffer stack and similar  $\text{SiN}_x$  passivation, with the only difference in gate-stack. This establishes the observed dependence on  $V_{GS-Stress}$  to be a gate-stack-dependent phenomenon. MIS gate-stack affects three major device parameters, (a) gate leakage, (b)  $V_{th}$  modulation due to traps in the gate-stack, and (c) gate's control over the 2-DEG.

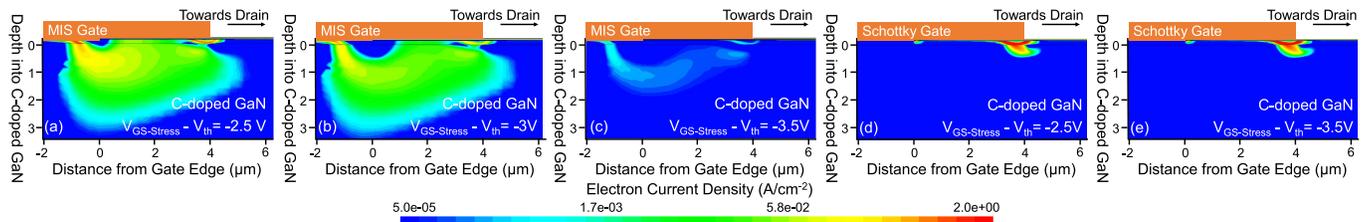


Fig. 4. Electron current density extracted in  $\text{SiN}_x$ -gated HEMTs at a  $V_{\text{GS-Stress}} - V_{\text{th}}$  of (a)  $-2.5$  V, (b)  $-3$  V, (c)  $-3.5$  V, and in Schottky HEMTs at a  $V_{\text{GS-Stress}} - V_{\text{th}}$  of (d)  $-2.5$  V, and (e)  $-3.5$  V. A  $V_{\text{DS-Stress}}$  of 200 V was taken with  $L_{\text{GD}} = 15 \mu\text{m}$ ,  $L_{\text{FP}} = 4 \mu\text{m}$ , and 40 nm  $\text{SiN}_x$  passivation.

Fig. 1(c) shows the gate leakage of the  $\text{SiN}_x$ -gated HEMTs to be significantly lower than the Schottky HEMTs due to the presence of the gate dielectric. If gate leakage is considered to play a major role in determining the dynamic  $R_{\text{ON}}$  performance of the GaN HEMTs, a lower gate leakage should reduce the dynamic  $R_{\text{ON}}$  of MISHEMTs. However, the phenomenon as depicted in Fig. 2(c) is observed only in MIS-gated devices (with lower gate leakage) but is absent in Schottky devices (with comparatively higher gate leakage). This suggests that gate leakage plays a minimal role in determining the unique gate bias-dependent dynamic  $R_{\text{ON}}$  in the MISHEMTs. It is also worth highlighting that when  $V_{\text{GS-Stress}}$  was increased in the negative direction, the gate current increased monotonously for both  $\text{SiN}_x$ - and Schottky HEMTs, as shown in Fig. 3(a). On the other hand,  $V_{\text{cr}}$  and dynamic  $R_{\text{ON}}$  of the  $\text{SiN}_x$ -gated MISHEMTs showed a different dependence on  $V_{\text{GS-Stress}}$  [see Fig. 2(a) and (c)], wherein  $V_{\text{cr}}$  initially reduced, showed a considerable increase and then remained constant as  $V_{\text{GS-Stress}}$  was reduced below  $V_{\text{th}}$ . This observation further validates that the mechanism responsible for  $V_{\text{GS-Stress}}$  dependence of dynamic  $R_{\text{ON}}$  is not attributed to gate leakage. Furthermore, it should also be noted that no  $V_{\text{th}}$  shift was observed for these devices, immediately after  $V_{\text{DS-Stress}}$  of 180 V for different  $V_{\text{GS-Stress}}$  values, as shown in Fig. 3(b). This indicates negligible trapping at the gate insulator–semiconductor interface or the gate-stack, which would otherwise result in an observable  $V_{\text{th}}$  shift. Therefore, the observed phenomenon can also not be attributed to trapping at the gate insulator–semiconductor interface or the gate-stack. This further indicates trapping in the access region as the source of dynamic  $R_{\text{ON}}$  degradation in these devices.

To investigate the third aspect, that is, the role of gate control modulation due to dielectric insertion, Fig. 4(a)–(c) compare the simulated source–drain leakage path for  $\text{SiN}_x$ -gated devices with different  $V_{\text{GS-Stress}}$ . Fig. 4(a) and (b) shows that the leakage path extends deeper into the C-doped GaN buffer as  $V_{\text{GS-Stress}}$  is reduced below  $V_{\text{th}}$ . This exposes a larger concentration of C-doping-induced traps to the injected carriers. This in turn leads to a higher dynamic  $R_{\text{ON}}$  with reduced  $V_{\text{cr}}$ , as seen experimentally for  $V_{\text{GS-Stress}} - V_{\text{th}} \geq -3$  V [see Fig. 2(c)]. On the other hand, Fig. 4(c) shows a significant reduction in electron current density, as the electron current path follows a longer trajectory in C-doped GaN buffer, when  $V_{\text{GS-Stress}}$  was lowered further. This reduces the carrier injection and hence carrier trapping in the GaN buffer, which in turn results in lower dynamic  $R_{\text{ON}}$  and higher  $V_{\text{cr}}$  as seen experimentally for  $V_{\text{GS-Stress}} - V_{\text{th}} \leq -4$  V in Fig. 2(c).

To investigate how this carrier injection into the GaN buffer is affected by the gate’s control over the 2-DEG,

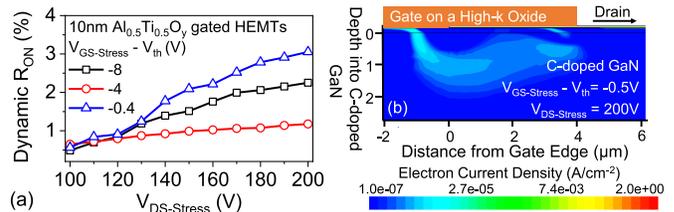


Fig. 5. (a) Dynamic  $R_{\text{ON}}$  characteristics of  $\text{Al}_{0.5}\text{Ti}_{0.5}\text{O}_y$ -gated HEMTs as a function of  $V_{\text{GS-Stress}} - V_{\text{th}}$  and  $V_{\text{DS-Stress}}$ . (b) Electron current density extracted in high- $\kappa$  ( $\kappa = 25$ )-gated HEMTs at  $V_{\text{GS-Stress}} - V_{\text{th}}$  of  $-0.5$  V. The only difference in the device was the gate dielectric’s  $\kappa$  value.

Schottky-gated devices were analyzed. Fig. 1(c) shows better gate control in Schottky HEMTs (subthreshold slope (SS) = 87 mV/dec), when compared with  $\text{SiN}_x$ -gated HEMTs (SS = 120 mV/dec). Simulated electron current density for Schottky HEMTs, as shown in Fig. 4(d), shows that the improved gate control effectively suppresses the source–drain leakage path for Schottky HEMTs. However, electron injection into the C-doped GaN buffer now occurs near the field plate (FP) edge due to significant gate leakage current observed in the Schottky devices. This leads to dynamic  $R_{\text{ON}}$  in Schottky HEMTs with a  $V_{\text{cr}}$ , as seen in Fig 2(b). However, given the leakage path in the C-doped GaN buffer originates near the FP edge, it is not affected by gate control and is independent of  $V_{\text{GS-Stress}}$ , as seen in Fig. 4(d) and (e). This explains the  $V_{\text{GS-Stress}}$  independence of  $V_{\text{cr}}$  in Schottky HEMTs, as seen in Fig. 2(b).

The above discussion indicates weaker gate control in MISHEMTs to be responsible for the observed  $V_{\text{GS-Stress}}$  dependence of dynamic  $R_{\text{ON}}$ . To validate the proposed phenomenon AlTiO-gated ( $\kappa = 25$ ) [25] devices, as shown in Fig. 1(b), were fabricated. The AlTiO-gated devices, with an SS of 90 mV/dec, demonstrated a gate control similar to that of Schottky HEMTs, as seen in Fig. 1(c), and resulted in  $V_{\text{GS-Stress}}$  independent dynamic  $R_{\text{ON}}$ , as seen in Fig. 5(a). The simulated leakage current path for GaN HEMTs with a high- $\kappa$  ( $\kappa = 25$ ) gate oxide is shown in Fig. 5(b). It establishes a significant reduction in source–drain leakage through C-doped GaN buffer for devices with a high- $\kappa$  gate oxide, even for a lower  $V_{\text{GS-Stress}} - V_{\text{th}}$ . The improved gate control [see Fig. 1(c)] and associated reduction in leakage current [see Fig. 5(b)] results in  $V_{\text{GS-Stress}}$  independence of dynamic  $R_{\text{ON}}$  in high- $\kappa$  AlTiO-gated GaN MISHEMTs, as seen in Fig. 5(a). The above discussions thus establish degraded channel control, due to incorporation of gate dielectric, to result in a  $V_{\text{GS-Stress}}$ -dependent dynamic  $R_{\text{ON}}$  in AlGaIn/GaN MISHEMTs.

#### IV. CONCLUSION

This work reports a unique gate bias-dependent critical OFF-state drain stress voltage, beyond which dynamic  $R_{\text{ON}}$

of AlGaIn/GaN MISHEMTs on C-doped buffer degrades significantly. Experiments were conducted on Schottky-gated and MIS-gated HEMTs; both realized using the same epi-stack and passivation. Schottky-gated HEMTs reveal the critical voltage in dynamic  $R_{ON}$  to be independent of gate bias condition. The same, however, was a strong function of gate bias in the case of MIS-gated devices. This unique dependence is caused by reduced gate control in MIS-gated devices, which modifies the source–drain leakage path through the GaN buffer. This, in turn, modulates carrier injection into the C-doped GaN buffer leading to gate bias-dependent dynamic  $R_{ON}$ . The proposed phenomenon is further validated using high- $\kappa$   $Al_{0.5}Ti_{0.5}O_y$  gate oxide-based HEMTs, which relaxed the dependence of dynamic  $R_{ON}$  on the gate bias conditions due to superior channel control. This study thus establishes gate bias conditions and channel control to play a major role in determining the dynamic  $R_{ON}$  of AlGaIn/GaN MISHEMTs.

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