Physical Insight Toward Heat Transport and an Improved Electrothermal Modeling Framework for FinFET Architectures

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***Abstract*—We report on the thermal failure of fin-shaped field-effect transistor (FinFET) devices under the normal operating condition. Pre- and postfailure characteristics are investigated. A detailed physical insight on the lattice heating and heat flux in a 3-D front end of the line and complex back end of line—of a logic circuit network—is given for bulk/silicon-on-insulator (SOI) FinFET and extremely thin SOI devices using 3-D TCAD. Moreover, the self-heating behavior of both the planar and nonplanar devices is compared. Even bulk FinFET shows critical self-heating. Layout, device, and technology design guidelines (based on complex 3-D TCAD) are given for a robust on-chip thermal management. Finally, an improved framework is proposed for an accurate electrothermal modeling of various FinFET device architectures by taking into account all major heat flux paths.**

***Index Terms*—BEOL reliability, electrothermal modeling, ESD, extremely thin silicon on insulator (SOI) (ETSOI), fin-shaped field-effect transistor (FET) (FinFET), thermal fail.**

I. Introduction

With the downscaling of technology down to the 20-nm node, planar devices have shown degraded switching characteristics [1]. This has motivated researchers to come up with a number of nonconventional planar and nonplanar CMOS devices, such as tunnel field-effect transistors (FETs), fin-shaped FETs (FinFETs), nanowire FETs, impact ionization MOS, and extremely thin silicon-on-insulator (SOI) (ETSOI) FETs, as technology options for sub-22-nm node gate lengths [2]–[4]. One such device which shows tremendous potential to scaling, while maintaining CMOS compatibility, is FinFET. FinFET is a nonplanar device with a thin fin between source and drain forming the channel. The thin fin is surrounded by the gate on the top three sides, with thickness and height of the fin defining the effective channel width. Among the two important kinds of FinFETs—SOI and bulk—both the devices show almost the same on-to-off current ratio [5]–[7]. However, the differences appear due to factors such as junction leakage, parasitic capacitances, etc. In SOI FinFETs, it becomes easier to avoid latchup and achieve desired performance, because of the isolation provided by the buried oxide (BOX) [7], [8]. Alternatively, extremely thin body SOI (ETSOI) FETs were demonstrated as an option for sub-22-nm gate lengths, with advantages such as lower 3-D parasitics, ease of incorporating strain effects, flexibility in width selection, and suppressed random dopant fluctuation [9], [10].

The electrical characteristics of these devices are well understood; however, thermal behavior still needs a detailed study. These devices are expected to suffer from heavy self-heating, as nanoscale dimensions in the devices cause a high thermal resistance between heat source and sink, causing poor thermal coupling. It is due to this self-heating that the saturation currents in SOI devices get reduced by almost 10%–15% and the maximum allowable frequency gets limited [11]. The increase in overall temperature due to the device's self-heating degrades many other important parameters including chip's lifetime [12], [13]. The basic phenomenon behind the self-heating is attributed to electron phonon interaction occurring in the high-electric-field region near the drain-to-channel junction. The detailed physics behind heat generation and its conduction within semiconductors is explained elsewhere [14], [15].

So far, there have been several studies on possible heat flow paths in FinFETs [16]–[21]. Few of them claim interconnect to be the prime heat flow path, while others assume that most of the heat should leave through the substrate of the chip, i.e., silicon (Si) body. As per [17], maximum heat dissipates out through the BOX, whereas [18]–[20] establish the fact that most of the heat indeed gets away from active region through interconnect metals. In [19], authors have compared metal/polygate FinFETs for their impact on the self-heating behavior and have found metal gates to give better thermal performance, thus supporting the fact that significant part of the heat flows through gate contacts and, hence, through interconnects. These investigations [16]–[21] were, however, based on certain assumptions on thermal boundary condition, which are not always realistic.

So far, different electrothermal models for the same have been proposed [22]–[24]. The models in [23] and [24] consist of lumped resistances for the entire sections of the device even though the heat flux paths are 3-D in nature. FinFET-like devices necessitate modeling of the sections with finer

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granularity in order to achieve a better accuracy while including the 3-D nature of heat flux, which is missing in the literature. In addition to this, the boundary conditions in these models [22]–[24] assume an isothermal surface next to the electrical contacts without including the BEOL topology and assuming that most of the heat leaves through BOX. Also, the additional rise in temperature due to hot ambience caused by neighboring devices switching simultaneously has been ignored in previous studies. Moreover, often, adiabatic boundaries are assumed for all other surfaces, which is a debatable issue. Such boundary conditions rule out any heat flux via the bottom silicon substrate. A practical definition of thermal boundary condition is still missing in the literature. In another study, a new device structure was proposed in order to relieve self-heating in FinFET devices [21]. This proposal was based on the thermal boundary conditions discussed in [22]–[24], with the limitations discussed earlier.

Extending the previous work on heat flux in realistic BEOL of ETSOI and SOI FinFETs [25], this paper emphasizes our investigations on bulk FinFETs and guidelines for 3-D lumped element modeling. Moreover, this paper performs the following:

1) establishes practical thermal boundary conditions;
2) gives a proper understanding of the heat transport by taking into account realistic BEOL structures;
3) provides design guidelines taking BEOL details into account and their impact on thermal management;
4) includes additional temperature rise due to hot ambience caused by devices switching simultaneously in the neighborhood;
5) describes the impact of various FinFET device architectures on thermal management by taking into account all major heat flux paths into account.

This paper is arranged as follows. Experimental results and TCAD calibrations are presented in Sections II and III, respectively, while physical insight into the thermal behavior and heat transport in ETSOI and SOI/bulk FinFET devices is given in Section IV. Moreover, we have provided useful FEOL/BEOL design guidelines for sub-22-nm node device options in Section IV, by taking into account complete BEOL/FEOL details in our investigations. A new framework is proposed for an accurate electrothermal modeling of FinFET-like architectures in Section V, which takes all major heat flux paths into account extracted from 3-D TCAD simulation. In Section VI, we have demonstrated the performance of various trigate and tall-fin FinFET architectures using our proposed model. Finally, Section VII concludes this paper.

II. Device Fabrication and Experimental Results

Undoped trigate FinFET devices were fabricated with a metal midgap TiN gate and SiON dielectric ($EOT = 1.9$ nm). All fins are processed with a target width of 15 nm and length of 70 nm and are of 60-nm height.

A. Experiments

Fig. 1 shows $I_{\rm DS}$–$V_{\rm DS}$ characteristics of the fabricated FinFET devices. While stressing beyond $V_{\rm DS} = 1$ V, it can be observed that the device suffers from high impact ionization at lower gate bias under which the drain current is extremely low compared to its ON current ($I_{\rm ON}$). However, almost negligible impact ionization at higher gate bias (i.e., higher drain current) was observed. It is evident that the observed impact ionization current is due to a high lateral electric field (under low vertical electric field) at smaller gate bias and higher drain bias. There can be two distinct physical arguments for the observed behavior at high drain and gate bias, i.e., high electric field and current density.

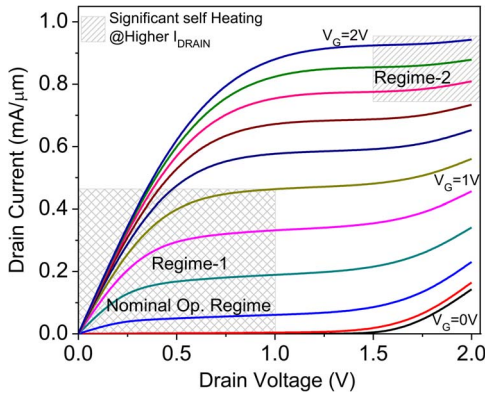

Fig. 1. Measured I_D–V_D characteristics of a FinFET device. Mitigated impact ionization at higher bias conditions shows the presence of significant self-heating.

1) The lateral electric field is lowered near the drain under high gate bias, which eventually mitigates impact ionization at drive current.
2) Under high drive current and high lateral electric field, the device gives rise to a significantly higher lattice temperature, which eventually degrades the generation of excess carriers from impact ionization [26], [27].

TCAD simulations prove that self-heating is the dominating effect. The device significantly suffers from self-heating even under low operating condition ($\sim 2 \times V_{\rm DD}$). It is worth mentioning that the device failed after three to four measurements when it was stressed under $V_{\rm DS} = V_{\rm GS} = 2$ V ($\sim 2 \times V_{\rm DD}$). Fig. 2 compares the leakage behavior of the virgin device and the failed device. It is evident from Fig. 2 that the device suffered a thermal failure, which further motivates the requirement of modeling electrothermal behavior in various FinFET architectures.

B. Discussion

In order to validate our arguments and motivation, Fig. 3 shows a typical failure picture of a FinFET device stressed for 100 ns under a high current ($= 6$ mA/μm) and a high electric field ($V_{\rm DRAIN} = 3$ V), which can easily lead to thermal failure by giving rise to a lattice temperature ($T_{\rm MAX}$)[1] above 1000 K [28]. Moreover, our TCAD simulations predict a temperature rise of 400 K–500 K under nominal operating conditions (i.e., $V_{\rm DD} = 1$ V and $I_{\rm ON} \sim 0.5$ mA/μm), when stressed for 1 ms. Based on these observations, one can easily predict the thermal

[1] $T_{\rm MAX} \propto \int J.E dt$, where J is the current density, E is the electric field, and dt is the stress time.

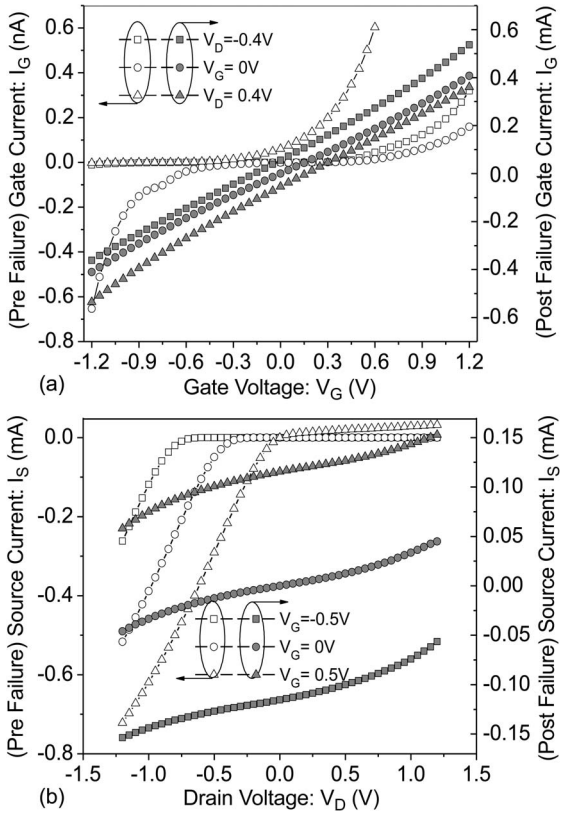

Fig. 2. (a) and (b) Post- and prefailure currents. The figures show significantly high leakage current after three measurements. Postfailure characteristics show a very low resistance path from drain to gate and from drain to source, which in conjunction with self-heating behavior (Fig. 1) validates an early thermal failure.

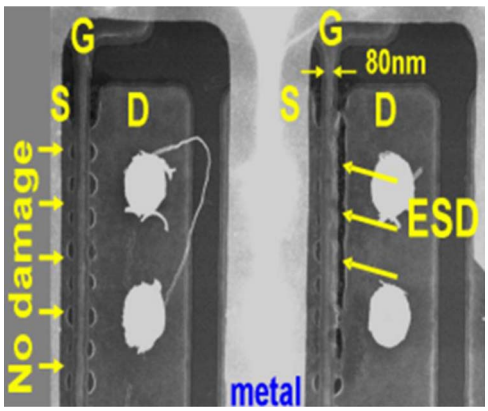

Fig. 3. SEM (failure analysis) picture of a FinFET device, which shows a typical thermal fail of the device under ESD-like stress condition.

behavior of FinFETs or similar nanoscale devices operating at an ON current $\sim$1 mA/μm or higher [29].

III. Model Calibration and TCAD Framework

A well-calibrated 3-D device simulation deck was used for this work where the source/drain and channel doping profiles of realized devices were extracted from Monte Carlo implant (atomistic) simulations [30]. Fig. 4 shows the calibration of TCAD model parameters for drift–diffusion transport considering quantum corrections at the oxide–silicon channel interface, which is carefully matched with the experimental data. The channel in FinFET is on the sidewall of the fin that lies on a (110) plane, if the device is fabricated on a wafer having orientation (100). Due to the dissimilar effective mass values along the various axes, hole mobility in FinFET gets enhanced, and electron mobility gets degraded as compared to conventional planar devices with (100) surface orientation [31]. Sidewall roughness, stress, and strain also affect the mobility. Since the default model parameters of the device simulator are for (100) plane, the mobility model parameters have been modified for (110) plane. The values of the model parameters were then extrapolated to 22-nm L_G devices as described in [32]. The contact resistivity value chosen for all simulations is $2.4 \times 10^{-8}\ \Omega \cdot \mathrm{cm}^2$.

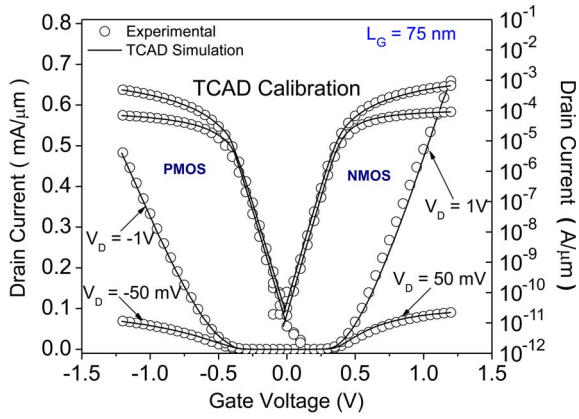

Fig. 4. Calibration of TCAD models for 3-D drift–diffusion transport (considering quantum corrections) with experimental data. Note that the left and right y-axes are on linear and log scales, respectively.

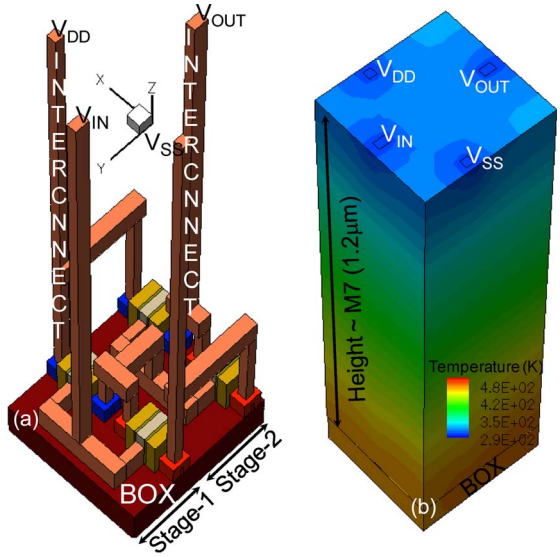

Fig. 5. (a) Two-stage driving inverter with full BEOL definition. (b) Temperature distribution up to seven metal layers which shows the impact of boundary conditions.

In order to fully capture the heat flux through various interconnect lines and interlayer dielectric (ILD) regions, a two-stage Inverter-driving-inverter with full BEOL definition is realized for TCAD simulations, which is shown in Fig. 5. Layout rules for 22-nm length scale were taken from predictive

TABLE I
DIMENSIONAL/LAYOUT AND THERMAL PARAMETERS TAKEN FROM [30], [33], AND [34]

Symbol	Quantity	Values used in this work
L_G	Channel Length	22nm
W_{FIN}	Fin Width	8nm
$W_{interconnect}$	Interconnect Metal Width	28nm
$H_{interconnect}$	Interconnect Metal Height	59nm
$L_{contact}$	Length of Contact Hole	22nm
$W_{contact}$	Width of Contact Hole	22nm
$H_{contact}$	Height of Contact Hole	115nm
H_{Box}	Buried Oxide Thickness	100nm
H_{FIN}	Fin Height	30nm
H_{gate}	Metal Gate Height	70nm
$L_{SourceFin}$	Length of Source Fin	30nm
$L_{DrainFin}$	Length of Drain Fin	30nm
L_{Pad}	Length of Contact pad	40nm
W_{Pad}	Width of Contact Pad	50nm
t_{Si}	Silicon Thickness below BOX	980-250μm
$L_{NitrideSpacer}$	Nitride Spacer thickness	25nm
$L_{GatePad}$	Length of Gate Contact Pad	40nm
$W_{GatePad}$	Width of Gate Contact Pad	50nm
$H_{NitrideSpacer}$	Height of Nitride Spacer	70nm
$L_{interconnect}$	Total Interconnect Height	1.2μm
K_{Nitride}	Nitride Thermal Conductivity	18.5 W/K-m
K_{Metal}	Metal Thermal Conductivity	385 W/K-m
K_{BOX}	Buried Oxide Thermal Conductivity	1.4 W/K-m
K_{ox}	Gate Oxide Thermal Conductivity	1.35 W/K-m
K_{finSi}	Silicon S/D Thermal Conductivity	62 W/K-m
K_{gate}	Gate Metal Thermal Conductivity	238 W/K-m
$K_{channelSi}$	Silicon Channel/Fin Thermal Conductivity	25 W/K-m
K_{ILD}	Interlayer Dielectric Thermal Conductivity	1.4 W/K-m
$K_{bottomSi}$	Thermal Conductivity of Silicon below BOX	148 W/K-m

technology model [33]. The simulation approach used in this work is to extract quasi-static temperature (i.e., the worst case temperature), which should be the cumulative rise in peak temperature after 1000 s of pulses, and is discussed in our work elsewhere [20]. Thermal properties of various regions are calibrated as per their exact dimensions and region-specific material used in a typical CMOS process flow. Table I shows various layout/dimensional and calibrated thermal parameters used for TCAD simulations. The same is used later for deriving a modified electrothermal model and related framework.

IV. PHYSICAL INSIGHT AND DESIGN GUIDELINES

Figs. 5(b) and 6 show the temperature distribution across BEOL (i.e., along the interconnect metals) and FEOL (i.e., in the active regions) of a two-stage inverter designed using FinFET devices. Fig. 6 shows that hot spot is located near the drain-to-channel junction. Channel current under the influence of high lateral electric field at drain-to-channel junction leads to strong heat dissipation (due to the phonon generation), which eventually gives rise to a significant lattice temperature. Moreover, Fig. 7 shows that maximum contribution of heat flux is through metal interconnect instead of Si body unlike the theories presented in [17]. This was observed for SOI FinFET, ETSOI devices, as well as for bulk FinFETs too. This behavior is attributed to the following: 1) high thermal resistance of the silicon substrate compared to metal interconnects; 2) significantly lower thermal conductivity of thin silicon fins; and 3) substrate/Si-body topology in bulk FinFETs. A simple calculation shows that the thermal resistance of a Si body

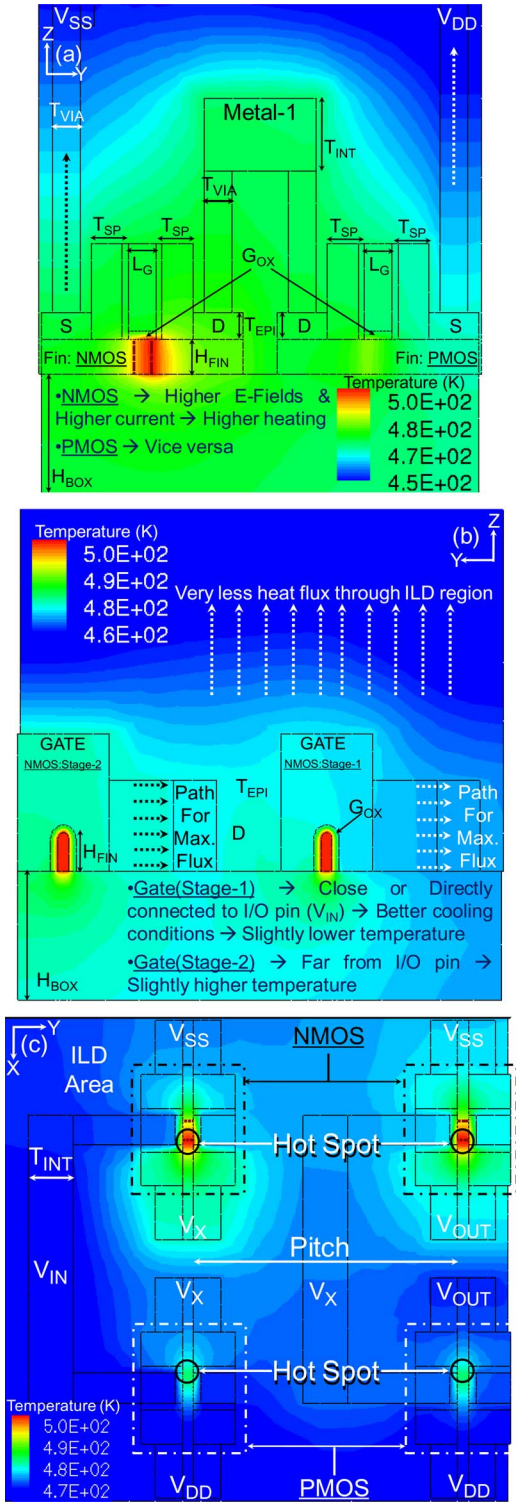

Fig. 6. (a) Heat flux per unit area from various heat sinkers (or thermal contacts). (b) Temperature distribution across the interconnect metals and active (Si) region along different planes. The figures show the following: 1) NMOS has a higher temperature rise as compared to PMOS; 2) devices close to I/O pads have lower heating as compared to others, which is due to better cooling conditions; and 3) maximum heat flux is through interconnect metals as compared to BOX and ILD layers.

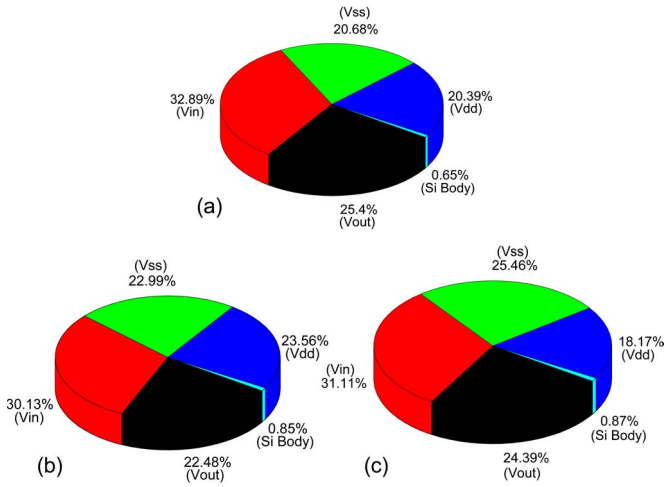

Fig. 7. Percentage of heat flux coming out from various parts of the investigated logic network designed using (a) SOI FinFET, (b) bulk FinFET, and (c) ETSOI devices, respectively. The figures show that most of the thermal energy flows through interconnect metals, whereas the back side of the chip (Si body) has a negligible contribution on the overall heat flux coming out of the chip.

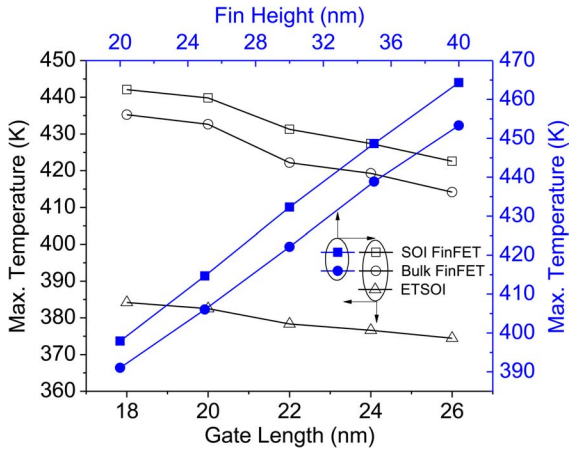

Fig. 8. Impact of scaling gate length and fin height on the self-heating behavior. The figure shows the following: 1) ETSOI device has a smaller temperature rise as compared to FinFET device, and 2) fin height scaling in FinFET device (similar to active area scaling of ETSOI) and gate length scaling can counterbalance the self-heating effect.

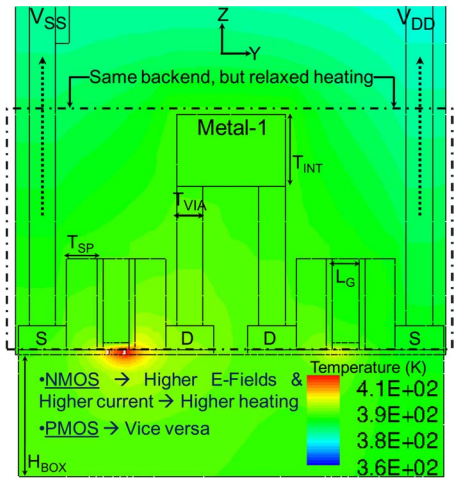

Fig. 9. Self-heating in ETSOI devices. It shows relaxed self-heating in ETSOI device, which is due to lower volume of power source while keeping the BEOL same.

was 15× higher compared to that of a metal interconnect. Note that the thermal resistances (for a unit cross section area) of 100-nm-thick BOX, 1-μm-long metal interconnect, and 250-μm-thick Si body are 71 nK $\cdot$ m^2/W, 2.6 nK $\cdot$ m^2/W, and 1.7 μK $\cdot$ m^2/W, respectively. Such a high thermal resistance contributed by Si body leads to most of the heat to sink into the overlying back-end metallization instead of the silicon body. Moreover, substrate topology in bulk FinFETs (a narrow inactive fin surrounded by STI, which is in between hot spot and large Si body) does not allow dumping all heat in the Si body in a similar fashion as it does for planar bulk MOS devices. Note that NMOS devices have a higher temperature rise as compared to PMOS, which is due to a relatively higher drive current of NMOS device.

A. Impact of Device Scaling

Fig. 8 shows the impact of technology scaling over the self-heating behavior. As a rule of thumb [34], if a FinFET device with a fin width ($W_{\rm FIN}$) of 15 nm and a channel length (L_G) of 25 nm scales down to $L_G = 16$ nm, its fin width should also scale down from 15 down to 8 nm, in order to keep the leakage unchanged. This will eventually scale down the fin height from 45 down to 24 nm, to keep the aspect ratio unchanged. Considering the trends shown in Fig. 8 and the aforementioned rule of thumb, one can get an indication that technology scaling should not affect the thermal performance significantly if fin width and fin height are scaled simultaneously with channel length scaling. Moreover, Fig. 9 shows self-heating effects in the logic network designed using ETSOI device. It is evident from Figs. 8 and 9 that ETSOI devices suffer less from self-heating compared to FinFET device.

It is worth mentioning that the rise in lattice temperature depends on the following: 1) volume of power source (active region); 2) volume of heat sink in the surrounding area; and 3) thermal boundary conditions in the exteriors which define the quasi-static temperature rise. Relaxed lattice temperature in ETSOI device can be attributed to a smaller power density within a given volume of active Si region in ETSOI device compared to the same in FinFET device, while keeping the BEOL definition identical for both the devices.

B. Impact of Wafer Thickness and Interconnect Height

In order to validate our argument about the significant rise in lattice temperature due to a 15× higher thermal resistance of Si body compared to that of metal interconnect, the impact of Si-body thickness and interconnect height is investigated in this section. Fig. 10(a) shows that, when the substrate thickness was greatly reduced, the rise in overall temperature relaxes significantly, which is attributed to an increased flow of thermal energy through heat sink connected with the Si body as shown in Fig. 10(b). Moreover, Fig. 11 shows that, when the interconnect height is increased, the overall temperature rises significantly for a thicker substrate ($T_{\rm Si} = 950$ m) as well as for a thinner substrate ($T_{\rm Si} = 250$ μm). On the other hand,

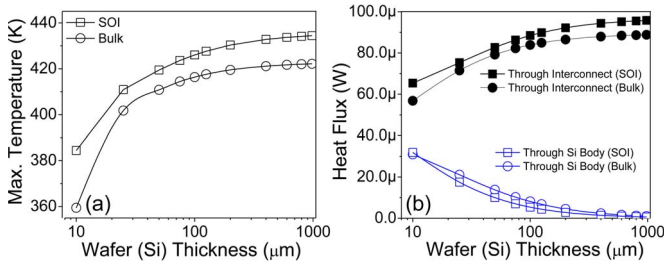

Fig. 10. Figure shows the impact of wafer/silicon thickness ($T_{\rm Si}$) on the (a) self-heating behavior and (b) flow of energy (i.e., heat flux) through the heat sinks connected with interconnect metals and silicon substrate (back side of the chip).

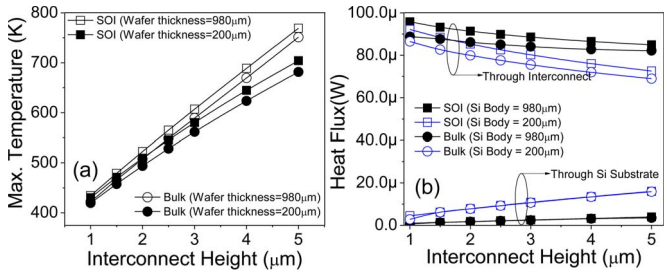

Fig. 11. Impact of interconnect height on the (a) self-heating behavior and (b) heat flux through heat sinks connected with interconnect metals and silicon substrate of SOI as well as bulk FinFETs with $T_{\rm Si} = 950$ and 200 μm.

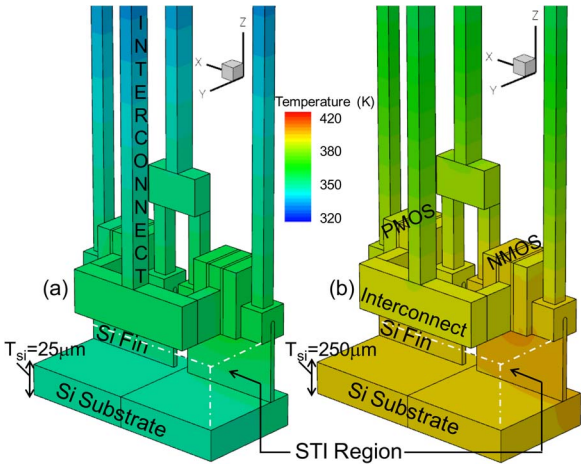

Fig. 12. Figure shows the rise in temperature along the bulk FinFET inverter (single stage) for two different cases (a) $T_{\rm Si} = 25$ μm and (b) $T_{\rm Si} = 250$ μm.

heat flux through the back side of the chip was insensitive to $T_{\rm Si} = 950$ μm; however, it increases with the interconnect height for $T_{\rm Si} = 250$ μm case as shown in Fig. 12. Fig. 13 shows a significant difference in temperature distribution across the inverter stage for $T_{\rm Si} = 250$ μm and $T_{\rm Si} = 25$ μm. Overall, Figs. 7–13 show that there is no difference in the self-heating behavior in SOI and bulk FinFETs. This further supports the motivation for a better approach of modeling thermal behavior in these nanoscale devices.

C. Impact of Layout and Material's Thermal Parameters

Fig. 13 shows that the interconnect metal thickness ($\sim 3 \times \lambda$) and its thermal conductivity have a significant impact on the self-heating behavior. Increasing (decreasing) the interconnect

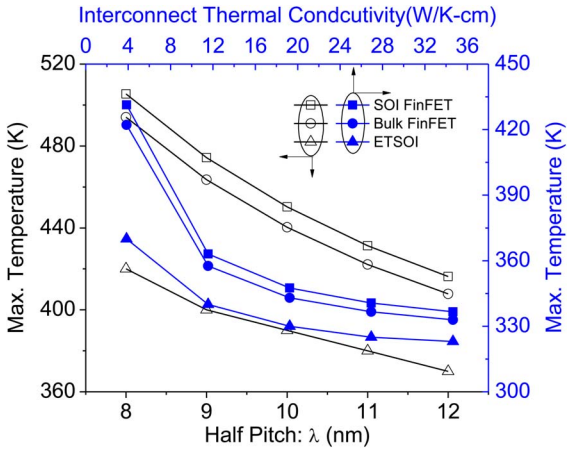

Fig. 13. Impact of interconnect half pitch (lambda) and interconnect thermal conductivity on the self-heating behavior of ETSOI and SOI and bulk FinFETs.

dimensions improves (degrades) the thermal performance due to lower (higher) thermal resistance. Moreover, increasing the interconnect metal's thermal conductivity reduces the thermal resistance and improves the cooling conditions, which eventually leads to a significantly relaxed temperature rise. It is worth pointing out that lattice temperature was significantly relaxed ($\Delta T \leq 10$ K) when the interconnect thermal conductivity was equivalent to carbon nanotube (CNT)-like material ($\sim$35 W/K $\cdot$ cm) [25]. This could be a strong motivation toward replacing the interconnect metal by CNT-like high-thermal-conductivity materials for a robust thermal management in nanoscale nonplanar CMOS. However, this has a penalty of increased process complexity required to reduce the intrinsic interface resistance associated with CNT. For example, a graphite capping layer may be required between the metal silicide and the CNT interconnect/via in order to reduce the interface resistance, as has been reported recently [35].

Fig. 14 shows the impact of ILD thermal conductivity and BOX thickness on the self-heating behavior. Increasing the ILD's thermal conductivity slightly relaxes the rise in lattice temperature. This is due to the fact that increasing ILD thermal conductivity improves thermal coupling of ILD material with metal interconnects, which eventually reduces the effective thermal resistance between the heat source and the heat sink. This further gives us a motivation toward the requirement for higher granularity in the lumped element electrothermal model. On the other hand, due to a very weak thermal coupling between the heat sink and the active region through BOX region, improving the BOX material's thermal conductivity has no impact on the self-heating behavior contrary to the results presented earlier [21], [22].

D. Parameters Insensitive to Thermal Behavior

Before we discuss further, it is worth mentioning that the following have no significant impact on the self-heating behavior of both the FinFET and ETSOI devices (data not shown here): 1) BOX thickness; 2) ILD thickness; 3) active area pitch; 4) gate oxide thickness; and 5) epitaxial (raised S/D) thickness. BOX thickness has a negligible impact due to the significantly lower thermal coupling between the power source (active Si

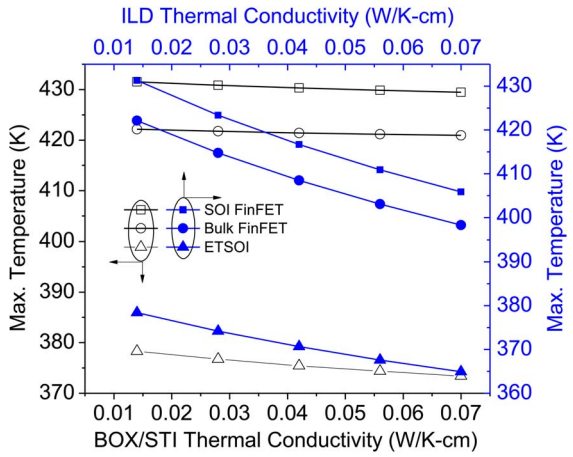

Fig. 14. Impact of BOX's and ILD's thermal conductivities on the self-heating behavior of ETSOI and SOI and bulk FinFETs.

fin) and the heat sink connected at the back side of Si body via BOX. Gate oxide has almost a negligible impact on self-heating effects because of its extremely low thermal resistance (due to its physical thickness) compared to that of metal interconnects.

V. Modified Modeling Framework

Based on our understanding of heat flux paths, interregion thermal coupling, and various key contributors toward the self-heating behavior, a thermal resistance network is derived by the following: 1) discretizing the device into a finer mesh of resistances along the dominant heat flux paths within the device; 2) considering the 3-D nature of device and associated heat flux moving out of the device; and 3) thermal coupling between adjacent regions.

A. Building Blocks

The device is divided into sections where each section of the device (fin, channel, gate, source, drain, spacer, and interconnects) is further subdivided into smaller elements (i.e., "Block," "Ch," and "Pad"). Fig. 15(a) shows the block element, which models the nonchannel regions of the fin, the gate, and spacers. R_1, R_3, and R_5 account for the heat flux path via the BOX and the Si body (bulk Si). R_2 and R_4 model the path along the length of the element. The other $R_{\rm xy}$ resistances model the lateral heat conduction paths and serve to couple the adjacent regions via the ILD. Moreover, Fig. 15(b) shows the channel element (Ch) used for modeling the heat conduction through a channel region. Finally, Fig. 15(c) shows contact pad element (Pad), which models the gate, source, and drain contact pads. R_0 models the heat flux path from fin to pad. R_i accounts for the heat flux path to interconnects through the via, and R_b models the heat flux path via BOX and the Si body (bulk Si). R_1 and R_2 resistances model lateral heat conduction paths for coupling of pads to adjacent fins. In addition to the heat flux paths modeled by the block element, this model adds $R_{\rm ox}$ for the additional heat flux path through the gate oxide. The parameters of the nominal FinFET device are presented in Table I. Various thermal resistances for the basic building blocks of the model mentioned earlier are derived in the Appendix. A complete 3-D representation of the thermal model used for various FinFET architectures is shown in Fig. 16.

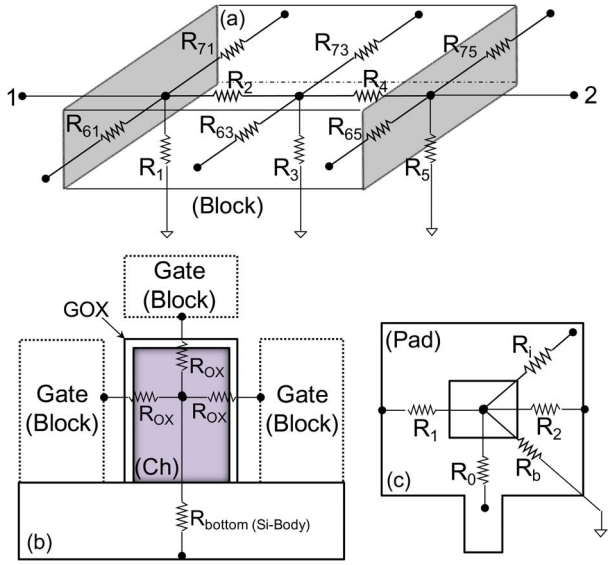

Fig. 15. Overall approach for the thermal-resistance-network-based model for electrothermal simulations. (a) Block element of the model (Block). (b) Channel element (Ch). (c) Pad element (Pad).

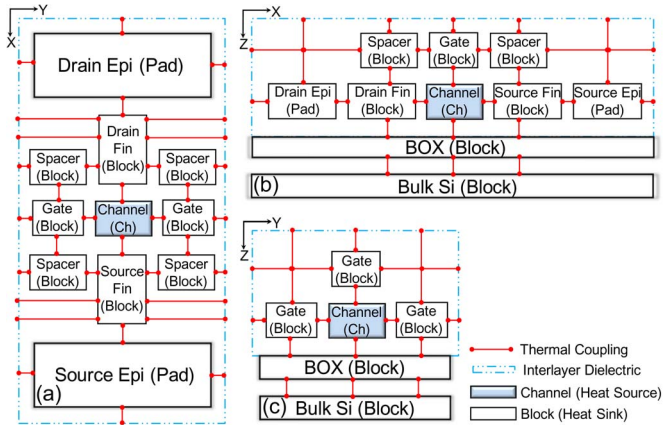

Fig. 16. Complete 3-D representation of the thermal model used for various FinFET architectures.

B. Heat Source and Boundary Conditions

Joule heating (near the drain end of the channel) and classical heat diffusion are considered for computing the total rise in lattice temperature using the relation $\nabla(\lambda\nabla T) = -\eta$, where λ is the thermal conductivity of various heat flux paths (given in Table I); heat generated (η) is approximated from the product of the current density (J) and the electric field (E). For this study, J and E values where extracted from 3-D TCAD simulations. Isothermal boundary conditions with an $ambient\ temperature = 300$ K (outside of the chip) is considered.

C. Validation

Fig. 17 shows that the model derived from the proposed framework gives an excellent fit with the predictions made from

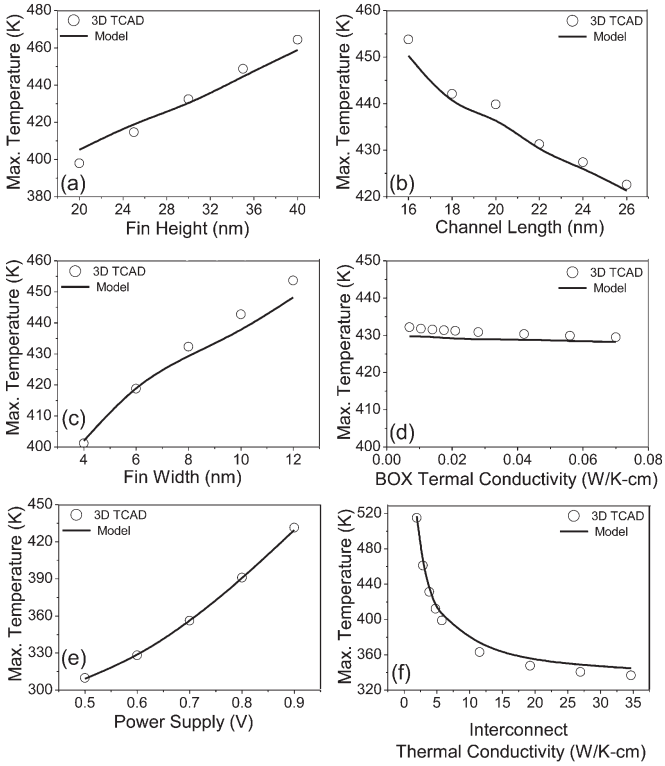

Fig. 17. Figure shows matching of model predictions with TCAD data without any fitting parameter. This validates the accuracy of the proposed modeling framework.

TABLE II
INFLUENCE OF KEY DEVICE/TECHNOLOGY/MATERIAL PARAMETERS OVER SELF HEATING BEHAVIOR, DERIVED FOR TWO DIFFERENT CASES: (A) WHEN CHANGE IN ELECTRICAL CONDITIONS WERE CONSIDERED AND (B) SOLE IMPACT OF THERMAL BOUNDARY CONDITIONS

Parameters	*Impact including change in electrical conditions*	*Sole impact of Thermal Boundary Conditions*
K_M	$\uparrow K_M \rightarrow \downarrow\downarrow T_{MAX}$	$\uparrow K_M \rightarrow \downarrow\downarrow T_{MAX}$
λ	$\uparrow \lambda \rightarrow \downarrow T_{MAX}$	$\uparrow \lambda \rightarrow \downarrow T_{MAX}$
H_{FIN}	$\downarrow H_{FIN} \rightarrow \downarrow T_{MAX}$	$\downarrow H_{FIN} \rightarrow \downarrow T_{MAX}$
H_{Box}	$\downarrow\uparrow T_{BOX} \rightarrow \bullet\ T_{MAX}$	$\downarrow\uparrow T_{BOX} \rightarrow \bullet\ T_{MAX}$
K_{BOX}	$\downarrow\uparrow K_{BOX} \rightarrow \bullet\ T_{MAX}$	$\downarrow\uparrow K_{BOX} \rightarrow \bullet\ T_{MAX}$
W_{FIN}	$\downarrow W_{FIN} \rightarrow \downarrow T_{MAX}$	$\uparrow W_{FIN} \rightarrow \downarrow T_{MAX}$
K_{ILD}	$\uparrow K_{ILD} \rightarrow \downarrow T_{MAX}$	$\uparrow K_{ILD} \rightarrow \downarrow T_{MAX}$
L_G	$\downarrow L_G \rightarrow \uparrow T_{MAX}$	$\downarrow L_G \rightarrow \bullet T_{MAX}$

TCAD (and summarized in Table II) without including any fitting parameter.

VI. TRIGATE VERSUS TALL-FIN FINFETS

This section investigates the self-heating behavior of some other FinFET device architectures using our derived model and compares the same with TCAD-derived predictions.

Fig. 18 compares three different device configurations, i.e., (a) trigate FinFET [Aspect Ratio $(AR) = 1$ with $W_{\mathrm{FIN}} = 30$ nm, (b) tall-fin $(AR = 7)$ FinFET with fin volume conserved, and (c) tall-fin $(AR = 7)$ FinFET with fin-to-gate interface area conserved. Configuration "b" keeps the thermal resistance along the length of the fin the same as in the trigate FinFET—configuration "a." This allows us to investigate the impact of the other conduction path, i.e., from the channel to the gate contact (via the gate oxide + gate metal). Configuration "c" keeps the thermal resistance from the channel to the gate contact the same as in the trigate FinFET and allows us to study the effect of the other conduction paths, i.e., along the length of the channel. Overall, Fig. 18 shows that the trigate architecture has a better thermal performance in comparison to both the tall-fin configurations, which is attributed to increased Si volume underneath the active fin region or hot spot. This helps in dumping most of the heat into the Si body in a similar fashion as it does for planar bulk MOS devices. It is worth pointing out that this behavior is in a good agreement with the predictions made from TCAD.

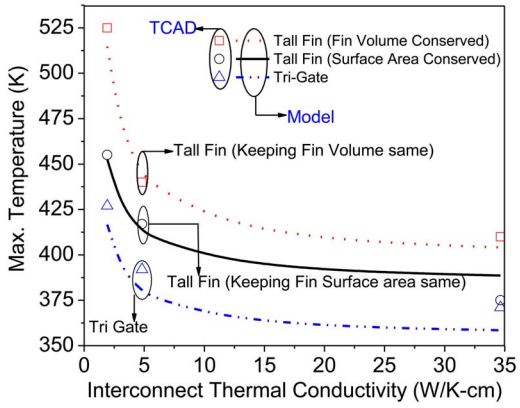

Fig. 18. Self-heating behavior predicted by the proposed model for trigate and tall-fin architectures on bulk and SOI substrates.

VII. CONCLUSION

We have studied the thermal failure of FinFET devices under nominal operating conditions. Our work clearly establishes the fact that, due to a huge thermal resistance contributed by the Si body and the 3-D topology of Si substrate in bulk FinFET structures, there is no difference in the thermal behavior of bulk and SOI FinFET devices. Trigate FinFET devices and planar ETSOI devices were found to have better thermal performance compared to various tall-fin FinFET (bulk/SOI) architectures. CNT-like high-thermal-conductivity materials for interconnects were found to be the key requirement to resolve the thermal issues in these nanoscale CMOS technologies. The importance of thermal boundary conditions is discussed. Our results demonstrate that, in order to build a 3-D thermal resistance network for FinFET-like devices, proper knowledge of various heat flux paths and thermal coupling between the various regions or blocks must be considered. Based on this knowledge, a new framework is proposed in this paper for accurate electrothermal modeling of nanoscale FinFET devices. This modified model takes into account the 3-D nature of the device and includes the possible heat flux paths and necessary thermal coupling between the different regions/blocks of the device. It was found that scaling of all the layout/technology parameters does not have the same impact on the self-heating behavior, i.e., only a few parameters in BEOL have the maximum impact. Based on our investigations, a design guideline is extracted and summarized for robust thermal management.

APPENDIX

Various thermal resistances for the basic building blocks of the model mentioned in Section V are derived in this section.

Drain/Source, Fin (Blocks):

$$R_1 = \frac{\frac{H_{\mathrm{BOXeff}}}{4\times k_{\mathrm{BOX}}} + \frac{1}{\alpha_{\mathrm{eff}}}}{W_{\mathrm{fin}} \times L_{\mathrm{finelement}}}(\mathrm{SOI})$$

$$R_1 = \frac{\frac{H_{\mathrm{BOXeffbulk}}}{4\times k_{\mathrm{BOX}}} + \frac{1}{\alpha_{\mathrm{eff}}}}{W_{\mathrm{fin}} \times L_{\mathrm{finelement}}}(\mathrm{Bulk})$$

$$R_2 = \frac{L_{\mathrm{finelement}}}{2 \times k_{\mathrm{finSi}} \times W_{\mathrm{fin}} \times H_{\mathrm{fin}}}$$

$$R_4 = \frac{L_{\mathrm{finelement}}}{2 \times k_{\mathrm{finSi}} \times W_{\mathrm{fin}} \times H_{\mathrm{fin}}}$$

$$R_3 = \frac{\frac{H_{\mathrm{BOXeff}}}{2\times k_{\mathrm{BOX}}} + \frac{1}{\alpha_{\mathrm{eff}}}}{W_{\mathrm{fin}} \times L_{\mathrm{finelement}}}(\mathrm{SOI})$$

$$R_3 = \frac{\frac{H_{\mathrm{BOXeffbulk}}}{2\times k_{\mathrm{BOX}}} + \frac{1}{\alpha_{\mathrm{eff}}}}{W_{\mathrm{fin}} \times L_{\mathrm{finelement}}}(\mathrm{Bulk})$$

$$R_5 = \frac{\frac{H_{\mathrm{BOXeff}}}{4\times k_{\mathrm{BOX}}} + \frac{1}{\alpha_{\mathrm{eff}}}}{W_{\mathrm{fin}} \times L_{\mathrm{finelement}}}(\mathrm{SOI})$$

$$R_5 = \frac{\frac{H_{\mathrm{BOXeffbulk}}}{4\times k_{\mathrm{BOX}}} + \frac{1}{\alpha_{\mathrm{eff}}}}{W_{\mathrm{fin}} \times L_{\mathrm{finelement}}}(\mathrm{Bulk})$$

$$R_{61} = \frac{W_{\mathrm{pad}} - W_{\mathrm{fin}}}{8 \times k_{\mathrm{ILD}} \times L_{\mathrm{finelement}} \times H_{\mathrm{fin}}}$$

$$R_{63} = \frac{W_{\mathrm{pad}} - W_{\mathrm{fin}}}{4 \times k_{\mathrm{ILD}} \times L_{\mathrm{finelement}} \times H_{\mathrm{fin}}}$$

$$R_{65} = \frac{W_{\mathrm{pad}} - W_{\mathrm{fin}}}{8 \times k_{\mathrm{ILD}} \times L_{\mathrm{finelement}} \times H_{\mathrm{fin}}}$$

$$R_{71} = \frac{W_{\mathrm{pad}} - W_{\mathrm{fin}}}{8 \times k_{\mathrm{ILD}} \times L_{\mathrm{finelement}} \times H_{\mathrm{fin}}}$$

$$R_{73} = \frac{W_{\mathrm{pad}} - W_{\mathrm{fin}}}{4 \times k_{\mathrm{ILD}} \times L_{\mathrm{finelement}} \times H_{\mathrm{fin}}}$$

$$R_{75} = \frac{W_{\mathrm{pad}} - W_{\mathrm{fin}}}{8 \times k_{\mathrm{ILD}} \times L_{\mathrm{finelement}} \times H_{\mathrm{fin}}}$$

$$H_{\mathrm{BOX_{eff}}} = H_{\mathrm{BOX}} + \frac{H_{\mathrm{BottomSi}} \times k_{\mathrm{BOX}}}{k_{\mathrm{BottomSi}}}$$

$$H_{\mathrm{BOX_{effbulk}}} = \frac{(H_{\mathrm{BOX}} + H_{\mathrm{BottomSi}}) \times k_{\mathrm{BOX}}}{k_{\mathrm{BottomSi}}}$$

$$L_{\mathrm{element}} = \frac{L_{\mathrm{fin}}}{N_{\mathrm{fin}}}.$$

Drain/Source/Gate Contacts (Pad):

$$R_1 = \frac{W_{\mathrm{pad}}}{2 \times k_{\mathrm{nonchannelSi}} \times H_{\mathrm{SD}} \times L_{\mathrm{pad}}}$$

$$R_2 = \frac{W_{\mathrm{pad}}}{2 \times k_{\mathrm{nonchannelSi}} \times H_{\mathrm{SD}} \times L_{\mathrm{pad}}}$$

$$R_O = \frac{(L_{\mathrm{pad}} - L_{\mathrm{contact}}) \times 2.3025 \times \log\left(\frac{W_{\mathrm{contact}}}{W_{\mathrm{fin}}}\right)}{2 \times k_{\mathrm{nonchannelSi}} \times H_{\mathrm{SD}} \times (W_{\mathrm{contact}} - W_{\mathrm{fin}})}$$

$$R_i = \frac{H_{\mathrm{contact}}}{k_{\mathrm{contact}} \times L_{\mathrm{contact}} \times W_{\mathrm{contact}}}$$

$$R_b = \frac{H_{\mathrm{BOX_{eff}}}}{k_{\mathrm{BOX}} \times W_{\mathrm{pad}} \times L_{\mathrm{pad}}} + \frac{1}{\alpha_{\mathrm{eff}} \times W_{\mathrm{pad}} \times L_{\mathrm{pad}}}(\mathrm{SOI})$$

$$R_b = \frac{1}{\frac{k_{\mathrm{BOX}} \times (W_{\mathrm{pad}} - W_{\mathrm{fin}}) \times L_{\mathrm{pad}}}{H_{\mathrm{BOX_{eff}}}} + \frac{k_{\mathrm{BOX}} \times (W_{\mathrm{pad}} - W_{\mathrm{fin}}) \times L_{\mathrm{pad}}}{H_{\mathrm{BOX_{effbulk}}}}} + \frac{\alpha_{\mathrm{eff}}}{W_{\mathrm{pad}} \times L_{\mathrm{pad}}}(\mathrm{Bulk}).$$

Channel (Block and Ch):

$$R_{\mathrm{ox}} = \frac{t_{\mathrm{ox}}}{2 \times k_{\mathrm{ox}} \times H_{\mathrm{fin}} \times L_{\mathrm{channel}} + k_{\mathrm{ox}} \times W_{\mathrm{fin}} \times L_{\mathrm{channel}}}.$$

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