Part I: On the Behavior of STI-Type DeNMOS Device Under ESD Conditions

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***Abstract*—We present experimental and simulation studies of shallow trench isolation (STI)-type drain-extended n-channel metal–oxide–semiconductor devices under human body model (HBM)-like electrostatic discharge (ESD) conditions. Physical insight toward pulse-to-pulse instability is given. Both the current (I_{TLP}) and time evolution of various events such as junction breakdown, parasitic bipolar triggering, and the base push-out effect are discussed in detail. Differences between the 2-D and 3-D simulation (modeling) approaches are presented, and the importance of 3-D technology-computer-aided-design-based modeling is discussed. Furthermore, a deeper physical insight toward the base push-out is given, which shows significant power dissipation due of space charge build-up, which is found at the onset of self-heating in the 2-D plane.**

***Index Terms*—Base push-out, charge device model (CDM), charge modulation, current filamentation, drain-extended metal–oxide–semiconductor (DeMOS), electrostatic discharge (ESD), human body model (HBM), input–output (I/O), Kirk effect, laterally diffused metal–oxide–semiconductor (LDMOS), space charge build-up, thermal runaway, transient interferometric mapping (TIM).**

I. Introduction

AGGRESSIVE scaling has resulted in CMOS devices operating below 1 V in sub-100-nm-node technologies. To communicate with the external world, high-voltage (HV) input–output (I/O) devices are required, which can be integrated in the same CMOS process flow. To protect these devices from an electrostatic discharge (ESD) event, dedicated ESD protection devices are used [1]. An accurate modeling of ESD behavior, in these ESD protection and I/O devices, is a critical need for designing robust ESD protection circuits in sub-100-nm-node technologies [1], [2]. With the growing cost of scaled technologies and increased competition in the market, it is also mandatory to reduce the development cycle. One way to do so is to develop accurate presilicon concepts by using technology computer-aided design (TCAD) simulations in order to understand the failure mechanism and to get proper insight of failure levels [3]. The failure of a device under ESD condition has been traditionally linked to the rise of temperature because of self heating, which causes intrinsic carrier concentration higher than background doping [4] and takes the device into a negative differential resistance (NDR) mode [5]. This eventually leads to the onset of filamentation and device failure because of thermal runaway.

The drain-extended n-channel MOS (DeNMOS) is an HV device, which can be easily integrated with a standard CMOS process in sub-100-nm-node technologies. Attributed to a shrinking ESD window, it is very important to design self-protecting I/O devices since the I/O devices may themselves be prone to failure because of an ESD event. The reliability of the DeNMOS device under ESD condition is very critical for its use as an ESD protection device for some HV I/O circuit applications and its use for I/O device applications. However, these devices have been found to be extremely vulnerable to ESD events, and until now, several mechanisms have been proposed for DeNMOS failure [6]–[15].

Work done by Hower *et al.* [6], [7] claimed that a safe operating area (SOA) is a fundamental limiting property of the laterally diffused MOS (LDMOS) devices. Furthermore, their work [8] discussed the device design methodology for the required SOA. However, the discussed methodology does not address ON-resistance (R_{ON}) degradation. It was claimed that these devices will be affected by either electrical or thermal instability, whereas detailed 3-D simulations in this work suggest that both are coupled in nature and advanced drain-extended MOS (DeMOS) devices undergo electrothermal instabilities. Base widening and space charge formation were also observed in these papers [6]–[8], whereas physical insight and its impact on device failure require further investigations. Recent reports [9], [10] claimed that the bipolar-driven snapback causes the failure of LDMOS devices, and they have discussed optimization schemes and hot spot hopping in vertical diffused MOS devices. However, a detailed insight into the filament behavior or hot spot hopping is still missing. Furthermore, the optimization for ESD robustness in these works [9], [10] means giving up on R_{ON}, which again leads to a tradeoff between ESD robustness and the device's nominal operation. Work reported in [11] shows improved ESD robustness of DeNMOS devices by using gate and substrate biasing, whereas the proposed ESD protection implementation does not provide an ESD robust I/O driver. The DeNMOS device is still prone to failure when used as an I/O driver (specifically output driver). Furthermore, the work does not give any detailed insight toward 3-D filamentation and the reported improvement. Recently, it has been proposed that carrier heating in the high field region

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influences saturation drift velocity and impact ionization, which starts a regenerative n-p-n action and causes second breakdown [12]. Results discussed in [12] were obtained through 2-D simulation, and the 3-D filament behavior could not be captured from these studies. In addition, the proposed regenerative n-p-n action in the device was discussed for the charge device model (CDM) time domain (1–2 ns), whereas the device does not get heated within this short interval of time. These simulation studies also show influence in saturation drift velocity at temperatures higher than 1000 K, which is itself sufficient for the onset of filamentation because of NDR and further thermal runaway. The study does not also discuss base push-out behavior. Other studies show that, because of the space-charge-limited current, the peak electric field shifts at drain contact, which causes a regenerative avalanche injection. This again leads to filamentation and device failure [13], [14]. A more detailed 3-D modeling of filamentation has shown that the regenerative turn-on of parasitic n-p-n causes short circuit power dissipation and leads to an enhanced heating and filamentation [15]. However, a complete picture of the transient device behavior during base push-out and the various phases of filamentation based on 3-D simulation studies is still missing.

This paper is the extended version of our previous work [16], which gives a better understanding of various phases of filamentation with a clear and correlated understanding of device failure during the ESD event. In the first part of this paper, we present experimental results and a detailed 2-D simulation study of shallow trench isolation (STI)-type DeNMOS device under ESD conditions. Part I of this paper is arranged as follows: Experimental and 2-D simulation studies are discussed in Section II. Section III concludes the importance of 3-D TCAD simulations in modeling the ESD behavior of DeMOS devices. A new physical insight into the space charge build-up and current discharge is given in Section IV, whereas Section V concludes this paper.

In the second part of this paper, we present a clear and correlated picture on the impact of base push-out, space charge build-up, and regenerative n-p-n action over various phases of filamentation and thermal runaway. Furthermore, we propose a modification in the device layout to achieve improvement $(\sim 2.5\times)$ in failure threshold (I_{T2}). The CDM performance of various devices is also discussed, and the validation of the failure/filamentation model is presented by using detailed transient interferometric mapping studies [17].

II. Experimental and Simulation Results

A thin-gate-oxide DeNMOS device with STI under gate–drain overlap, as shown in Fig. 1, is processed in state-of-art 65-nm-node CMOS technology. This device is realized for 1.8–5-V I/O or HV CMOS applications, and can sustain up to 10 V without any severe reliability concerns. The physical or mask gate length of the realized device was 800 nm, whereas the effective channel length (source/n-well edge) was 200 nm. The lateral width of the STI region was kept at 350 nm, whereas the length of the gate/n-well overlap region was 300 nm, with the drift region length kept at 650 nm. Fig. 2 shows that the device exhibits failure at a very low current (1–1.7 mA/μm), even in the presence of gate bias or source resistance, unlike in [13] and [15]. Oscillations in the moderate current branch

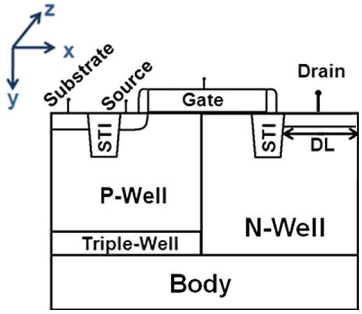

Fig. 1. DeNMOS device under study, showing the one-sided structure (simulated). The actual structure on silicon has folded geometry, where the drain (n-well) region is shared between two fingers.

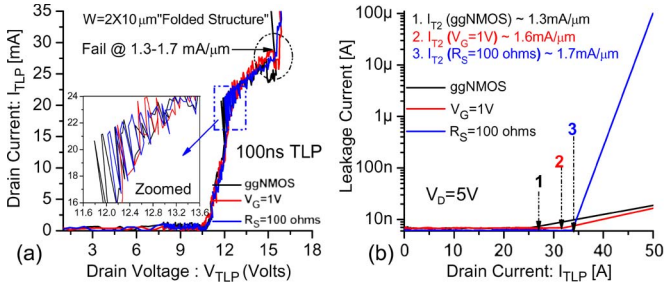

Fig. 2. Various experimental 100-ns (left) TLP and (right) leakage characteristics of the DeNMOS device, failing at early current. Only a small improvement in I_{T2} was observed by using gate bias or source resistance.

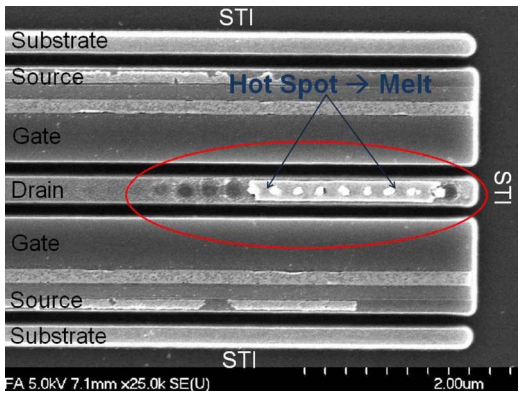

Fig. 3. SEM image of the failed device, showing failure analysis results, which proves catastrophic failure of the device because of filamentation and self heating. The location of filament and hot spot is validated and modeled further through 3-D device simulations.

of transmission line pulsing (TLP) characteristics show two different stable states for the device [inset of Fig. 2(a)], in which one state tries for deep snapback and the other state tries to move into the high-resistance branch. No change in leakage occurs in this regime. Finally, these two states are getting balanced into high-resistance branches, causing device failure. The I–V characteristics are reversible for stress current values up to 90% of I_{T2}.

The failed device was physically characterized using a scanning electron microscope (SEM), which is shown in Fig. 3. The failure analysis result (SEM image) proves a catastrophic failure of the device because of filamentation and self heating at the drain side. It validates the location of the filament and hot spot, which is modeled further through 3-D device simulations.

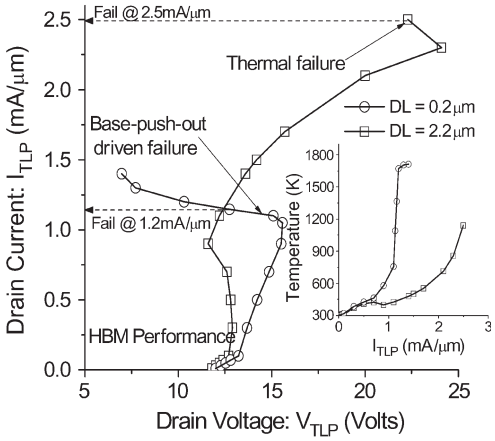

Fig. 4. Simulated (3-D) TLP (HBM) characteristics of the DeNMOS device having different drain DLs. We find that the devices having higher DL survive higher currents.

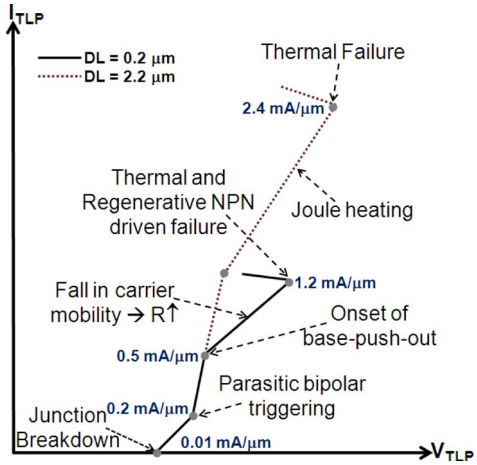

Fig. 5. Approximate TLP characteristics of DeMOS devices having DL $=$ 0.2 μm and DL $=$ 2.2 μm show the device behavior in the different current (per micrometer) regimes.

Fig. 4 shows simulated TLP characteristics for devices having different drain diffusion lengths (DLs). The device having shorter DL (high current density in n-well) leads to an early base push-out and device failure with a deep snapback, whereas the device having longer DL (low current density in n-well) has no base push-out (follows a highly resistive branch) and survives higher currents.

Fig. 5 gives an explanation for the behavior of the two different devices types. The device behavior of the shorter-DL case is discussed here.

A. Junction Breakdown

The initial current flow through the device is because of junction breakdown. Fig. 6 shows current density contours at low current ($\sim$0.1 mA/μm). The maximum fraction of forced current at the drain (collector of n-p-n) terminal moves out through the substrate (base of n-p-n) contact, which proves the dominance of junction breakdown for conduction at low TLP currents. The absence of source (emitter of n-p-n) current in the contours shows that the parasitic bipolar is not yet triggered.

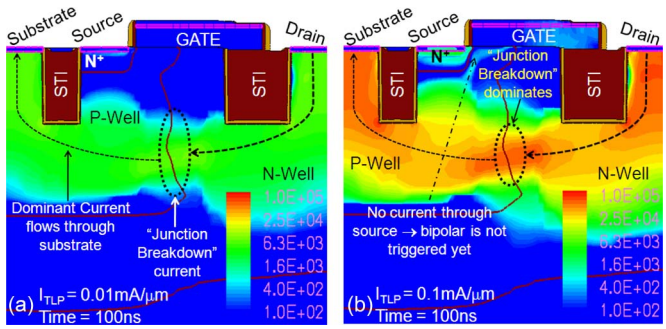

Fig. 6. Conduction current density (in amperes per square centimeter) at (a) $I_D = 0.01$ mA/μm and (b) $I_D = 0.1$ mA/μm. The initial current flow through device is dominated by junction breakdown, whereas the parasitic bipolar is yet not triggered at 0.1 mA/μm.

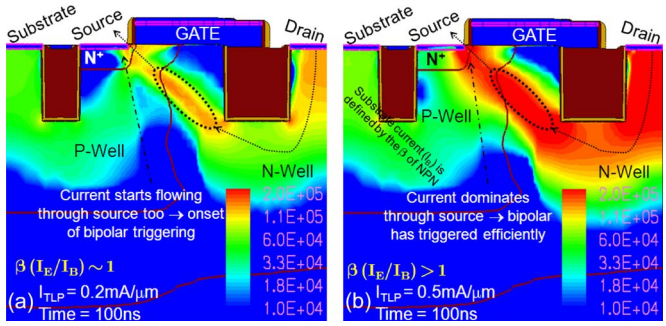

Fig. 7. Conduction current density (in amperes per square centimeter) at (a) $I_D = 0.2$ mA/μm and (b) $I_D = 0.5$ mA/μm. The parasitic bipolar is triggered at 0.2 mA/μm. At higher currents, the base (substrate) current is defined by the β of n-p-n.

B. Bipolar Triggering

Fig. 7 shows the triggering nature of the parasitic bipolar in the DeNMOS device considered for this work. The onset of current flow through the source [Fig. 7(a)] shows that the parasitic bipolar is turned on at moderate currents. At higher currents [Fig. 7(b)], most of the current flows through the emitter (source) of the parasitic bipolar, whereas the base (substrate) current is defined by the β of n-p-n. The slope of TLP characteristics increases at higher current, which is partially because of the fall in carrier velocity (drops the carrier mobility) and due to an increase in the base length at higher currents. Both of these effects (discussed in more detail later) eventually lead to a larger resistance of the bipolar path.

C. Space Charge Formation

Fig. 8 shows the space charge regions near 1) the well junction and 2) drain diffusion, at a moderate current value (0.5 mA/μm). The current evolution of space charge formation (i.e., w.r.t I_{TLP}) is described here. For lower TLP currents ($<$ 0.4 mA/μm), significant space charge builds up at the well junction (loc A). At moderate TLP currents ($\sim$0.5 mA/μm), the space charge concentration decreases (from its peak value) near the well junction and starts increasing (from the zero value) underneath the drain diffusion (loc B). This shift is also denoted as the onset of base push-out throughout this work. As the TLP current increases (0.9–1.1 mA/μm), charge modulation due to excess carriers in the n-well region leads to significant space charge build-up underneath the drain diffusion, whereas

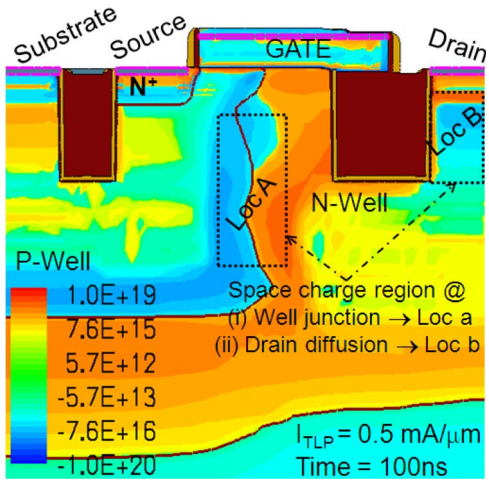

Fig. 8. Space charge contour (in cubic centimeter) at a moderate current level (0.5 mA/μm), showing the impact of carrier modulation and space charge build-up at different locations.

the space charge near the well junction diminishes gradually. Furthermore, we will correlate the change in electric fields at different locations based on the preceding observations and will discuss the development of significantly high electric fields underneath the drain diffusion because of carrier modulation, i.e., base push-out.

D. Base Push-Out

At the onset of base-push-out-driven snapback, devices having shorter and longer DLs behave differently. The devices with smaller DL suffer from high current densities, which drives them into early base push-out, causing thermal failure. The devices with a larger DL assume a high ohmic state until they fail at higher current density without showing a base push-out.[1] Fig. 9 shows the onset and complete base push-out of the DeNMOS device for the case of shorter DL. At lower TLP current (i.e., 0.2 mA/μm), there are high fields only at the n-well/p-well junction, whereas, at moderate currents (i.e., 0.5 mA/μm), the onset of base push-out leads to the development of electric fields under the drain diffusion (N^+) region as well. Furthermore, at higher TLP currents (i.e., 1.2 mA/μm), the high electric field at the junction was washed out and shifted under the drain diffusion, which shows a complete base push-out. Fig. 9 shows the current ($I_{\rm TLP}$) dependence of the base push-out behavior, whereas the transient nature of this interesting behavior is also studied in the latter part of this work.

E. Impact Ionization and Base Length Modulation

Fig. 10(a) and (b) shows impact ionization contours at moderate and higher TLP currents, i.e., at the onset of base push-out and after significant space charge build-up (i.e., high field formation under drain diffusion), respectively. At moderate TLP currents, the well junction has the strongest electric field and, thus, the impact ionization [Fig. 10(a)], whereas, due to significant space charge build-up or very high electric field under drain diffusion, the impact ionization peak shifts toward the drain diffusion at higher TLP currents [Fig. 10(b)]. Prior to device failure (< 1.2 mA/μm), the shifting of the peak impact ionization location affects the device behavior (i.e., bipolar triggering) in the following way; when the peak electric field (or impact ionization) occurs near the well junction, the parasitic bipolar has a smaller base length ($L_{\rm B1}$), which increases further as the peak shifts away from the well junction ($L_{\rm B2}$, i.e., toward drain diffusion). This leads to degradation in the bipolar turn-on (β decreases with increase in base length) after the onset of base push-out, which eventually leads to a larger ON-resistance (evident in Fig. 5) as the $I_{\rm TLP}$ increases beyond moderate current levels.

The observed TLP behavior [Fig. 2(a)] of the investigated folded double-finger structure (as clear from SEM image) can be explained as follows: The drain diffusion is shared between two fingers. Initially, only one finger is turned on. At a moderate current, this finger moves into the base push-out regime, which causes a regenerative n-p-n action. In this voltage regime, the second finger might trigger as well, which reduces the overall current density. In this case, both fingers are operating in a state without base push-out exhibiting lower absolute resistance but higher differential resistance (similar to the case of larger DL). This is seen as a bistable state in the I–V characteristics. At higher currents, the device stabilizes into a high resistance state because of lower current density.

At this stage, it is worth pointing out the differences between the DeMOS device in sub-100-nm-node technology, DeMOS/LDMOS devices realized in the same technology with higher feature sizes, and the devices operating at very high voltages (40–100 V). Fundamentally, there is no difference in all these devices in terms of their bipolar triggering or device failure due to base push-out. However, higher feature size devices usually have a longer drift region, which gives rise to a higher slope in the pulsed I–V characteristics due to their higher $R_{\rm ON}$. Parasitic n-p-n may not trigger efficiently in these devices due to the larger base (source/n-well) length of parasitic n-p-n. Lower doping density in the drift region leads to an early onset of charge modulation, i.e., base push out, which can eventually be attributed to the lower ESD failure currents.

III. On the Differences Between 2-D and 3-D Modeling Approach

TCAD simulations are used by various groups in the past in order to model the ESD behavior of various devices. Since grounded gate n-channel MOS and silicon-controlled-rectifierlike structures fail purely due to excess temperature rise (at drain/anode) and thermal runaway at very high TLP currents, they can easily be modeled at high current densities using 2-D device simulations, which has been greatly used as a strong tool in the past. However, we found that devices such as DeMOS or, in general, devices that suffer from heavy charge modulation at early currents cannot be modeled using

[1]In the past, it was reported that the carrier heating in the high field region influences the saturation drift velocity and enhances impact ionization. This causes higher impact-ionization-generated carriers, which flow (holes for parasitic n-p-n) through the substrate. Excess holes in the substrate trigger the parasitic n-p-n device faster, causing a deeper snapback. This type of regenerative carrier generation and bipolar triggering was named *regenerative n-p-n action*. Furthermore, the deep snapback leads to a short circuit power dissipation, which was reported as the dominant cause of second breakdown [12], [13].

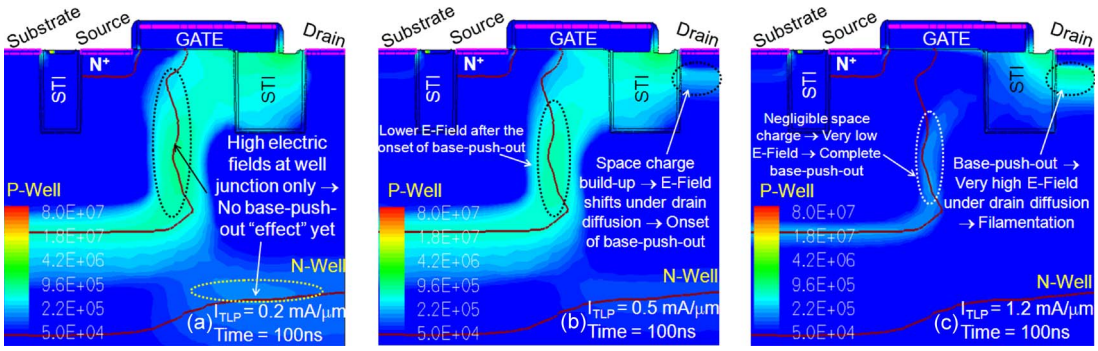

Fig. 9. Electric field at (a) $I_D = 0.2$ mA/μm, (b) $I_D = 0.5$ mA/μm, and (c) $I_D = 0.5$ mA/μm. Also shown is the onset of base push-out at 0.5 mA/μm. After base push-out, there is a significantly high electric field under drain (n^+) contact.

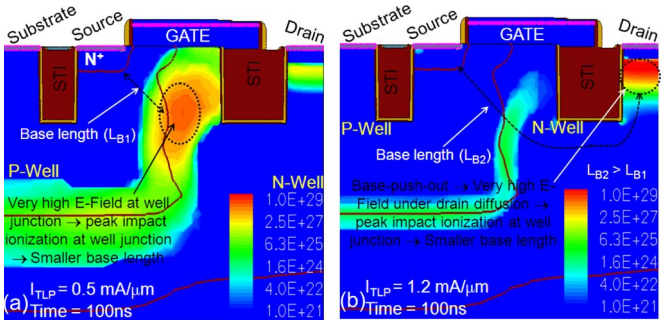

Fig. 10. Impact ionization contours ($cm^{-3}s^{-1}$) at (a) $I_{TLP} = 0.5$ mA/μm and (b) $I_D = 1.2$ mA/μm, showing that base push-out leads to increase in effective base length, which eventually degrades the parasitic bipolar.

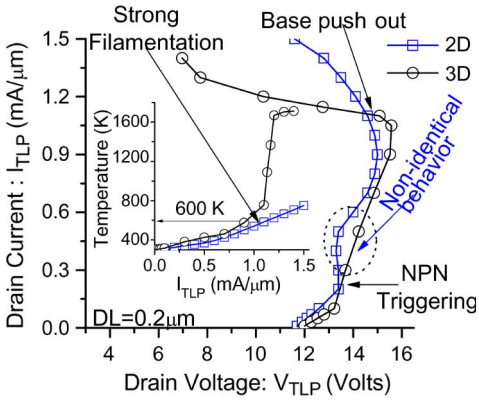

Fig. 11. Comparison of the 2-D and 3-D TLP characteristics of the DeNMOS device with DL = 0.2 μm. Also shown is nonidentical 2-D versus 3-D behavior, which signifies the need for 3-D device modeling of DeMOS devices.

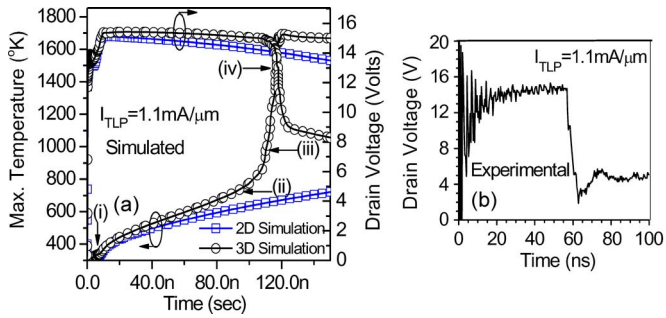

Fig. 12. (a) Comparison of the 2-D and 3-D transient characteristics of the DeNMOS device with DL = 0.2 μm, extracted from 100 ns (HBM) of ESD stress. (b) Measured transient characteristics (drain voltage w.r.t. time), which matches well with the simulated (3-D) characteristics and validates the 3-D modeling approach.

2-D device simulations. This section signifies the importance of 3-D TCAD while modeling DeMOS-like devices.

Fig. 11 compares the 2-D and 3-D TLP characteristics of a DeNMOS device with DL = 0.2 μm. It shows a distinct 2-D and 3-D behavior, which is attributed to the presence of charge modulation at lower TLP currents. Both characteristics can be differentiated as follows: 1) Nonidentical characteristics at moderate current (0.5 mA/μm) show the nonuniform nature of n-p-n triggering. Pulse-to-pulse instability can also be explained using Fig. 1 as follows: When the device triggers uniformly (2-D simulation), it leads to a snapback state, whereas it is actually driven into a high resistance state during nonuniform n-p-n triggering across the device width (3-D simulation). 2) At higher TLP currents ($\sim$1.1 mA/μm), the onset of filamentation[2] and thermal runaway leads to a strong snapback; however, lack of thermal runaway and filamentation in the 2-D plane (i.e., 2-D simulations) drives the device into a soft snapback state. 3) The onset of filamentation and thermal runaway at very low temperature (600 K) signifies the leading role of base push-out on the device failure (inset Fig. 11) mechanism.

Fig. 12(a) compares the transient behavior of 2-D and 3-D DeNMOS devices, which are extracted from 100 ns (HBM) of ESD stress. This is evident from the figure that 2-D device simulation does not lead to a deep snapback, which is due to base-push-out-driven filamentation. On the other hand, the 3-D device simulation captures the deep snapback and very fast temperature rise due to filamentation. Fig. 12(b) shows the measured transient characteristics of the DeNMOS device (drain voltage w.r.t. time), which matches well with the simulated (3-D) characteristics and validates the discussed 3-D modeling approach. The following events occur during the 100-ns duration: 1) parasitic bipolar triggering; 2) space charge build-up and its discharge; 3) localized charge modulation, which causes the onset of filamentation; and 4) thermal runaway. It is evident from the transient characteristics that parasitic bipolar triggers at 5–10 ns, whereas the thermal runaway and device failure occurs at 80–100 ns, which proves that the parasitic bipolar triggering is not the dominant cause of device failure. The time at which deep snapback occurs depends on the pulsed current after charge modulation or base push-out. Increasing the current further causes faster filamentation, which eventually

[2]Filamentation is discussed in more detail in Part II of this paper.

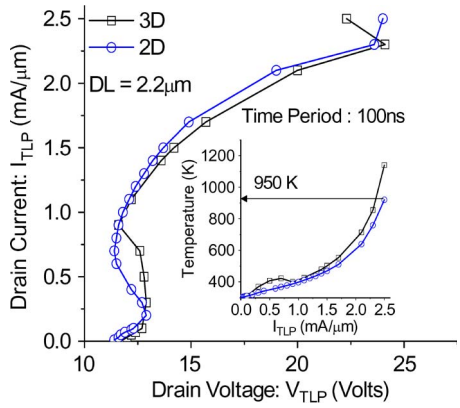

Fig. 13. Comparison of the 2-D and 3-D TLP characteristics of the DeNMOS device with DL $= 2.2$ μm, showing almost-identical 2-D versus 3-D behavior, which, in turn, shows that the devices that survive base push-out can be modeled using 2-D device simulations.

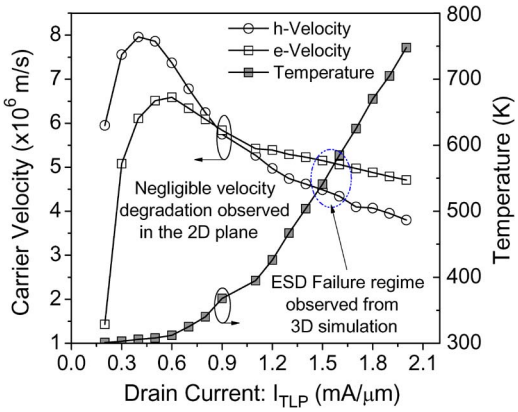

Fig. 14. Variation of carrier velocity and maximum temperature with respect to drain current. No significant drop in carrier velocity was observed from 2-D simulations for higher current at which the device fails.

leads to an even earlier snapback with respect to the pulse time. Furthermore, the depth of the snapback (ΔV_D) depends on the width of the device under stress, i.e., higher width leads to a deeper snapback. In a positive feedback system, it is worth understanding the sequence of these events. In these devices, snapback is due to current filamentation, i.e., current filamentation occurs first, which eventually leads to a deep snapback and failure. Three-dimensional simulations and experiments show a slight difference in the snapback time and ΔV_D due to the slightly different stress currents (abs. $I_{\rm TLP}$) and width used in simulations, compared to the experimental devices.

Fig. 13 shows almost identical 2-D and 3-D TLP characteristics of the DeNMOS device with DL $= 2.2$ μm, which is attributed to the absence of base push-out. This eventually leads to a higher value of critical temperature (950 K) for the onset of filamentation and thermal runaway (inset of Fig. 13) and provides a higher value of failure currents. It is worth mentioning that the nonidentical 2-D versus 3-D behavior at lower TLP current (bipolar-driven snapback region) provides a signature of pulse-to-pulse instability, which may also occur in the modified (device with higher DL) DeNMOS device.

It can be concluded from the preceding discussion that those devices that suffer from base push-out need 3-D device simulations, whereas the devices (parasitic bipolar type) that survive the base push-out can easily be modeled using 2-D device simulations.

IV. Two-Dimensional Device Modeling and Onset of Filamentation

Before we start discussing about failure mechanism, it is important to understand the definition of failure threshold and thermal boundary conditions in this work. Failure threshold (I_{T2}) is the forced TLP current at which the maximum temperature inside the device goes above 1500 K. We choose 1500 K since it is very close to the melting point of Si (i.e., 1687 K) in order to compare the relative behavior of I_{T2} for various device configurations. To achieve proper thermal boundary conditions, we extended the device boundaries by 5 μm and defined 300 K of thermal boundary condition at the surroundings of the device. The extension was done in such a way that it does not affect the electrical behavior of the device. We choose 5 μm since thermal diffusion (in Si) length for 100 ns (HBM) is 3.3 μm [3].

Fig. 14 shows the carrier velocity and the corresponding temperature with respect to the forced TLP current. The carrier velocity in the high-field region was extracted from 2-D device simulations. As claimed in [12], carrier velocity significantly drops down (in the 2-D plane) at the failure levels. In other words, the device has failed because of the drop in saturation drift velocity in the 2-D plane, which further leads to a regenerative n-p-n action and current filamentation in the 3-D structure. We found that there is no significant fall in carrier drift velocity (observed in the 2-D plane) at higher currents, which may lead to regenerative action and device failure. This means that carrier velocity plays no role in the current filamentation. On the other hand, a fall in carrier velocity (or carrier mobility) affects the bipolar resistance, leading to a higher ON-resistance at higher TLP currents, which is evident from Fig. 4.

The studies done in previous DeNMOS works had not modeled the transient behavior of the device during 100 ns of the HBM event. The proposed model in [15] shows device failure at the onset of bipolar triggering (bipolar snapback). It was proposed that bipolar snapback (because of regenerative n-p-n action) leads to dissipation of the energy stored in the junction capacitor, which eventually leads to a filament formation. We calculated that the energy stored in the junction capacitor is in the range of picojoules, which is not sufficient for device failure. All these contradictions point to a need for understanding the transient behavior of the device at the failure current.

Fig. 15(a)–(c) shows the device behavior at the failure current having a junction breakdown at 0.5 ns, the onset of parasitic bipolar triggering at 2 ns, and efficient bipolar triggering at 5 ns, respectively. Furthermore, after 20 ns, as shown in Fig. 16, at higher currents, the onset of base push-out causes a significantly higher space charge build-up in the device.

It was found that the build-up of a space charge region leads to the formation of very high capacitance during the first 40 ns, which stores a very high amount of energy (unlike the energy stored across the junction capacitance presented in [15]). The stored energy was dissipated in silicon, which significantly exceeds the $V \cdot I$ component, as shown in Fig. 17. This phenomenon was not observed at lower currents, i.e., before base push-out.

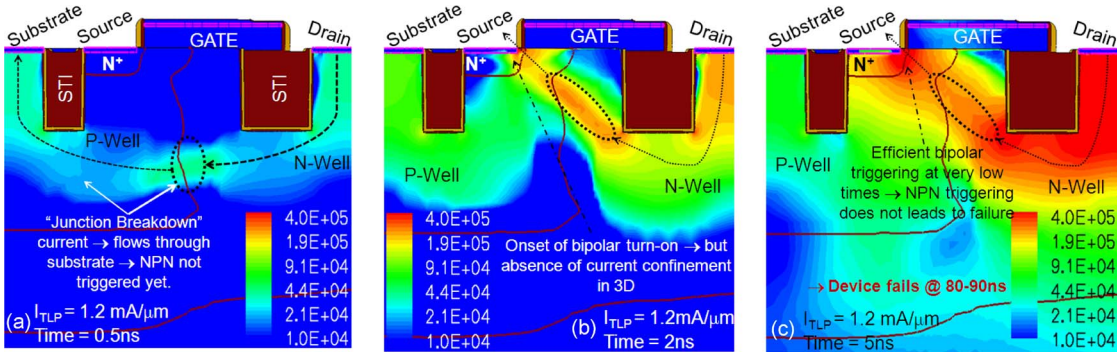

Fig. 15. Conduction current density (in amperes per square centimeter) at time (a) 0.5, (b) 2, and (c) 5 ns for failure current. The junction breakdown happens at 0.5 ns, whereas the parasitic bipolar is triggered at 5 ns.

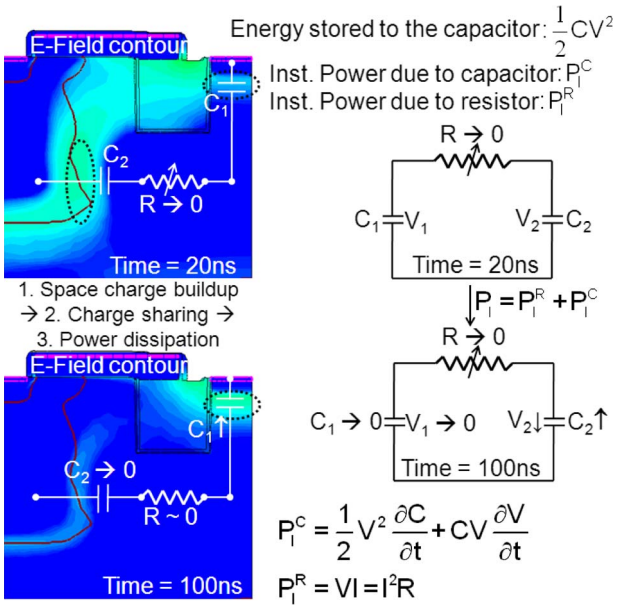

Fig. 16. Model for space charge build-up and further discharge, which causes high instantaneous power dissipation during base push-out. It also shows the transient nature of the base push-out behavior.

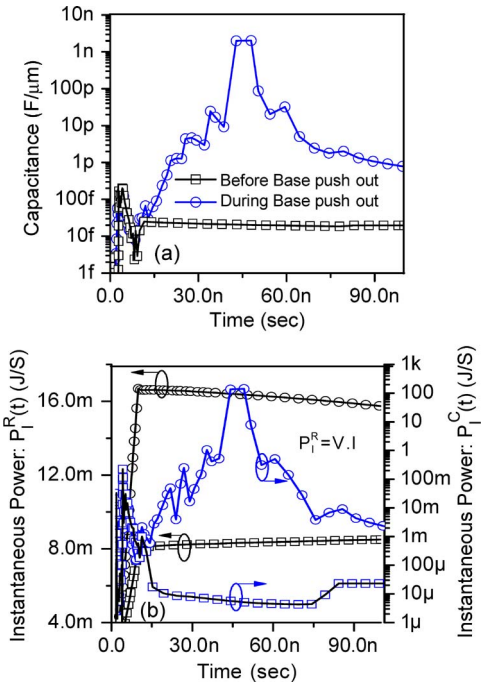

Fig. 17. Capacitance (t) and instantaneous power dissipated (stored) by various parasitic (electrical) components before and after base push-out.

V. Conclusion

We have shown that the parasitic bipolar triggers at very low currents and earlier in time, whereas the device fails at higher TLP currents and at a later time. This gives an indication that the triggering of parasitic n-p-n is not the dominant cause of DeNMOS failure. Pulse-to-pulse instability was found to occur because of the triggering of one finger or two fingers, which gives rise to an absolute current density in the triggered finger (one-finger-triggering mode), causing an early charge modulation in the 2-D plane leading to a snapback. The differences between the 2-D and 3-D TLP characteristics and the importance of 3-D simulations for the device that suffers from early charge modulation are discussed. In the DeMOS, a strong charge modulation (i.e., base push-out) was found to occur, which degrades the ON-resistance of the parasitic bipolar and increases the slope of the TLP characteristics. Additionally, a high space charge build-up during the base push-out contributes to electrothermal instability, which gives rise to an early filamentation/failure under HBM condition.

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