A Novel Bottom Spacer FinFET Structure for Improved Short-Channel, Power-Delay, and Thermal Performance

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***Abstract*—For the first time, we propose a novel bottom spacer fin-shaped field-effect-transistor (FinFET) structure for logic applications suitable for system-on-chip (SoC) requirements. The proposed device achieved improved short-channel, power-delay, and self-heating performance compared with standard silicon-on-insulator FinFETs. Process aspects of the proposed device are also discussed in this paper. Physical insight into the improvement toward the short-channel performance and power dissipation is given through a detailed 3-D device/mixed-mode simulation. The self-heating behavior of the proposed device is compared with standard FinFETs by using detailed electrothermal simulations. The proposed device requires an extra process step but enables smaller electrical width for self-loaded circuits and is an excellent option for SoC applications.**

***Index Terms*—Bulk fin-shaped field-effect transistor (FinFET), electrothermal, fin-shaped field-effect transistor (FinFET), self-heating, short-channel performance, spacer, width quantization.**

I. Introduction

FIN-SHAPED field-effect transistors (FinFETs) are being considered as preferred devices for the sub-22-nm-node CMOS technologies [1], [2]. Multigate FinFET devices have shown excellent scalability and improved logic performance, as well as improved analog and mixed-signal circuit performance in sub-32-nm-node CMOS technologies [3]–[5] compared with planar bulk CMOS transistors. Body-tied or bulk FinFET structures have also received significant interest from various groups [6], [7]. Bulk FinFETs are found to have less defect density and process complexity along with several other advantages such as better heat dissipation capability and lower cost [7]. Bulk FinFETs can be fabricated with an extra implant to increase the doping in the inactive fin region to suppress the source-to-drain coupling through the substrate [8]. Although the FinFET devices show excellent promise, they still suffer from issues such as process complexity, additional parasitic capacitances due to the nonplanar nature of the structure, and width quantization effects. Width quantization effect is of particular concern for analog circuit applications [9]. It is also an important concern for logic as well as static random-access-memory (SRAM) applications, where self-loading is dominant. For example, increasing the active width of the device increases the current and the load capacitance in the same ratio, thereby making the delay invariant. The channel width of a single fin device is restricted by the height of the fin H_{Fin}. The channel width for a multigate device is given as follows:

$$W \sim 2H_{\mathrm{Fin}} + W_{\mathrm{Fin}} \tag{1}$$

where W_{Fin} is the fin width. For a device having $H_{\mathrm{Fin}} = 60$ nm and $W_{\mathrm{Fin}} = 10$ nm, the effective channel width can be calculated [from (1)] as 130 nm. For technologies below the 20-nm channel length, such a high channel width only increases the static and dynamic power dissipation (due to the higher currents) for a given value of delay.

In this paper, for the first time, we propose a novel bottom spacer (BS) FinFET structure that solves the problem associated with the width quantization effect. We found significant improvement in terms of static and dynamic power consumption without compromising on the circuit performance. The proposed device exhibits a much better short-channel behavior as compared with the standard FinFET structure, and, hence, it is better scalable for channel lengths below 20 nm. The proposed device can be fabricated by using a standard silicon-on-insulator (SOI) FinFET process along with an extra anti-punchthrough implant similar to the one used for a bulk FinFET [8] device. The BS FinFET can also be fabricated in a standard bulk FinFET process without an extra mask. Although the device needs an extra process step, it is an excellent option for system-on-chip (SoC) applications, where a higher channel width is required for the analog, and a lower channel width is essential for digital functions. In the BS FinFET, while the electrical width is decreased, the heat is still dissipated over the entire fin height and metal gate, which, therefore, reduces the power density and, hence, self-heating. Relaxed heating eventually leads to lower I_{ON} degradation.

This paper is organized as follows. Section II explains the proposed device structure, process steps for the novel BS, and the associated 3-D simulation setup. Simulation results and self-heating behavior are presented in Sections III and IV,

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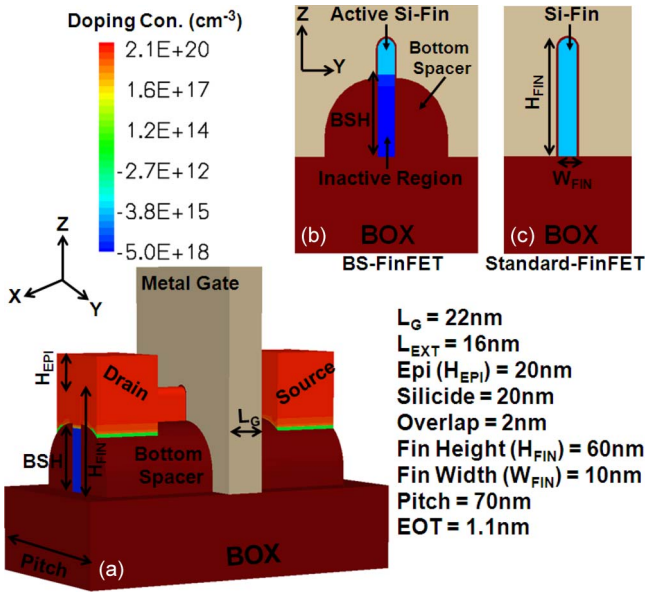

Fig. 1. Proposed device structure. (a) BS FinFET. Inset (b and c) shows the difference between the fin region of the proposed structure and the standard FinFET device. Important device dimensions are also listed here.

respectively, while Section V summarizes the important findings from this paper.

II. Device Structure and Simulation Setup

Fig. 1(a) illustrates the isometric view of the proposed BS FinFET structure realized using the *Sentaurus Device Editor* [10]. The device structure is similar to the standard FinFET with an added region, which is called the BS, along both sides of the fin region. The BS provides isolation to the inactive fin region from gate contact. The inactive fin under the BS is moderately p-type doped (5×10^{18}) similar to the inactive region in the bulk FinFET [8]. In BS FinFETs, the inactive fin region is isolated from the substrate because of buried oxide (BOX). This feature improves the substrate noise compared with bulk FinFETs. The inset in Fig. 1(b) and (c) shows the difference between the fin region in the standard FinFET and the proposed structure. The important device dimensions are summarized in Fig. 1. The proposed process flow to form the BS region along the fin (as shown in Fig. 2) is explained as follows.

1) Etch silicon (Si) fin over BOX.
2) Isotropic deposition of low-K oxide to form the BS around the Si fin.
3) Anisotropic etching of BS oxide.
4) Mask Si fin using Si_3N_4. Vertical *anti-punchthrough* [P-type for n-channel MOS (NMOS)] implant.
5) Dopant straggle will take place through the BS and eventually dope the inactive (bottom) Si fin region (P-type moderate doping for NMOS).

Processing steps for gate stack and S/D formation are similar to the standard FinFET device as follows: 1) gate oxide formation (high-K) followed by metal/poly deposition; 2) gate stack etch followed by SiO_2 deposition and etching for spacer 1; 3) lightly doped drain implant followed by spacer 2 (Si_3N_4)

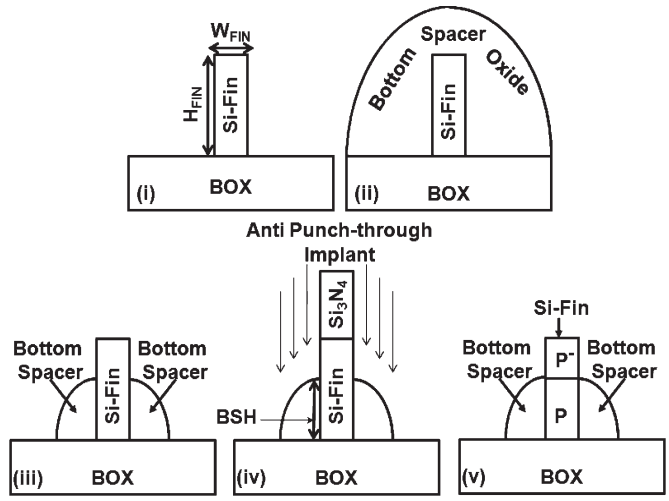

Fig. 2. Proposed process flow to form the BS region along the fin.

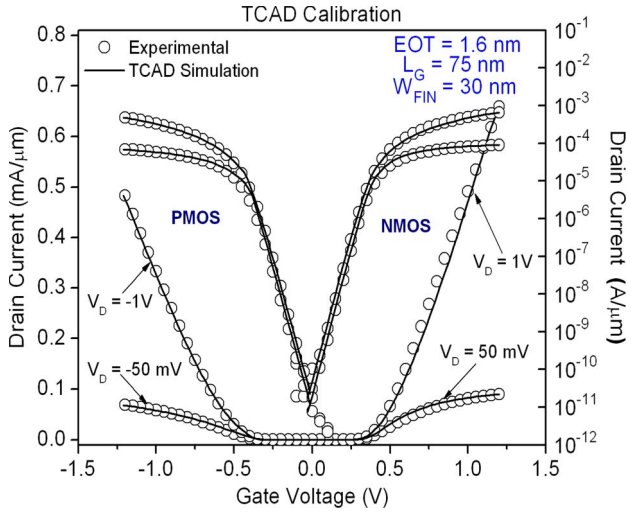

Fig. 3. Calibration of TCAD models for drift diffusion transport with experimental data [2], [14].

formation; 4) epitaxial growth for S/D formation followed by S/D implant; and 5) silicidation.

The BS height (BSH) defines the active channel width of the proposed device through the relation

$$\text{Active channel width} = W - 2\text{BSH} \tag{2}$$

where W is the active channel width of the standard FinFET from (1). The channel length used here is 22 nm, and fin thickness is kept approximately 10 nm to control the short-channel effects. The fin is undoped with a doping density of 1×10^{16} cm^{-3}. The intrinsic fin helps in reducing the random dopant fluctuations [11].

The 3-D device/mixed-mode circuit simulations are performed using *Sentaurus Technology Computer Aided Design (TCAD) tools* [12]. TCAD mobility model parameters for drift-diffusion transport considering quantum correction at the oxide–silicon channel interfaces were carefully matched with measured FinFET data [2], [13], [14], as shown in Fig. 3. The channel in the FinFET is on the sidewall of the fin that lies on

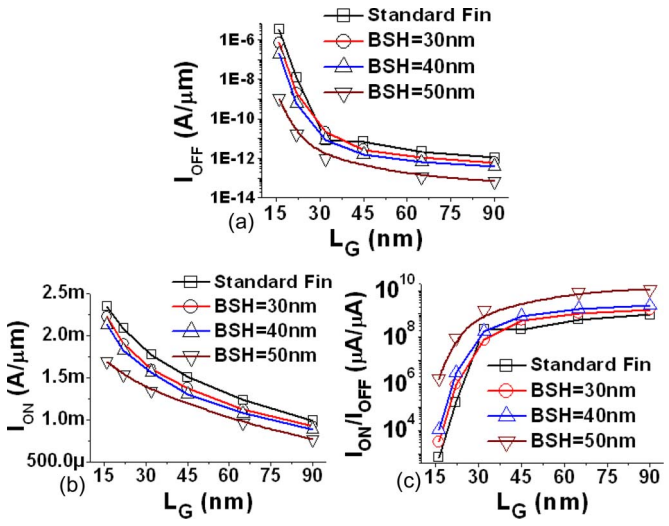

Fig. 4. Intrinsic performance comparison of devices having a different BSH (i.e., 30, 40, and 50 nm) with respect to the standard FinFET structure. (a) $I_{\rm OFF}$ (amperes per micrometer). (b) $I_{\rm ON}$ (amperes per micrometer). (c) $I_{\rm ON}/I_{\rm OFF}$.

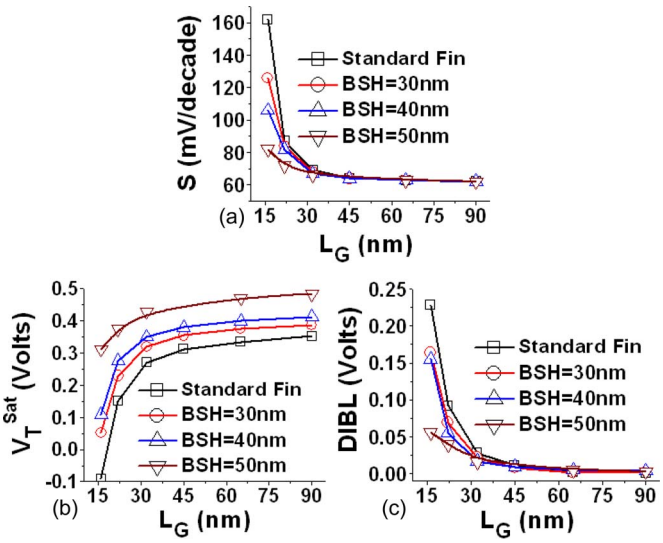

Fig. 5. Short-channel performance comparison of devices having a different BSH (i.e., 30, 40, and 50 nm) with respect to the standard FinFET structure. (a) Subthreshold slope. (b) V_T roll-off. (c) DIBL.

the (110) plane if the device is fabricated on a wafer having orientation (100). Due to dissimilar effective mass values along various axes, hole mobility in the FinFET gets enhanced, and electron mobility gets degraded as compared with conventional planar devices with (100) surface orientation [15]. Sidewall roughness, stress, and strain also affect the mobility. Since the default model parameters of the device simulator are for the (100) plane, mobility model parameters have been modified for the (110) plane. The values of model parameters were then extrapolated to 22-nm L_G devices as described in [16]. The contact resistivity value chosen for all simulations is 2.4×10^{-8} Ωcm^2. A metal gate technology is used, and the threshold voltages are adjusted by modifying the metal work function (4.6 eV for the standard FinFET). All internal 3-D parasitic capacitances of the transistors and the series resistances are taken into account in the 3-D device/mixed-mode circuit simulations.

Briefly, for devices with a different BSH, we found that the ON-current $I_{\rm ON}$ per fin is not scaled linearly, while the OFF-current $I_{\rm OFF}$ per micrometer is suppressed significantly with respect to the BSH or the active channel width. This is attributed to the improved short-channel performance of the devices with a reduced active fin height. The detailed physics of this improvement is discussed in Section III.

III. Simulation Results

A. Intrinsic and Short-Channel Performance

As stated in Section II, the intrinsic and short-channel performance can be improved by reducing the active fin height, as shown in Fig. 4. Fig. 4(a) shows a significant improvement in $I_{\rm OFF}$ (at $V_{DS} = 1$ V and $V_{GS} = 0$ V) for the reduced height of the active fin (i.e., BSH $= 50$ nm) as compared with a standard FinFET structure. However, $I_{\rm ON}$ (at $V_{DS} = 1$ V and $V_{GS} = 1$ V) does not reduce at the same rate as $I_{\rm OFF}$, as shown in Fig 4(b). Furthermore, Fig. 4(c) compares the $I_{\rm ON}/I_{\rm OFF}$ ratio of various devices having a different BSH with respect to the standard FinFET device. For shorter channel lengths,

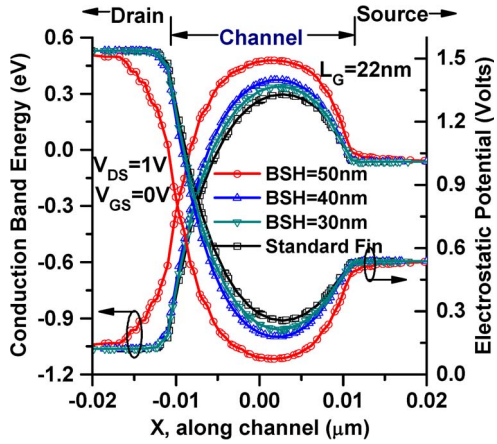

Fig. 6. Electrostatic potential and conduction band energy for a standard FinFET and devices with different values of the BSH along the channel.

$I_{\rm ON}/I_{\rm OFF}$ is significantly improved for devices with a reduced active fin height (i.e., BSH $= 50$ nm).

Fig. 5(a)–(c) shows the improved subthreshold slope, the V_T roll-off, and the drain-induced barrier lowering (DIBL), respectively, for the device having BSH $= 50$ nm as compared with the standard FinFET structure. The reduced $I_{\rm ON}$ (per micrometer) for the device having BSH $= 50$ nm is attributed to a higher threshold voltage ($\sim$0.45 V) as compared with the standard FinFET structure.

To clarify how short-channel performance improves as the BSH increases, variation of the energy barrier between the source and the channel with the BSH is simulated. Simulation results (Fig. 6) show that for a given drain voltage, the energy barrier between the source and the channel increases as the active fin height reduces with an increasing BSH. This leads to improved short-channel performance (i.e., $I_{\rm OFF}$, DIBL, and the subthreshold slope) in the device having BSH $= 50$ nm. This behavior is attributed to the increased influence (control) of the top gate over the channel. As the BSH increases, the effective

fin height reduces, which reduces the effective I_{ON} per fin. Therefore, the optimum value of the BSH is a choice based on the target performance and the required electrical width of FinFET devices in self-loaded circuits, i.e., core logic and SRAM [13] for a given technology.

Devices with a different BSH will have a different BS thickness value. Therefore, it is worth pointing out at this stage that because of the higher BS thickness (40–50 nm) value, the device intrinsic performance and parasitics will not be affected by the tuning of BS thickness for optimum device/circuit performance.

B. Logic Performance

The proposed BS *SOI FinFET* not only provides higher flexibility in fin height sizing but also reduces the overhead of nonoptimal FinFET sizing for digital circuit applications. As the effective height of the FinFET reduces, its effective gate capacitance reduces, and, hence, the FinFET logic gate will be able to achieve the required delay with less power dissipation. This assumption is valid as long as the FinFET loading is not limited by interconnect parasitics or any other height-independent parasitics. In other words, in many digital modules on SoC, the device delay is limited by the gate capacitance, and, hence, significant improvement in dissipated power is expected. Such improvement is demonstrated by the detail simulations carried out in this paper.

To study the impact of the BS *SOI FinFET* on the enhancement of the power-delay characteristic of logic circuits, an inverter with fan out 1 (driving another inverter) is realized and simulated. All 3-D parasitics are captured in 3-D mixed mode circuit simulation. Since BS thickness is much higher than the effective oxide thickness, the parasitic capacitance of the BS does not add an overhead to the FinFET footprint or the main 3-D gate-related capacitances. It is worth mentioning that various parasitic capacitances of the proposed device are similar to the parasitic capacitances of the standard FinFET device as discussed in [13]. To explore the effect of the BSH, we simulated the transistor with the BSH of 30, 40, and 50 nm, and compared the circuit performance with that of a standard FinFET structure. Fig. 7 shows the simulated transient characteristics of various devices with different BSH values compared with a standard FinFET device. The inset in Fig. 7 provides the inverter delay for different transistors. The standard FinFETs result in an inverter delay of 2 ps, whereas the delay increases up to 3.5 ps for the case of BSH = 50 nm. This is partially because of the lower ON current I_{ON} as compared with the standard device and partially because of the 3-D parasitics, which are not scaled linearly with the scaling of the active channel width.

Nevertheless, Fig. 8 shows a 2× improvement in power-delay performance, which is an important figure of merit for logic circuits. The power is the average of the dynamic power loss during one switching cycle. This improvement is attributed to the significant reduction in switching current as shown in the inset in Fig. 8.

It should be noted that the overhead of the BS on the device footprint is not significant. This is because 1) the thickness of

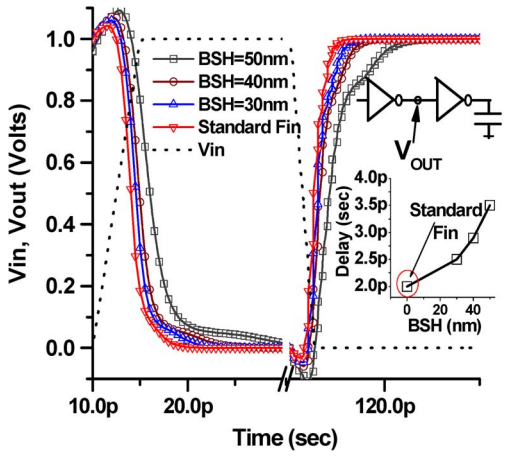

Fig. 7. Inverter transient characteristics of devices having a different BSH. The inset shows a slight increase in the inverter delay as the active channel width reduces (i.e., the BSH increases).

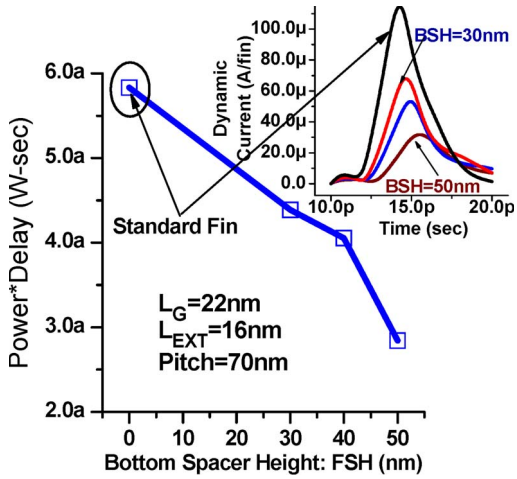

Fig. 8. Power delay product for devices with a different BSH. The inset shows the dynamic current for devices with different values of the BSH.

the BS is always less than the minimum available pitch (here, 70 nm), and 2) the BS is required only where a minimum electrical width is needed, which is the case for single fin devices.

C. Comparison and Discussion

Furthermore, the short-channel performance and the circuit performance of the proposed device having a BSH = 50 nm are compared with respect to the standard FinFET structure, where the gate metal work function of the proposed device is adjusted to achieve an identical 1) V_T (i.e., 150 mV) and 2) delay (i.e., 2 ps). The comparison chart is illustrated in Fig. 9. The figure shows that the proposed device exhibits a 20% higher inverter delay for the identical V_T case, while the other figures of merit such as the short-channel performance and the power dissipation improve significantly. The slight loss in the inverter delay can be attributed to the dominance of the 3-D device parasitic capacitance. Similarly, the proposed device shows a significant improvement in terms of dynamic power

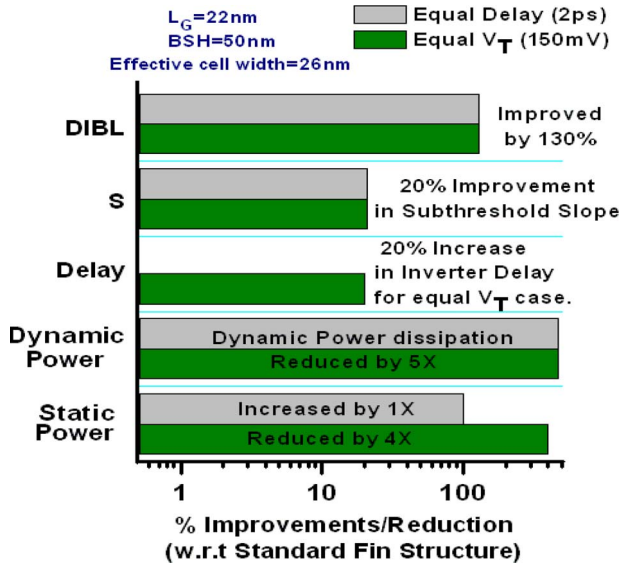

Fig. 9. Short-channel and logic performance comparison of the proposed device with BSH = 50 nm for different cases (i.e., equal V_T and equal delay) with respect to the standard FinFET structure.

dissipation and short-channel performance for an equal inverter delay with respect to a standard FinFET, except for a $1\times$ higher static power dissipation.

At this stage, it is worth mentioning that the basic idea of the BS FinFET is to use it for applications where self-loading (a circuit that requires minimum width transistors) is dominant. $H_{\rm FIN}$ is a parameter that is usually decided prior to fabrication for a particular application (in most of the cases, SRAM). The assumption for scaled technologies is that the interconnect capacitance will dominate for the SRAM compared with the device's parasitic capacitance. To address interconnect capacitance issues, one usually wants to keep as much as possible the height of the fin during the technology development phase. Whereas, in our recent report, we have concluded that even for SRAMs, the device's parasitic capacitance dominates over the interconnect capacitance [13]. This means that for the logic circuit block having local interconnects and SRAM cells, higher electrical widths are not required, which can be easily done by using shorter fins. Whereas, very short fins lead to longer intrinsic delays because some of the parasitic capacitances do not scale with the fin height. Furthermore, having very short fins leads to the requirement of many fingers, where a higher effective electrical width is needed, i.e., for global interconnect drivers or for most of the analog/RF applications (e.g., operational amplifiers, RF power amplifiers, line drivers, etc.). Hence, when SoC is a concern, a shorter fin will lead to larger area consumption as compared with a taller fin (higher $H_{\rm FIN}$) device.

To address both issues, the BS process is proposed with the standard FinFET process for SoC applications where logic/SRAM needs a minimum width (i.e., single fin device) device [13] and an analog/RF circuit or global interconnect drivers need devices with higher electrical widths. For the logic and SRAM circuits, a BS can be used to reduce the excess electrical width associated with the height of the single fin and to improve the power-delay product. For analog and RF applications, the BS can be blocked to achieve a higher electrical width or multifin structures.

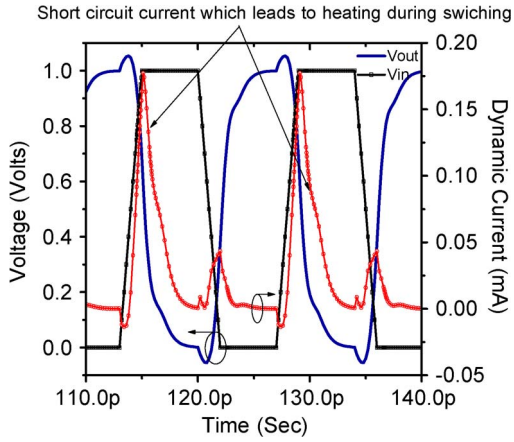

Fig. 10. Transient input/output characteristics of an inverter driving another inverter and the dynamic (short circuit) current through the active (i.e., NMOS or PMOS) device during the inverter switching operation.

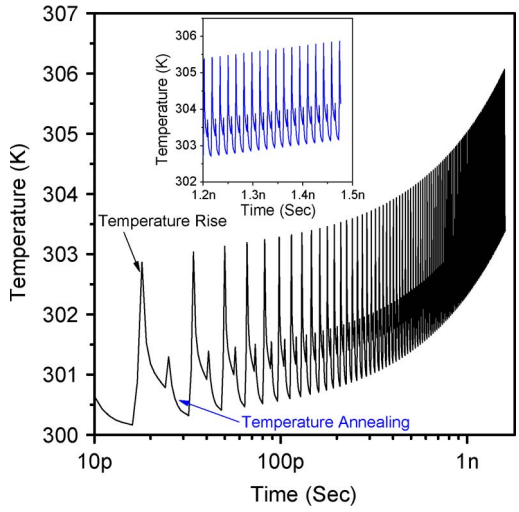

Fig. 11. Transient evolution of temperature across the device. During any inverter cycle, $\Delta T = (T_R - T_A) > 0$, where T_R and T_A are the temperature rise and the annealed temperature, respectively, during that inverter cycle.

IV. Electrothermal Behavior

Fig. 10 shows the transient input/output characteristics of an inverter driving another inverter and the dynamic (short-circuit) current through the active [i.e., NMOS or p-channel MOS (PMOS)] device during inverter switching operation. The figure shows that the short-circuit current through the respective (i.e., NMOS or PMOS) active device is maximum during the switching operation, which causes a short-circuit power dissipation and eventually leads to joule heating, i.e., temperature rise across the active device.

Fig. 11 shows that the temperature rise is a function of time. During the switching operation, when the short-circuit current is maximum, the temperature across the device increases. Whereas, when the input and output pulse stabilizes at V_{DD} and V_{SS}, respectively (and also during switching from V_{SS} to

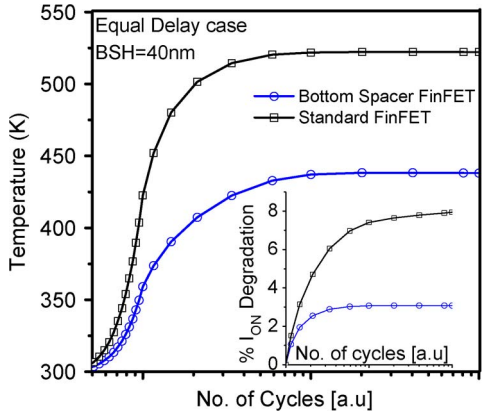

Fig. 12. Temperature rise and % $I_{\rm ON}$ degradation with respect to the number of cycles of inverter switching.

V_{DD}), the short-circuit current through the active device goes to a minimum value (Fig. 10). This leads to annealing or a temperature relaxation.

Fig. 11 shows that during any inverter cycle, $\Delta T = (T_R - T_A) > 0$, where T_R and T_A are the temperature rise and the annealed temperature, respectively, during that inverter cycle. Since ΔT is always greater than 0, a continuous rise in temperature takes place across the device even after 100 pulses (Fig. 11). Furthermore, Fig. 12 shows that during initial time periods, the temperature rises across the device, but eventually saturates to a value $T_{\rm MAX}$ after a few hundreds of thousands of pulses (a few microseconds for a pulse train with a pulse width of 14 ps). This means that $T_{\rm MAX}$ is a more important parameter than ΔT, which leads to device degradation. $T_{\rm MAX}$ across the device will depend on the thermal power density inside the device and the thermal boundary conditions (i.e., cooling conditions) around the device. Fig. 12 shows that the BS FinFET has a lower temperature rise and % $I_{\rm ON}$ degradation as compared with the standard FinFET device. The increase in temperature leads to higher lattice vibrations and increased carrier scattering, which adversely affects the carrier mobility and eventually degrades the device performance (i.e., $I_{\rm ON}$).

The cause for lower heating in the proposed BS FinFET as compared with the standard FinFET device is elaborated in Figs. 13 and 14. Fig. 13(a) shows that the lattice heating or temperature rise occurs at the drain-to-channel junction, where the electric field E and the current density J are both maximum $(\Delta T \propto \int J \cdot E dt)$. Furthermore, Fig. 13(b) and (c) shows that maximum heating occurs in the lower part of the fin (because of higher current density), and the maximum heat flux is through the metal gate instead of the source/drain contact. Since the gate oxide has negligible thickness and since the metals have a good thermal conductivity as compared with silicon and oxide (BOX), the maximum heat flux occurs through the metal gate, i.e., the heated fin gets cooled primarily because of the transfer of heat through the metal gate. Fig. 14 shows that the BS FinFET has heating at the drain-to-body junction in the *active fin* region. Since the BS FinFET has a lower electrical width, it leads to a lower thermal power density in a given volume (Si fin). Furthermore, the metal gate in both

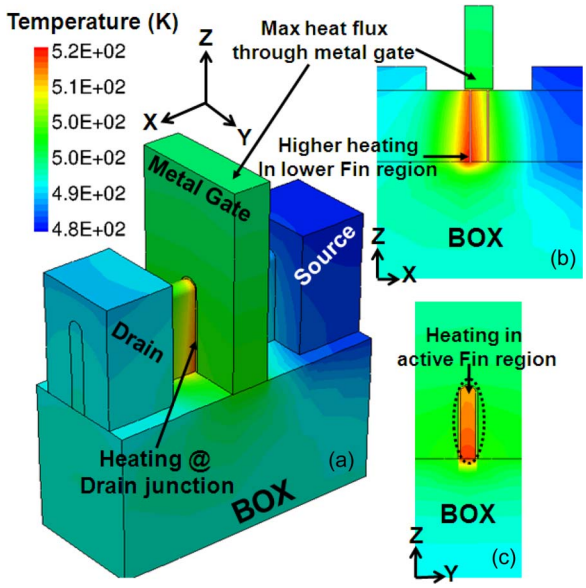

Fig. 13. (a) Self-heating behavior across the standard FinFET device. (b) and (c) Maximum heating occurs in the lower fin region, and the maximum heat flux (i.e., cooling) is through the metal gate.

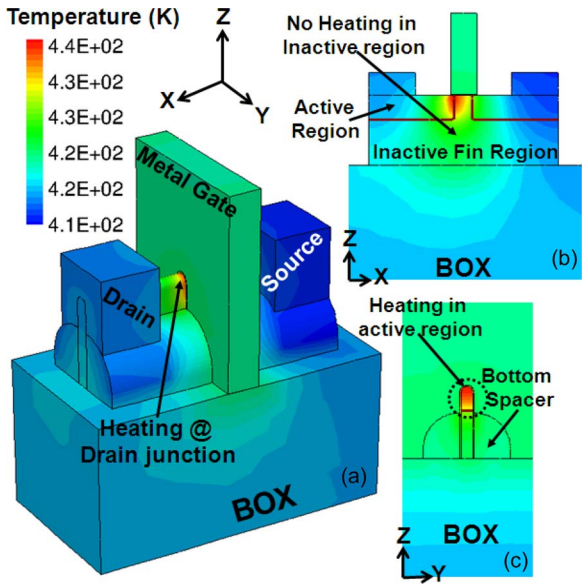

Fig. 14. (a) Self-heating behavior across the proposed BS FinFET device. (b) and (c) Maximum heating occurs in the active fin region. The proposed device gets better cooling because of lower thermal power density and a similar volume for heat diffusion.

devices has a similar volume for heat diffusion, and, hence, the proposed device lowers the thermal issues in FinFETs. This eventually leads to a lower $T_{\rm MAX}$ and device degradation $I_{\rm ON}$ in the proposed device.

V. Conclusion

In this paper, we have proposed a solution toward the problem of width quantization in FinFET technology for SoC applications. For the first time, we have proposed a novel BS FinFET structure to achieve improved short-channel performance and lower power dissipation. Process aspects of the proposed device have also been discussed. The proposed device

can be manufactured in a standard SOI FinFET process with the addition of an extra implantation step, whereas the same device can be fabricated in the bulk FinFET process without the need for even an additional masking step. It has been shown in this paper that reduction of the active fin height by the proposed method considerably reduces the static and dynamic power dissipation, while improving the short-channel performance significantly. Detailed 3-D simulations give a thorough physical insight into the tradeoffs involved with this device design in terms of the delay and the power dissipation. The proposed structure, because of its additional electrically inactive fin area, has also been shown to be highly effective in alleviating the self-heating problems in FinFETs.

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